Conference on

EEE Components for Space Applications
(EEE-Con 2017)

PROCEEDINGS

April 2017

ISRO SATELLITE CENTRE

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भारतीय अन्तरिक्ष अनुसंधान संगठन
अन्तरिक्ष विभाग
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आ. सी. किरण कुमार / A. S. Kiran Kumar
अध्यक्ष / Chairman

Message

I am glad to note that ISRO Satellite Centre is organizing a Conference on "Electrical, Electronic and Electromechanical (EEE) Components for Space Applications (EEE-CON 2017)" on April 25, 2017 at Bengaluru.

It is vital to sustain a constant supply chain of high reliability EEE components for the space programme, while meeting the challenges associated with their availability. Considering the fact that a significant part of the EEE component requirement in the country is dependent on imports, this area must receive focused attention within the "Make-in-India" strategies.

I sincerely hope that the conference will serve as a platform for sharing the experience among the ISRO Centres, industry & academia, and enable focused efforts in generating the essential IPs and build end-to-end indigenous capability within the country.

I convey my best wishes for the grand success of the Conference.

आ सी किरण कुमार
(A S Kiran Kumar)

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डॉ. एम. अण्णादुरै
Dr. M. Annadurai
निदेशक / Director

MESSAGE

ISRO Satellite Centre, Bangalore is primarily responsible for the realization of large number of satellites every year to meet the demands of the country in various application areas which include Communication, Navigation, Earth observation etc. EEE Components are the basic building blocks for all electronic systems which in turn determine the quality and long term reliability of spacecrafts.

In view of the current satellite productionisation scenario, involvement of Industries and ZeeDP initiatives taken up in the center there is a need to address all the aspects related to EEE components management, end to end.

The present Conference on EEE Components for Space Applications **EEE- Con 2017** is expected to discuss and consolidate all the techno managerial issues with the participation of all the stakeholders.

I wish the Conference a grand success.

एम. अण्णादुरै

(डॉ. एम. अण्णादुरै)
Dr. M. Annadurai

तपन मिश्रा
निदेशक
Tapan Misra
Director

भारत सरकार GOVERNMENT OF INDIA
अंतरिक्ष विभाग DEPARTMENT OF SPACE
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MESSAGE

I am very happy to note that ISRO Satellite Centre, Bengaluru, is organizing a Conference on "EEE Components for Space Applications" at Bengaluru on April 25, 2017.

The Space programme in India over the years has contributed significantly towards various application areas for the national development. EEE Components management is one of the key areas enabling the realization of long mission life of spacecrafts.

I am sure this Conference will provide a good opportunity to present and show case the capabilities developed in ISRO, Industries and academic institutes in the area of EEE Components. This Event will also provide a platform to discuss the advances and challenges in the area of EEE Component Management.

I wish the Conference a grand success.

Tapan Misra

(तपन मिश्रा)
(Tapan Misra)

Place: Ahmedabad
Date: 21 April 2017

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एस सोमनाथ/S. Somanath
निदेशक/Director

MESSAGE

I am happy to note that a Conference on "EEE Components for Space Applications – EEE-Con-2017" is being organised at ISRO Satellite Centre, Bengaluru on 25 April 2017.

Ultra reliable Electrical, Electronics and Electromechanical components play very significant role in our space missions, both launch vehicle and spacecrafts. The conference topics related to parts management and inventory control, COTS usage, counterfeit mitigation, new and improved components and its packaging technologies are very relevant topics to be discussed and brought to the attention of the community in ISRO dealing with such issues on a regular basis.

I am also delighted to note that there is participation from all ISRO Centres as well as academic institutes, industries and vendors. This Conference will provide a platform for them to exchange their experience & expertise and to discuss the new trends & challenges ahead. I am sure that the deliberations in this conference will be extremely useful and productive for the professionals engaged in this vital area.

On this occasion, on behalf of Liquid Propulsion Systems Centre, I extend my warm greetings and felicitations to the organisers and delegates.

I wish the conference all success.

18 April 2017

[S. SOMANATH]

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Dr. G.N. Rao
Director, LEOS

MESSAGE

I am extremely delighted to know that Reliability & Quality Area of ISRO Satellite Centre is organizing the EEE Conference - 2017 on 25th & 26th April 2017 at ISAC, Bengaluru.

This conference is very timely and appropriate, since EEE parts play a crucial role in the design and analysis of present Aerospace systems.

I hope this conference will be useful in the design & development of various advanced electro-optical sensor systems in LEOS.

I am sure that the meet will provide platform for all EEE parts professionals to have fruitful interaction and exchange ideas. I hope this meet will inspire academic institution and research organisation to take up challenges in the development of state of the art electrical and electronic components available for space application through collaborative efforts.

I convey my sincere greetings and best wishes for the success of the National conference.

Jai Hind

जी. एन. राव
19/4/2017

April 19, 2017 **[Dr. G.N. RAO]**

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एम वी ढेकणे / MV Dhekane
विशिष्ट वैज्ञानिक / Distinguished Scientist
निदेशक/DIRECTOR

MESSAGE

I am extremely glad to note that ISRO Satellite Centre, Bengaluru is organising a conference on EEE Components for Space Applications (EEE-Con 2017) from 25th to 26th April 2017 at ISAC, Bengaluru.

Over the last few decades, world has witnessed a paradigm shift in the electrical, electronic and electromechanical component sector across all regions. There has been significant focus on the industries manufacturing these components and driven by their global competence, especially for aerospace applications. ISRO over a period of time has streamlined the EEE component management protocols giving due importance to their qualification and also to ensure reliability throughout the intended life cycle of systems using these components. At this juncture, the conference on EEE component management is most apt as it will provide a platform to discuss the emerging concepts with regard to not only newer technologies of manufacturing, but also on the reliability, failure analysis, indigenisation, obsolescence management etc. The mitigation technique with regard to counterfeit components is a major challenge to the aerospace component managers which needs focussed attention and solutions.

I have no doubt that this conference is going to be a step forward in India's Space odyssey in an era when we are ready to explore other planets. I am sure that the conference will provide a forum where engineers, researchers, academicians and industrial partners can network and exchange ideas on the latest developments and also set new goals to be achieved in this area of robust EEE component management for future.

I wish the conference a great success and convey my best wishes to all delegates for fruitful interactions and deliberations.

Dhekane

April 19, 2017

(MV DHEKANE)

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MESSAGE

I am extremely happy to learn that ISAC is organising EEE-Con 2017 during 25-26 April 2017. This Conference provides a common platform for all those under the umbrella of EEE to come together, exchange / consult / discuss the happenings and the current developments on this field. The field of EEE is taking rapid strides and accelerating itself towards plentiful innovations. This congregation is sure to pave the way for sharing of knowledge and expertise among the fellow participants.

The Conference is certain to bring a better synergy among the academic institutions, industries, vendors and the Engineering community. A wide range of inter-related topics has provided a holistic approach to understand nitty-gritty of the subjects involved.

The souvenir portraying the proceedings are well compiled and congratulations to all those who made this conference possible. I am sure this Conference will stimulate the participants towards greater challenges ahead. Wish the Conference all success.

V.V. Srinivasan

(V V SRINIVASAN)
DIRECTOR, ISTRAC

April 20, 2017
BANGALORE-58

Surinder Singh
Director
Semi-Conductor Laboratory

Message

It is heartening to know that a Conference on Electrical, Electronics & Electromechanical (EEE) Components for Space Applications (EEE-Con 2017) is being organized on April 25 & 26, 2017 at ISRO Satellite Centre, Bangalore.

An effective management of EEE Components is crucial for scaling-up and timely realization of space missions. Space environment, with many extremes, require a completely different approach in terms of raw material, fabrication, quality concerns and reliability of the highest order.

I am sure that deliberations in the Conference by Academic Institutes, Industries and Vendors will bring-out newer and innovative approaches for EEE Components in Space Applications.

I wish all the success to EEE-Con 2017.

(Surinder Singh)

April 19, 2017

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DR M.RAVINDRA,
OUTSTANDING SCIENTIST
CHAIRMAN, ORGANISING COMMITTEE

Message

ISRO Satellite Centre, Bangalore has entered a productionsation era with Zero Defect Programme approach, targeting realization of more than 12 satellites per year, to meet our commitment to the country for continued and improved satellite based services.

Towards achieving this target, one of the key factors is Reliability and Quality Assurance management of EEE Components. Also there is a need to address the various challenges related to advanced technology devices, diminishing manufacturing sources, obsolescence, counterfeit parts etc.,

The present Conference on EEE Components for Space Applications EEE-Con 2017 is expected to discuss and consolidate all the techno-managerial issues with the participation of all the stakeholders.

On behalf of the Organizing Committee, I extend a warm welcome to all the delegates and wish them fruitful deliberations.

WISHING THE CONFERENCE A GRAND SUCCESS.

20TH April 2017

(Dr.M.Ravindra)
Deputy Director, RQA/
Chairman, Organising Committee

From the Editorial Committee

Towards the pursuit of the intended Quality objective of zero defect delivery of space systems, the Reliability and Quality Assurance (R&QA)of Electrical, Electronic and Electromechanical (EEE) Components play a critical role in realizing reliable on-orbit performance of spacecraft systems. The conference on **`EEE Components for Space Applications** ‘provides an excellent platform to share the best practices, skills, lessons learnt and innovative EEE Components management aspects those are in vogue in our Indian Space Research Organization.

Editorial committee received overwhelming response in a short span of time from all ISRO centres, academia and industries &shortlisted 53 papers falling in line with the theme of the conference. The topics of the papers cover a wide spectrum of areas ranging from R&QA of EEE Components, Failure Analysis & Destructive Physical Analysis (DPA) of Components, Radiation Hardness Assurance, Indigenisation, Commercially Off The Shelf (COTS) components, Storage and Handling, Obsolescence, Counterfeit Components, Fabrication and Testing Processes & Methodology. Few papers highlight the management aspects for space programs such as supply chain management, quality management, Inventory management and Components Management for Off-The Shelf Avionics. Topics related with challenges in Reliability and Quality for both spacecraft and Launch Vehicles in the above topics are widely covered in the shortlisted papers.
With this high volume of response, the committee has spent considerable amount of time and effort in completing the editorial assignment in spite of the pressing project schedules, we seek pardon for any omissions in our final output.

We as part of editorial committee feel proud to be associated with the conference. We are amazed to see the response and quality of articles received. We are happy to present the compendium of this conference with the expectation that this initiative will be highly useful for the future development for EEE components management for space applications. On behalf of Editorial Committee, we humbly acknowledge encouragement & unflinching support from Director, ISAC, Senior Colleagues, organizers and reviewers.

We are proud to put forth EEE-Con2017 conference proceedings for you.

Editorial Committee

PROGRAMME SHEET

CONFERENCE ON
EEE COMPONENTS FOR
SPACE APPLICATIONS
[EEE-Con 2017]

ISRO SATELLITE CENTRE, BENGALURU

April 25, 2017 (Tuesday)

Satish Dhawan Auditorium

09:30 AM – 11:00 AM

INAUGURATION

Invocation	
Welcome and Program Overview	**Dr. M. Ravindra** **Chairman, Organizing Committee** **EEE-Con 2017**
Lighting of the Lamp	
Address by Director	**Dr. M. Annadurai** **Director, ISAC**
Inaugural Address	**Shri A. S. Kiran Kumar,** **Chairman, ISRO/Secretary, DOS**
Release of Conference Proceedings	
Keynote Address	***Nanotechnology and Internet of Things*** **Prof. V.Ramgopal Rao** **Director, IIT Delhi**
Vote of Thanks	**Shri Kinshuk Gupta** **ISAC**

Programme at a Glance

Time/Venue	Satish Dhawan Auditorium	MOCC Conference Hall
11:10 AM - 01:00 PM	Technical Session 1 A	Technical Session 2 A
01:00 PM - 02:00 PM Lunch Break		
02:00 PM - 03:30 PM	Technical Session 1 B	Technical Session 2 B
03:30 PM - 04:30 PM	Panel Discussion "EEE Components – Advances and Challenges"	

Technical Session 1A

SATISH DHAWAN AUDITORIUM, **11.10 AM – 01.00 PM**

11:10 AM - 11:30 AM	*Components for Launch Vehicle Applications* ***Dr. Valsa B*** ***Dy.Director, SR , VSSC,Thiruvananthapuram***
11:30 AM - 11:50 AM	*EEE Component Management for Spacecrafts* ***Shri. V.Venkatesh*** ***Group Director, PMPG, ISAC, Bengaluru***
11:50AM - 12:10PM	*Components for Payload Applications* ***Shri. A.K.Lal*** ***Group Director, SR, SAC, Ahmedabad***
12:10 PM - 12:30 PM	*ASICs for Spacecraft/Launch Vehicles* ***Shri H.S.Jattana*** ***Group Head, DPG, SCL, Chandigarh***
12:30 PM - 12:50 PM	*MEMS Packaging for Space Applications* ***Dr. M.M.Nayak*** ***Emeritus Professor, IISc., Bengaluru***
12:50 PM - 01:00 PM	*Discussions*

Technical Session 1B

SATISH DHAWAN AUDITORIUM **02.00 PM – 03.30 PM**

02:00 PM - 02:20 PM	*Special Parts for Space Applications (Opto-electronic and Electro-optic Devices)* ***Shri.L.V.Prasad*** ***Group Director, CSSG, LEOS, Bengaluru***
02:20 PM - 02:40 PM	*Component Management – Industry Perspective* ***Shri. Vinod Chippalakatti*** ***VP, SEBU, Centum Electronics Ltd, Bengaluru***
02:40 PM - 03:00 PM	*University Satellites – Challenges & Benefits* ***Prof. DVA Raghava Murthy*** ***Director, Aerospace Research, Veltech University, Chennai***
03:00 PM - 03:20 PM	*Initiatives towards Global Leadership in Hi-Rel Components* ***Anurup MS*** ***ISRO HQ , Bengaluru***
03:20 PM - 03:30 PM	*Discussions*

Technical Session 2A

MOCC CONFERENCE HALL, 2nd FLOOR — 11.10 AM – 01.00 PM

11:10 AM - 11:25 AM	*Manufacturing Process and technology trends for silicon solar cell fabrication* *Dr. Sandeep Chandranil* *DM, SCPV Engineering, BHEL, Bengaluru*
11:25 AM - 11:40 AM	*Recent trends in Failure Analysis methodologies for sub-micron devices* *Dr. C Ramachandra* *Jain University, Benagluru*
11:40 AM - 11:55 AM	*Inventory Management & Storage of EEE Parts for Space Payloads* *Jayesh Jesalpura* *SAC, Ahmedabad*
11:55 AM - 12:10 PM	*Chip Capacitor for RF Applications & Associated Failure Mechanisms* *Dr. Kamaljeet Singh* *ISAC, Bengaluru*
12:10 PM - 12:25 PM	*Components Management for Off-The Shelf Avionics* *Dr. J.K. Kishore* *ISAC, Bengaluru*
12:25 PM - 12:40 PM	*Failure Analysis tools and techniques for Hi-Rel Electronics* *Meghal Ashvin Desai* *SAC, Ahmedabad*
12:40 PM - 12:55 PM	*Process of multilayer ceramic chip capacitors for hi-reliable applications* *Dr. Thandavan Settu* *Dalmia Industries, Bengaluru*
12:55 PM - 01:00 PM	*Discussions*

Technical Session 2B

MOCC CONFERENCE HALL, 2nd FLOOR — 02.00 PM – 03.30 PM

02:00 PM - 02:15 PM	*New Packaging Configuration of CCGA1752 leading to Challenges in its Assembly Process Reliability Assessment* *Ishwar Lal Prajapati* *SAC, Ahmedabad*
02:15 PM - 02:30 PM	*Overview of COTS Component Selection, Qualification, Subsystem Engineering, Redundancy Techniques and Testing for Nanosatellites* *Dr.Swarna Bai Arniker* *DSST, RCI, Hyderabad*
02:30 PM - 02:45 PM	*Component Obsolescence Risk Analysis and Mitigation Strategies for I&C Systems of Nuclear Power Plant* *Rajendra Prasad Behera* *IGCAR, Kalpakkam*
02:45 PM - 03:00 PM	*Counterfeit Part Control Plan and Obsolescence Management of EEE parts in Space systems* *Abhilasha Prasad* *ISAC, Bengaluru*
03:00 PM - 03:15 PM	*Robustness in Design, Fabrication, Testing of indigenous Connectors and induction into Launch Vehicle Application* *Thomas Varughese, Dr. KT Oommen Tharakan* *VSSC, Thiruvananthapuram*
03:15 PM - 03:30 PM	*Device Manufacturing Integration System-Tool for Best Practices in VLSI Fab* *Parveen K. Bangotra SCL, Chandigarh*

KEYNOTE ADDRESS

Nanotechnology & the Internet of Things

Prof. V.Ramgopal Rao Director, Indian Institute of Technology, Delhi

Nanotechnology is all about dealing with nanomaterials and devices and exploiting the size dependent phenomenon for building new applications and find solutions to the existing problems. High surface to volume ratio and novel properties of materials at the nano-scale are important aspectsthat can be specifically exploited for sensors and sensor systems. Internet of Things (IoT) can essentially benefit from this aspect of nanotechnologies in order to develop low cost sensors and sensor platforms having a high sensitivity, selectivity and functionality. Also, while silicon has been the most widely used material for Nanoelectronics and Micro/Nano-Electro-Mechanical-Sensor systems, polymers and graphene based nano-composites enable fabrication of MEMS/NEMS devices with superior electro-mechanical characteristics as compared to the traditional silicon based materials. Polymer nano-composites are alsoideally suited for low cost disposable sensor applications, as well as for applications that require high surface stress sensitivity. This talk discusses the current status of research withnano enabled MEMS/NEMS devices for IoT applications.

Dr. V. Ramgopal Rao is currently the Director, IIT Delhi. Before joining IIT Delhi as Director in 2016, Dr. Rao was a P. K. Kelkar Chair Professor in the Department of Electrical Engineering and the Chief Investigator for the Centre of Excellence in Nanoelectronics project at IIT Bombay. Dr. Rao has over 400 publications in the area of Electron Devices & Nanoelectronics in refereed international journals and conference proceedings and is an inventor on 35 patents (including 13 issued US patents) and patent applications, with many of his patents licensed to industries for commercialization. He is a co-founder of the company NanoSniff Technologies Pvt. Ltd. at IIT Bombay which is developing products in the area of Nanotechnology.

Prof. Rao's work is recognized with many awards and honors in the country and abroad. He is a recipient of the Shanti Swarup Bhatnagar Prize in Engineering Sciences in 2005 and the Infosys Prize in 2013. Dr. Rao also received the Swarnajayanti Fellowship award from the Department of Science & Technology, IBM Faculty award, Best Research award from the Intel Asia Academic Forum, Techno-Mentor award from the Indian Semiconductor Association, DAE-SRC Outstanding Research Investigator award, NASI-Reliance Platinum Jubilee award, J.C.Bose National Fellowship, Prof. C.N.R.Rao National Nanoscience award, VASVIK award and the Excellence in Research Award from IIT Bombay. Prof. Rao was an Editor for the IEEE Transactions on Electron Devices during 2003-2012 for the CMOS Devices and Technology area and currently serves on the Editorial boards of various other international journals. Dr. Rao is a Fellow of IEEE, the Indian National Academy of Engineering, the Indian Academy of Sciences, the National Academy of Sciences, and the Indian National Science Academy. He is a Distinguished Lecturer, IEEE Electron Devices Society and interacts closely with many semiconductor industries including Intel, IBM, Infineon, Applied Materials, Maxim and Texas Instruments.

For more information about Prof. Rao's current research interests and a list of publications visit: http://www.ee.iitb.ac.in/~rrao/.

INVITED SPEAKERS

"Reliability Aspects of Electronic Components used in Launch Vehicles"

Dr.Valsa.B, Deputy Director, Systems Reliability, VSSC

This presentation briefly explains the basic selection criteria and the screening practices followed for achieving the required Quality and Reliability of EEE components for launch vehicle application. Each launch vehicle uses about 20,000 active parts and 60,000 passive parts. Most of the components are very critical for mission success. Failure of any one of these components may cause mission failure. The service condition includes Shock, Temperature, Vibration. VSSC has adopted certain R&QA practices for EEE components which has undoubtedly contributed to a great extent in realizing successive successful missions.

The components range from very complex micro controllers , micro processors, FPGAs, ASICs, memories, data acquisition parts such as ADCs, DACs, linear and digital ICs, HMCs, relays, converters, RF and microwave parts and passive parts. Details are provided on the criteria for selection of parts and the necessity for qualification. Based on the technology, the policy followed for each category and the methodology of acceptance is elaborated.

Dr.Valsa.B started her career in VSSC in the year 1985 and currentlyshe is the Deputy Director of Systems Reliability Entity of Vikram Sarabhai Space Centre. She is responsible for the Quality and Reliability of all ISRO launch Vehicles launched by VSSC. Under her leadership the Quality and Reliability of PSLV, GSLV, GSLV Mk III and Reusable Launch Vehicle has been assessed and cleared, and all these Launches have been perfect successes.She has been associated with the launches of all the PSLV missions and played a key role in assuring the quality of the most recent mission PSLV C37, which meticulously launched the 104 satellites. The team led by her had a major role in ensuring the quality and reliability resulting in the consecutive successes of 38 PSLV missions.

She is leading a team of 210 Engineers working in all disciplines like – Mechanical, Chemical, Electronics and Software systems of the Launch Vehicle. Before every launch Dr.Valsa gives the quality assessment of the launch Vehicle to Mission Readiness Reviews, assuring all systems are in good health and can be cleared for launch.She has also significantly contributed in the Mars Mission where the software for a payload MENCA which studied the atmosphere contents of Mars, was reviewed and cleared by her. The Reusable launch Vehicle also posed many quality challenges as many of the technologies used were new, which were successfully resolved.

Before becoming Deputy Director, Dr.Valsa was Group Director of Software Quality Assurance Group.She was one of the first few members of Software Quality Division when it was formed in 1994 after the PSLV D1 failure which was due to a software error. She played a key role in establishing and sustaining a world class Independent Verification & Validation(IV&V) facility for evaluating Flight Software. The software IV&V facility thus set up is first of its kind in ISRO.

She was also the Management Representative of the Quality Management System (ISO 9001:2008) of VSSC for about 4 years(2011 to 2014), and was leading a team of about 130 auditors and organised two internal audits and two external audits every year.

EEE Component Management for Spacecrafts

V. Venkatesh, Group Director, Parts Materials and Process Group, ISAC, Bangalore

The talk on EEE Component Management for Spacecrafts by Mr.V.Venkatesh outlines various Reliability and Quality Assurance requirements of EEE Components for Spacecrafts. A robust EEE Components management approach is one of the key factors to ensure a successful and reliable satellite mission. In view of increased productionisation, industry involvement and Zero Defect Initiatives, there is a great thrust on strict configuration control and smooth work flow among various fabrication/testing agencies. Towards this, the talk addresses various aspects of Reliability & Quality Assurance including procurement, screening, qualification, storage & handling, Radiation Hardness Assurance, Failure Analysis and Inventory Management of EEE components at ISAC. The talk also addresses various global challenges related to Supply chain management, Obsolescence, Counterfeit parts, COTS etc.,

V.Venkatesh received his B.Tech in Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Andhra Pradesh and M.Tech in Microwave and Optical Communication Engineering from IIT, Kharagpur.

He joined Communication Systems Group, ISRO Satellite Centre in 1985. He was responsible for Design and Development of various TTC Antennas and Microwave Passive Networks for IRS and Geosat spacecrafts. He worked as Project Manager for INSAT-2C/2D/2E/3C and as Deputy Project Director for INSAT-3A for TTC-RF system.

In 2002 V.Venkatesh took over as Head, Thin Films Section in the erstwhile Indigenisation and Components Group and was responsible for Development and Qualification of Thin Film Microwave Integrated Circuits for onboard use. As Head, Hybrid Microcircuits Division, he guided the team towards the realization of High Power DC-DC Converter HMCs and vendor development for Thick Film HMCs.

Presently, V.Venkatesh is Group Director, Parts Materials and Process Group, leading a team of over 50 Engineers working in the area of HMCs, Thin Film MICs and Quality Assurance of EEE Components, Materials, PCBs & Electronic Assemblies.

V.Venkatesh has more than 50 technical papers to his credit in various National and International Journals and holds an European patent for the 'Hand-Held Antenna for Satellite Phone – Fabrication Methodology'.

He is a recipient of ISRO Team Excellence Award for the year 2015 for Zero Defect Delivery of Space Systems and participated in the 'Quality Improvement Programme' at NASA during October 2016.

V.Venkatesh is a Fellow of IETE and Life Member of 'International Microelectronics Assembly & Packaging Society - India Chapter' and Astronautical Society of India.

Components for Space Applications

A.K. Lal, Group Director, SR, SAC, Ahmedabad

Unlike Spacecraft systems and Launch vehicles, payload development demands an ever changing variety of functions, while reducing size, weight and power. This in turn envisages the use of state of the art cutting-edge technologies in the field of EEE components. At Space Applications Center (SAC) a variety of components are used, with are state of the art technologies. These include use of MMICs and GaN technologies for communication payloads, advanced imaging sensors for remote sensing payloads and Opto-Electronic components for Free Space Optical Communication.

However the major challenge for parts management , is these are available only in Commercial quality, which goes against the established philosophy of Space Grade part management. . SRG, SAC has developed and standardised the approach for the selection and Qualification of such advanced commercial devices. This has been successfully implanted on a wide variety of components, including ADCs, AFEs, sensors and microwave

With the requirement of high resolution and large swath with reduced payload volume, weight and power, state of the art COTS detectors with reduced pixel size as low as 2.2 µm and large image format of 4.2 Mpixel are selected for recent remote sensing payloads. For imaging in Infrared Region (SWIR, MWIR & LWIR) Detectors integrated with active Cryo-Coolers (IDCA) and Micro-Bolometer are being adopted. Unlike traditional passive cooling systems using large size and heavy radiators, these detectors are very compact and use less power to cool the detectors. A wide variety of all these types of detectors are qualified at SAC for space use and used/to be used in recent /current/future missions like Mars Orbiter Mission (MOM), Cartosat Series, ISRO Nano Satellite (INS), Chandrayaan-2, Aditya-L1, Space Docking Experiment (Spadex),etc.Free space optical communication is the new area of development. State of the art Opto-Electronic components like Optical Isolators, Beam Splitters, Band Pass Filters, Fiber Optic Couplers, Directly Modulated DFB Laser Modules etc. are being envisaged for development of free space optical communication link. These components are planned to be screened and qualified at SAC for space use.

ASICs for Spacecraft / Launch vehicle

Sh HS Jatana, Gr Head – Design & Process Group, SCL Chandigarh

The talk dwells onthe brief capabilities and Infrastructure available at SCL for development of a CMOS Product. After stabilizing the 180nm CMOS baseline process, many production batches and eight mask-sets covering 100 designs have been released and fabricated. Highlights impetus given for developmentof process options and variants which could be add-on to the baseline process for giving more flexibility to circuit designers. Keeping in view high gate counts (>5 Million gates) digital circuits, 6 Metal Process released, which results in around 15% saving in the signal-routing area and allow high current (> 16mA) carrying capability for power and output pads has been developed. CMOS is cost –effective for RF designs till 2.5GHz, and RFCMOS PDK has been made available which has process module for Top metal (MT) with 2µm thickness, to enable multiple benefits like high current capability, lower IR Drop, inductors having high Q and high resonant frequency. The talk is focussed around development of various standard products and ASICs for use in space and other applications. Many products in the domain of data converters, data communication and power management developed and these are silicon qualified The brief features of 24-bit ADC, 14 bit pipeline ADC (20 MHz), low power 12 bit ADC, Flash ADC, 12 bit DAC, CMOS Analog Signal Processor, Video Signal Processor, Reconfigurable Data Acquisition Systems (RDAS), C-to-D converter are explained. The talk mentions about the products developed for ISAC, viz. Quad LVDS Tx and Rx with cold spare feature, 16-bit Transceiver (hot insertion, cold spare pads), 16-bit buffer, Octal buffer, Hex Schmitt Trigger Inverter, 8 channel Mux/Demux, CD4093. Numerous Application specific ICs (ASICs) were developed for various ISRO Centres like OBC 2.1/OBC2.2 (RH), Vikram 1601 Processor, Programmable bias generator, RS Encoder, Bexm and programmable LDO's (1.2 V to 3.0V, 1A) As its essential to have library of various IPs that could be used for making bigger chips, details of IPs/Mega Cells developed for use in SoCs were also highlighted like – Rs422 Tx, RS 485, SPI, I2C, Analog comparators, analog mux, PLL which have been silicon validated. The talk gave emphasis on development of Radiation hardening by design (RHBD) standard cell library consisting of 105 cells which has been released and few products like OBC2.2 and CMOS Camera configurator ASIC ver 2.0 fabricated, to meet the radiation tolerant for TID >300krad (Si), SEE tested (no upset /no latch) up to 50 MeV-cm2 /mg. As Read out IC (ROIC) and imaging is an important domain for us, ROIC for MCT (320X256) and two CCD products namely FTI and TDI were developed, after freezing the baseline CCD process. Lastly, the number of ASICs / standard products developed for various units have been summarized.

Received his engineering education from **BITS Pilani** and had a brief stint at CMC Delhi as Software engineer wherein he worked on Railway Computerization Project, and later joined SCL in the CMOS division. He has worked in different areas of CMOS and has vast experience on CMOS design, Devicetesting /, characterization, Test program development on ATE, Silicon debugging, and process Integration / porting over few technology nodes; starting from 5µm to sub-micron nodes. He also worked at **AMS Austria** for ten months on deputation for porting of SCL's CMOS processes at their foundry. He has been instrumental in design of various ASICs and products viz, Data Converters : 12-bit ADC, 14-bit DAC, , signal processor, LVR, LDO's, RAdHARD devices etc. His areas of interest are low power CMOS design,analog design in DSM regime, SOI process development for ultra low power and enhanced mixed signal devices.

Has initiated many new process development modules like HV, SOI, BiCMOS, CCD process technology with back thinning, III-V materials on Si for photonics etc and APS for camera application, ultra-low power circuits (bias of few nA), rail-to-rail OTAs, RHDB SRAM etc.

Also interested in spreading VLSI education and have delivered numerous lectures and tutorials onVLSIDesign & Process Technology atIITs(kharagpur, Kanpur,Madras, Bombay, Roorkee, Guwahati, Ropar, Mandi)NITs (Hamirpur, kurushetra, Manipur, Jalandhar),SAC and VSSC etc.

MEMS Packaging for Aerospace Applications

M. M. Nayak, Centre for Nano Science and Engineering, Indian Institute of Science

Micro Electro Mechanical Systems (MEMS) play an important role in the Aerospace industry. MEMS have features such as small size, less weight, low power, higher sensitivity and better performance. In addition, the ability of mass production of MEMS leads to cost reduction as well. These qualities make MEMS a desirable choice for Aerospace applications. As Aerospace systems tend to be, in some sense, performance driven; robust, integrated and tested packaging schemes have usually been preferred. In this talk, the development, fabrication and testing procedures of MEMS packages for the Aerospace environment will be presented. As an example, MEMS based pressure transducers capable of operation in different pressure ranges with built in electronics for compensation and protection circuitry will be discussed. For this purpose, the in-house designed, fabricated pressure sensor chips are used. They are mounted on headers, wire bonded, encapsulated and packaged as a capsule to withstand extreme environmental conditions such as the over pressure, wide range of temperatures, vibration, mechanical & thermal shock, EMI/ESD effects, long term exposures, corrosion, humidity etc. These packages are tested and calibrated to determine the adequacy of the performance parameters under different pressure ranges and temperatures. The data and results are obtained on these devices with active temperature compensation, zero offset, full scale output (FSO), sensitivity compensation using a single IC ZMD 3150. This IC along with voltage regulator, EMI filters, reverse voltage protection diodes, transorbs, and other electronic components are integrated in a stacked 3 tier PCB assembly. This assembly along with sensor capsule is hermetically sealed in AISI 304 L stainless steel casing using Laser welding technique. The presentation includes detailed analysis of the results on the non-linearity & hysteresis, repeatability, sensitivity and stability obtained during static calibration and temperature extremes. A 2D/3D animation depicting various details of assembly and packaging stages, from die attach on glass - metal sealing, to final electrical connector assembly will be presented

Manjunatha Nayak received D.IISc .and Ph.D.(Engg) degrees in Electronic Design Technology and Instrumentation respectively from 11Sc Bangalore prior to his Bachelor's degree in Electrical Engineering from BMS College of Engineering Bangalore. He was awarded the Ph.D. degree of 11Sc for his thesis on "Sputtered Thin Film Strain Gauges & Pressure Transducer" in the year 1994. Subsequently he carried out his Post doctoral research in Micro Electro Mechanical Systems MEMS) at University of DELFT & TWENTE Netherlands under INSA Invitation fellowship programme , and at Toyohashi university, Japan under JSPS fellowship. He served in ISRO, Dept. of Space for nearly 40 years since 1971 in various capacities. Since then he has grown professionally from Technical Assistant to Scientist/Engineer 'H' and held dual positions as Deputy Director, Semi-Conductor Laboratory, Chandigarh and Director, Launch Vehicle Programme Office, ISRO HQ Bangalore. During his 39 years of service at Liquid Propulsion Systems Centre (LPSC) he has developed and productionised space qualified Pressure Transducers for PSLV, GSLV, gsLV M3, IRS, INSAT, Chandrayaan missions. The Ultrasonic liquid level sensors, depletion sensors and Temperature Sensors for the Launch vehicle programmes of ISRO, Digital Pressure Sensors for Automatic weather stations & Tsunami warning System were developed under his leadership and guidance. He was also responsible for realisation and export of about 8000 nos. of space qualified pressure transducers to European Space Programme, 25 nos. of High out-put Transducers to USA and supply of more than 30000 nos of Transducers to ISRO programmes. Various MEMS Sensors were designed, developed and fabricated with his guidance at SCL for Automotive, Radio Sonde, wind tunnel and Shock tube applications In recognition of his outstanding contributions to ISRO's programmatic activities in various capacities, he was awarded ISRO MERIT Award in 2008. He has also received several other awards for his academic excellence. The best paper award in NSI-1989, SEP France Vikas Agreement Completion award in 1989, NRDC award in 1985, NPE- 1984 special award and Kirloskar Electric company best student award are only a few examples of such recognitions. He has more than 70 publications in refereed international journals, 6 patents and guided 9 Research students. Superannuated from ISRO in June 2011, currently he is a Visiting Professor at Centre for Nano Science and Engineering, IISc, Bangalore, further pursuing his research activities in MEMS.

Special Parts for Space Applications (Opto-electronic and Electro-optic Devices)

L.V.Prasad, Group Director, CSSG, LEOS, Bengaluru

Atttitude Sensors employ Special components; electro-optic or opto-electronic devices either as sensing devices in the front end or as signal processing devices at the back end. These are usually high performance devices in terms of Sensitivity, Responsivity, Efficiency, Range, Noise etc., and are expected to handle incoming signals at micro levels to produce meaningful outputs as required in the further processing chain. There are very few manufacturers across the globe who can supply such devices that can meet the stringent requirements in terms of Performance and Quality and usually offer them at a premium cost, that too in precious foreign currency. Procurement lead times are generally long as many times the manufacture is against a developmental order. Obsolescence, coupled with non-availability due to business strategies is another constant threat to the procurement. All these factors impose a severe constraint on the design that needs to continuously adopt to the availability and on the reliability that depends on the available Quality. In order to overcome these issues, LEOS has taken up the onerous task of indigenizing special devices that are required for its designs. Some of these devices have been successfully developed and flown. The present manufacturing capacity at LEOS adequately meets the demands. This presentation aims to provide a glimpse of the efforts made at LEOS in this high technology area by showcasing some of the devices manufactured, successfully Qualified and flown in ISRO's missions.

Component Management – Industry Perspective.

Vinod Chippalakatti, VP, SEBU, Centum Electronics Ltd, Bengaluru

Space is not only one of the harshest environments that electronics need to operate in, but it's also one of the hardest to replicate. Various Space agencies across the globe, including ISRO establish baseline criteria for selection, screening, qualification, and derating of EEE parts for use on space flight projects.

The grades of EEE components contribute to significant portion to the Quality and Reliability of the Space mission. The characteristic features of Space grade EEE components like low volume requirements versus minimum order quantities, high value, huge amount of technical data pack, pre-shipment clearance requirements, long lead times and limited source of suppliers are to be well understood to strategize the procurement process. The statutory requirements like Export License procedures, documentation and compliance to End use requirements are additional complexities to be addressed.

The ability to understand all aspects of procurement from Design, Preferred Parts List, Procurement Specification, Export licensing procedures, ERP driven ordering and tracking, interaction on technical and commercial areas with the supplier base have made Centum a major turn-key space grade solution provider in Space segment for ISRO.

This talk covers the Industry perspective of component management and gives the capabilities and experience of Centum Electronics team in technical and operational aspects of Space grade EEE component management. The systems followed, ERP tools used, tracking mechanism and interdisciplinary team involvement covering Design, Sourcing and Quality and the roles and deliverables of each of the teams in successful procurement and component management are highlighted in the talk. The lessons learnt, improvements made and overall experiences are also shared.

Vinod S Chippalkatti is the Vice President, Strategic Electronics Business Unit (SEBU) at Centum Electronics Limited, Bangalore.

He has Masters degreein Engineering from Indian Institute of Science and has overall 28 years of experience.He is a fellow of IETE and life member of IMAPS (India). He has around 55 technical papers at the National and International level. He also has applied for 7 patents.

He served Indian Space Research Organization (ISRO) in Bangalore for ten years working on System Integration of INSAT-2 series,India’s first set of Communication Satellites. Subsequently, he joined Centum Electronics in the year 2000 as head of Design and Engineering.

He has been a part of Centum’s growth story as a key member of the management team. He is actively involved in Centum scaling-up to be a leading Indian Industry in Design & Manufacturing of High Reliability and High Technology modules, subsystems and systems in Defense, Space and Aerospace segments

Manufacturing Process and technology trends for silicon solar cell fabrication

Dr. Sandeep Chandranil, DM, SCPV Engineering, BHEL, Bengaluru

The solar photovoltaic manufacturing has grown rapidly in recent years to cater to the exploding solar market driven by sustainability initiative across the globe and crystalline silicon solar cell manufacturing has emerged as the dominant technology capturing more than 90% of the entire market share. The total shipment for solar cells in 2016 was more than 70 GW consisting mostly of crystalline silicon solar cells. The starting material for typical solar cell fabrication is a thin silicon wafer and the essential requirements for the fabrication are a. absorption of the incident light into the wafer, b. generation and separation of charges and c. collection of charges. The various processes utilized for the manufacturing of the solar cells have been developed to address these essential requirements. The absorption of light into the wafer is maximized by the process of texturing the light facing surface and covering it with an anti-reflection coating. The generation and separation of charges is controlled by creating an in-built electric field inside the wafer by creating a p-n junction to direct the motion of the light-generated charge particles. And the collection of the charges generated is carried out by a suitably designed metal grid patterns on the front and the back surfaces of the solar cell. Amongst various manufacturing processes that have been developed for the manufacturing, the most successful processes have addressed the issues of low cost of manufacturing and easy up-gradation to the emerging technologies. These are some of the key factors that have made crystalline silicon solar cells the dominant product for harnessing solar energy. The most common type of solar cell is the aluminum-back surface field (Al-BSF) multicrystalline solar cell. The conversion efficiency of this type of solar cell has gradually moved to about 18% with the process improvements brought about in the recent years mainly in the areas of generation and collection of charges. These issues have been addressed by the quality of the input material and the quality of the printing pastes used for forming metal contacts. Several other cell structure that are occupying smaller market segments or are competing to enter the market are based on the incremental improvements over this conventional cell structure. Notable amongst then are the passivated-emitter-rear-contact (PERC) and Bifacial technologies. Further, the technology trends for the solar cell manufacturing point towards the continued dominance of the silicon based solar cells and to an evolutionary approach leading to incremental gains in the cost of manufacturing and the efficiency of the solar cells

Mr. Sandeep Chandril received PhD in Semiconductor thin films from West Virginia University, USA in 2010. He joined Bharat Heavy Electricals Limited (BHEL) solar cell R&D department at Gurgaon in 2010 and worked on amorphous, crystalline and hybrid silicon solar technologies until 2013 before he moved to Electronics Division-BHEL, Bangalore to work on the crystalline silicon solar cell production. He is presently working in Electronics Division, BHEL, Bangalore on 100 MW multicrystalline silicon solar cell line and his interests are in design and development of crystalline silicon solar cells, PV modules, Solar cell efficiency improvement and PV manufacturing capacity expansion.

Recent trends in Failure Analysis methodologies for sub-micron devices

Dr. C Ramachandra, Jain University, Benagluru

During last four decades, technology nodes of semiconductor devices have developed from 10 micron to below 45 nm. Defects and deviations of submicron scale have started playing significant role in affecting device performance. Array of technological solutions have been developed to identify and capture defects /deviations of sub micron scale.

Semiconductor devices have typically three loops namely Transistor loop, Memory loop and Metal loop. Devices have multi layer structures which include oxide, nitride, metal, Titanium nitride, Poly silicon, Tungsten Silicides, etc. Defects / deviations responsible for the device failure can occur in any of these levels.

Failure analysis methodologies involves basically three phases namely Electrical Failure Analysis (EFA), Fault Isolation Techniques and Physical Failure Analysis (PFA).

Applications and limitations of some of these Fault Isolation techniques such as Passive Voltage Contrast, Liquid Crystal Analysis, Photon Emission Microscopy and Optical Beam Induced Resistance Changes (OBIRCH) etc have been highlighted.

Physical Failure Analysis (PFA) is done to confirm defects / deviations responsible for the observed failure. Importance of sample preparation and deprocessing are highlighted. Deprocessing requires intelligent use of wet and dry etch processes. Scanning Electron Microscopy and Transmission Electron Microscopy play key role in capturing sub micron scale defects / deviations. Convergence of Spectroscopy with Microscopy provides valuable inputs for failure analysis. Use of deprocessing methods for capturing Insufficient Buried Contact (IBC) and Cell to Cell short is shown.

Some of the challenges to be addressed for failure analysis are highlighted. These include development of high selectivity etching, decapsulation of multi chip modules, etc.

Qualification	**M.Sc.,**Physics, Mysore University **M.S.**, Electronics, BITS, Pilani. **Ph.D**, Electronics, Mangalore University
Work Experience	
ISRO Satellite Centre, Bangalore	June 1977 to Jan 1983
Siltronics India Pvt Ltd	Jan 1983 to Mar.1984
Central Electronics Engineering Research Institute	Mar. 1984 to May 1999
TECH Semiconductor, Singapore	June 1999 to August 2005
Tessolve Semiconductor Pvt Ltd	August 2005 to Dec. 2011
Central Manufacturing Technology Institute	Feb 2012 to August 2014
Jain University	Sept 2014 to till date
Area of specialization	
Failure and reliability analysis of semiconductor devices, Semiconductor device fabrication technologies, VLSI Circuit Edit Technologies, Micro / Nano structure fabrication and characterization	
Books authored	
Gateway for mathematical Physics	Himalaya Publishing House, India
VLSI Circuit Edit Technology	LAMBERT Academic Publishing, Germany

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A

RELIABILITY AND QUALITY ASSURANCE OF EEE COMPONENTS FOR SPACE APPLICATIONS

Study of electrical deviation observed in thruster driver hybrid microcircuit

Sujata Kulkarni, Vaishnavi S, Shilpa K R Reddy, M P James, V Venkatesh, M Ravindra
Reliability & Quality Area, Parts Materials & Process Group
ISRO Satellite Centre

Abstract— Hybrid Microcircuits (HMCs) are extensively used in Space Applications due to high reliability, reduced size, weight and volume. High reliability is achieved due to fewer interconnections, fewer intermetallic interfaces. Batch processing of thick film conductors, resistors and dielectrics further improve the HMC reliability and result in consistent HMC performance. Realization of critical circuits is possible as thick film resistors can be trimmed statistically or dynamically to achieve precise values with close tracking. HMCs form an essential part of all spacecraft subsystems including Power Systems, Control Systems, Inertial Reference Unit, Digital Systems, Communication Systems, Sensor Electronics.

This paper discusses the electrical deviations observed in Thruster Driver HMC meant for usage by Control Electronics subsystem for thruster operation at bus voltage of +70Volts. This HMC is qualified for space applications as per ISRO Standard-ISRO PAS 206 "Qualification requirements for Thick Film Hybrid Microcircuits".

During qualification, electrical deviations were observed in the HMC output which is measured across thick film resistors present in the HMC. These thick film resistors experience voltage up to +70Volts. This paper focuses on detailed analysis carried out to understand these observations. Corrective measures employed and improvements made in the resistor design and subsequent qualification methodologies are also brought out in this paper.

Index Terms: Hybrid Microcircuits, Thruster Driver, Thick Film Resistors, Voltage Coefficient of Resistance, Layout Modification

I. INTRODUCTION

Hybrid Microcircuits are circuits in which chip devices of various functions are electrically interconnected on an insulating substrate on which conductors & resistors have previously been deposited. Conductor and resistors are deposited using thick film printing process. Thick film resistors provide advantages as close tracking, improved stability and can be trimmed to achieve precise values. Batch processing reduces additional processing steps as that required for chip resistors. A thick film resistor should be designed considering various factors as power dissipation, stability, aspect ratio etc. Stability of the resistor value is mainly quantified with respect to variation in temperature called as Temperature Coefficient of Resistance and with

Voltage called as Voltage Coefficient of Resistance. Aspect ratio of a resistor is the ratio of resistor length to resistor width.

Thruster Driver HMC (Part Number 116TD) consisting of thick film printed resistors is used for thruster operation at +70Volts raw bus line. Typical HMC internal diagram is as per Figure1.

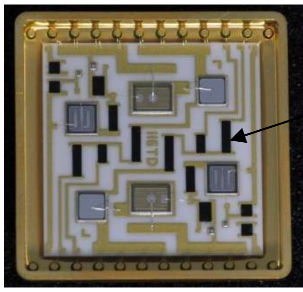


Fig 1: Thruster Driver HMC 116TD

Another thruster driver HMC (113TD) is qualified earlier for thruster flow valve operation at +42Volts. This HMC uses chip resistors across output terminals of the HMC as against thick film resistors used by HMC 116TD. This is the first time in HMC 116TD wherein thick film resistors are used at high voltage of +70Volts. So far thick film resistors have been used at +42V in numerous other space qualified HMCs.

The thick film resistors used in this HMC meet the Temperature Coefficient of Resistance (TCR) equal to 100 ppm(parts per million) per degree centigrade.

II. HMC QUALIFICATION PHILOSOPHY

This HMC is fabricated on a certified and qualified line as per standard ISRO PAS 206 "Qualification requirements for Thick Film Hybrid Microcircuits".

This HMC successfully completed layout verification, derating analysis and electrical performance verification at temperature extremes.

The typical tests this HMC has experienced during screening/circuit type qualification include Stabilization Bake, Temperature Cycling, Particle Impact Noise Detection, Constant Acceleration, Burn-in, Active Temperature Cycling, Electrical Verification, Seal leak tests; Endurance Tests including Operating Life test and High Temperature Storage test. Output monitor voltage electrical deviations observed during endurance tests of this HMC are discussed in this paper.

The root cause of deviation, corrective measures taken and improvements made in the HMC design are also briefed upon.

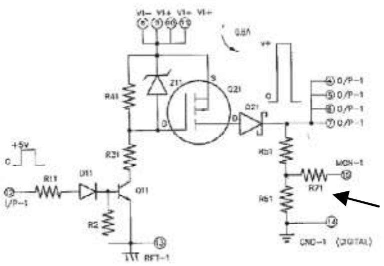
III. HMC DESIGN & ELECTRICAL TEST PROCEDURE

This HMC consists of two sections each incorporating MOSFET (Metal Oxide Field Effect Transistor) acting as a switch. This MOSFET is driven by NPN transistor which in turn is controlled by the HMC input. Output of the HMC is available across thick film resistors of value 470 kΩ and 45 kΩ connected in series to the MOSFET drain/ HMC output terminal**.** This resistor is derived from a paste with standard sheet resistivity of 100 kΩ. Trimming process is carried out to achieve precise value of 470 kΩ with a tolerance of +/- 1%.

As part of electrical performance verification at ambient, HMC supply current, output voltage, monitor voltage and drop across HMC MOSFET are measured for both direct current mode and pulse mode. During operating life test, rawbus voltage of +70V is applied across the HMC supply terminals and with drive input of +5V pulse. HMC operates at a temperature of 125˚C for 2000hours and performance is checked at ambient every 500hours for all the parameters listed above. During high temperature storage test, HMC is stored at 125˚C for 2000hours in passive condition i.e. without bias and performance is checked at ambient every 500hours for all the parameters.

IV. DEVIATION AND ANALYSIS

During Operating life test and high temperature storage test, this HMC revealed increase in the monitor voltage value. The observed value was 6.6V against the specification limit of 6.0 to 6.2V. Monitor voltage is measured across resistor divider network of the HMC consisting of thick film resistors of value 470kΩ and 45kΩ with a resistor of 22kΩ in series. Figure 2 indicates the HMC schematic and resistor divider network.



Resistor Divider

Figure 2: HMC Schematic

To know the cause of voltage drop, value of resistors connected across output were measured with $6^{1/2}$ digital multimeter. Value of one of the resistors was found to be degraded to 430kΩ against the required value of 470kΩ.

Following probable causes were analyzed to understand the root cause of deviation:

- Elemental composition verification

Energy Dispersive X-Ray Analysis (EDAX) conducted on the good and degraded resistor revealed similar elemental composition.

- Resistor lot related defect

470 kΩ resistor is fabricated using resistor paste with a sheet resistivity of 100K. Lot details of this resistor paste were studied and it was found that this paste is successfully used in fabrication of other HMCs.

- Inadequate process parameters

Process parameters for resistor printing and trimming processes were verified with approved Process Identification Document and were found satisfactory.

- Resistor design verification

Verification of resistor design was carried out with respect to maximum voltage rating/power dissipation in reference to application level voltage/power stresses. No issues were observed.

- Contamination

EDAX, Scanning Electron Microscope analysis did not reveal presence of any contaminants/corrosive elements on the degraded resistor.

- Study of similar issues in other HMCs with higher value resistors

Failure histories of high value resistor values used in other HMCs were studied and no issues are reported.

- Tests carried out as part of analysis:
  - Measurement of surface roughness and thickness of good and degraded resistor revealed no differences.
  - The temperature coefficient of resistance is expressed as the ratio of the resistance change to the temperature rise. TCR measurements were carried out on HMCs from this batch a) Pre and post temperature cycling (-55°C to +125°C) b) Pre and Post high temperature storage test. All values were found to be within 100ppm/˚C.
  - Power conditioning test with test condition as +70Volts for 1000 hours at 70°C was conducted on samples fabricated with 470kΩ resistors. All values were observed to be within 470kΩ ± 1% after 1000 hours.

- Literature study

Various literatures were referred to understand the root cause. Summary is as below:

- Resistors undergo temperature variations not only due to changes in ambient temperature, but also due to dissipation of electrical energy when current is passed through them. The resistance of a resistor can change due to a change in the voltage applied to it, even though the temperature may be held constant. This is called as Voltage Coefficient of Resistance (VCR) which characterizes the resistance change with an increase in applied voltage.
- As the voltage across thick film resistor (which consists of conductive material suspended in an insulating matrix) is increased, new conducting paths are opened resulting in drop in resistance. Glassy networks present in the paste temporarily break down and this decrease in insulation causes decrease in resistor value.
- Further, following factors influence VCR
  a. Ink resistivity – Lesser is the resistivity, lower is the VCR.
  b. Termination material – This must be correctly matched with resistor ink.

c. Layout and size – Increasing the resistor length reduces voltage per unit length.
d. Trimming geometry – Hot spots can be produced based on trim geometry.
   - Narrow trim – voltage sensitivity is high
   - Wide trim – voltage sensitivity is reduced
   - Top hat trim – voltage sensitivity is minimised
- Figure 3 shows VCR dependence on ink resistivity & termination material combination Figure 4 shows VCR dependence on resistor geometry. Figure 5 shows VCR dependence on resistor length. Figure 6 shows VCR dependency on trim geometry

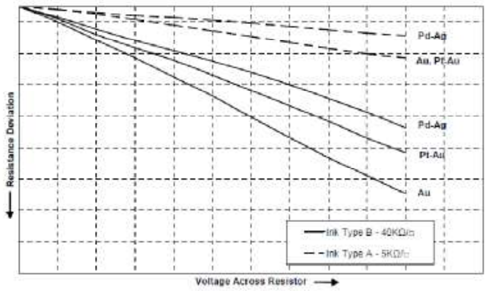


Figure 3: VCR dependence on ink resistivity & termination material combination

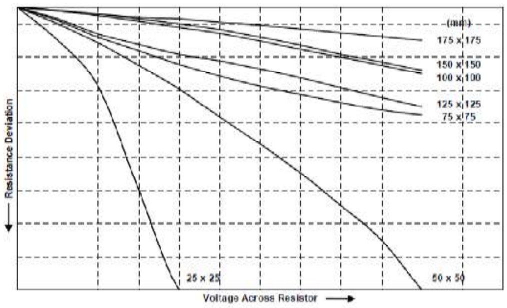


Figure 4: VCR dependence on resistor geometry.

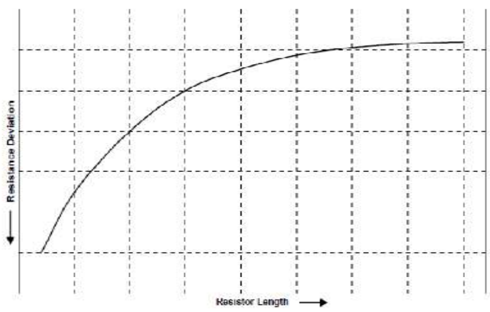


Figure 5: VCR dependence on resistor length

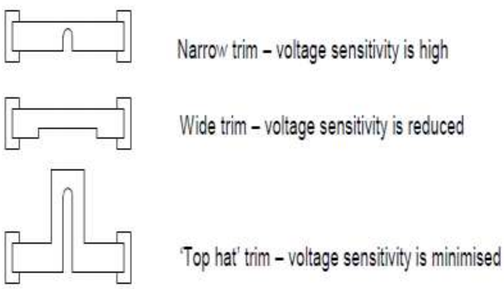


Figure 6: VCR dependence on trim geometry

Based on above points, following inferences are drawn from literature:

- Resistors with higher aspect ratio (greater length) are more sensitive to VCR.
- Only few volts can be enough to produce considerable resistance changes both temporary and permanent.
- Effect of voltage can be significant with any combination of high ohms per square compositions, small resistors and voltages over few volts.In order to minimize this effect it is essential that correct component design and material selection are employed.

This HMC employs ink resistivity of 100kΩ to achieve 470kΩ resistance value via trimming process. This resistor has a higher aspect ratio of 3.8:1 with narrow trim. Termination material with the resistor ink is qualified and no issues are observed so far. Hence, based on the analysis, tests conducted and literature study, it is inferred that the change in thick film resistor value is due to change in VCR at high voltages due to high aspect ratio (more length) of the resistor.

V. CORRECTIVE ACTIONS AND IMPROVEMENTS

The batch with electrical deviation was rejected. As an improvement, it was recommended to change the HMC design by incorporating two thick film series resistors of suitable value and lower aspect ratio against single resistor of value 470kΩ to reduce the effect of variation in resistor value at high voltages.

VI. REQUALIFICATION OF NEW DESIGN

Two series resistors of value 250kΩ and 200kΩ, each with aspect ratio of 2:1 were incorporated in the layout against single resistor of value 470kΩ having an aspect ratio of 3.8:1.

Derating analysis, layout verification were repeated and these met the requirements with change in the resistor design.

Protos were successfully evaluated, screening qualification tests including endurance tests as life test and high temperature storage test were successfully completed after resistor design change.

VII. CONCLUSION

Based on the analysis, tests conducted and literature study, it is inferred that the change in thick film resistor value is due to change in VCR at high voltages due to high aspect ratio (more length) of the resistor resulting in electrical deviation in the HMC.

No such issues are observed in thick film resistors used at lower voltages with value 470kΩ and aspect ratio of 3.8:1.

This HMC successfully underwent qualification with resistor design change having lower aspect ratio. This HMC is cleared for flight applications.

ACKNOWLEDGMENT

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Reliability Aspects of Electronic Components used in Launch Vehicles

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Abstract: This presentation briefly explains the basic understanding about the R &QA of EEE components and the practices followed, touching their importance for launch vehicle application. Each launch vehicle uses about 20,000 active parts and 60,000 passive parts. Most of the components are very critical for mission success. Failure of any one of these components may cause mission failure. The service condition includes Shock, Temperature and Vibration. VSSC has adopted certain R&QA practices for EEE components which has undoubtedly contributed to a great extent in realizing successive successful missions.

The components range from very complex micro controllers , micro processors, FPGAS, ASICs, memories, data acquisition parts such as ADCs, DACs, linear and digital ICs, HMCs, relays, converters, RF and microwave parts and passive parts. Details are provided on the criteria for selection of parts and the necessity for qualification. Based on the technology, the policy followed for each category and the methodology of acceptance is elaborated. Special mention is made on the verification of VHDL and Verilog designs and the test vector generation for the new designs of FPGAs and ASICs.

Also the problems/issues faced and their resolution are briefly touched upon

I. .INTRODUCTION:

All electronic packages used in launch vehicle consist of electronic parts that range from very complex microcontrollers, microprocessors, fpgas, memory devices, HMCs, linear and digital devices, RF and microwave parts, discrete parts such as mosfets, transistors, diodes, relays, to passive parts such as resistors, capacitors and inductors. VSSC has established a state-of-the art QA system, to evaluate and certify these parts for flight application.

In any avionic package, large number of electronic parts are used; the failure of one component may result in the total failure of the system.

The electronic parts, used in non-repairable systems like launch vehicles, satellites, aircraft etc should have a very low failure rate to ensure a very high degree of reliability for these systems.

The parts used in these systems may experience various thermal and mechanical stresses like temperature, humidity, vibration, shock etc. and are expected to perform for long duration without failure.

The result of a failure in these systems is very costly. For building such systems only high reliability components are to be used.

II. Life cycle of electronic components:

The life cycle of most electronic components shows 3 distinct phases with respect to their failure rate. These are the early life period, useful life period and wear-out period. Because of the characteristic shape of this curve, this is commonly known as the “Bathtub Curve”. As seen from the graph, the curve shows an increased failure rate initially, a predictable constant failure rate in the useful life period and again an increasing failure rate towards end of life.

The region where the failure rate is high initially is named the Infant Mortality period or the Early failure period, the predictable constant failure rate region is named the Useful Life period or the Random failure period, and the increasing failure rate region is called the Wear Out period or the End of life failure period.

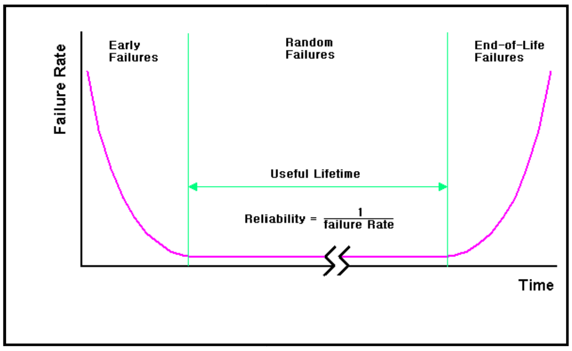

Figure.1 Bath Tub Curve

Table below shows the various causes of failure by failure period.

Failure period	Most common causes of failure
Early failure period	Defective design. Defective manufacturing. Defective material Unsuitable for environment
Random failure period	Extraneous surge Misuse Fluctuation in environmental conditions
Wear-out failure period	Corrosion Oxidation Fatigue Performance degradation

Table.1 Failure Periods

III. REQUIREMENT FOR SCREENING:

Screening is the process by which defective devices; both quality defects and latent defects are removed from a population of components. The objective of screening is to identify and remove devices having inferior quality

It should be clear that a product should be put to use after it has passed the infant mortality period, in order to reduce the number of field failures.

Bringing a part population out of this infant mortality period can be done by:

1. Aging the system for that period (this can be several months)
2. Aging the system under stress which accelerates the aging process

An important stress condition is increased temperature. The accelerating effect of temperature follows Arrhenius' equation

$$\lambda_{T_2} = \lambda_{T_1} * e^{(E_a(1/T_1 - 1/T_2)/k)}$$

- T_1 and T_2 are absolute temperatures (in Kelvin, K)
- λ_{T1} and λ_{T2} are the failure rates at T_1 and T_2, respectively
- E_a is the activation energy; constant expressed in electron-volts, eV
- k is Boltzmann's constant $k = 8.617*10^{-5}$ eV/K

The equation shows that the failure rate is exponentially dependent on the temperature. Thus, the ageing or burn in mechanism is used to screen out the weaker parts from a lot. The remnant surviving parts are thus stronger in terms of reliability and give a long almost failure free life.

Devices can also fail due to the environment to which they are exposed. According to a report brought out by Hughes Aircraft Co. (USA), about 60% of all environment induced failures have been attributed to incidental temperature and humidity.

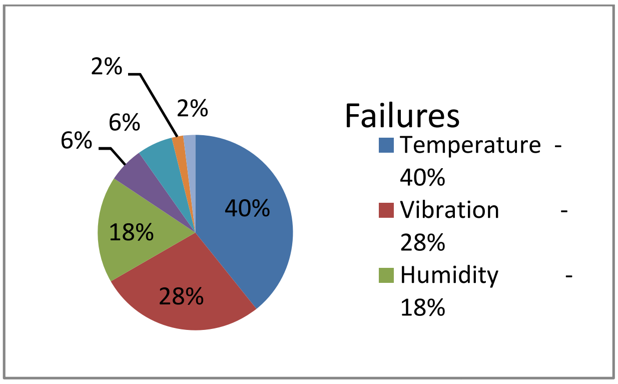

Figure.2 Percentage of Failure Occurrence

IV. SCREENING PROCEDURE:

Failures are brought out by subjecting to a screening process consisting of a series of electrical, mechanical and environmental stress tests. A typical screening procedure for a device may consist of tests like the following.

a) Visual inspection:
Observation of the devices under magnification.

b) Stabilisation bake :
To determine the effect on microelectronic devices of storage at elevated temperatures without electrical stress applied. Settles freely moving ionic content of an electronic part.

c) Temperature cycling/ Thermal shock:
To determine the resistance of the part to sudden exposure to extreme changes in temperature and its effect. Brings out failures due to difference in temperature coefficient of different materials used in the manufacture of an IC.

d) Centrifuge test/ Constant acceleration test:
Determines the effect of structural and mechanical weakness. It helps in determining the mechanical limits of the package of the device, internal metallization, die or substrate attachment and other elements of the device.

e) Leak tests:
Checks the effectiveness of sealing and hermiticity of cavity devices which protects the device against moisture and other contaminants. It consists of a fine leak followed by a gross leak test.

f) Burn-in test:
Eliminates marginal devices, those with inherent defects or defects resulting from manufacturing weaknesses which cause time and stress dependant failures.
Burn-in profiles are chosen to verify the capability of the device to perform under load and eliminate infant or latent failures. The electrical parameters are verified to be within permissible limits after the burn-in.

g) Final visual examination:
Observation under magnification.

The MIL standards provide detailed information regarding screening and qualification of electronic parts for high reliability applications like launch vehicles and satellites. Some of the standards relevant to VSSC are:

MIL-STD-883	Test methods and Procedures for Microelectronics
MIL-STD-750	Test methods for Semiconductor Devices
MIL-STD-202	Test methods for Electronic & Electrical Components Parts

MIL-S-19500	General Specification for Semiconductor devices
MIL-PRF-38534	General Specification for Performance of Hybrid microcircuits
MIL-PRF-38535	General requirements for integrated circuits (microcircuits) manufacturing

V. SCREENING PRACTICES FOLLOWED AT VSSC:

All parts are subjected to Screening as per the approved screening plan generated for individual parts. In some cases sample screening philosophy is followed based on the type of parts.

1) Mil-883 microcircuits
- Sample screening

2) Industrial grade microcircuits
- For telemetry packages such as ICU, DPU, Power modules, telecommand, tracking and SBT, the industrial grade active parts are fully screened.
- For all other telemetry packages, the industrial grade active parts are screened on sample basis and 100% SRC tested.

3) HMCs,Diodes, Transistors
- Full screening

4) Electro-mechanical relays
- 100 % electrical at SRC (Source screened with serialized test data)

5) Resistors
- Sample screening
- Carbon-composition & wire-wound type are fully screened.

6) Capacitors
- Full Screening.
- Sample screening for ceramic CCR, CKR and CDR capacitors.

7) Inductors
- Full screening

8) Other passive
- Sensistors, thermistors, heater kits, trimpots: Full screening

Sample screening includes: Full screening tests for 5% or 5 numbers (50 numbers for passive parts) whichever is larger from each date code and each procurement lot. 100% Functional test and parametric measurements. In case of failures in the samples, full screening to be carried out on the full batch.

VI. SCREENING VALIDITY PERIOD

The following gives the screening validity period :.

Resistors:
- Total life validity: 15 years (based on Datecode) till issue of components from Stores.
- Another 5 years in the Subsystems.
- Screening Validity period: 10 years after 1st screening.
- Rescreening test: 100% of devices Visual inspection and Parameter measurement.
- Storage: Controlled environment.

All other active and passive devices:
- Total Life validity: 15 years (based on Datecode) till issue of components from Stores.
- Another 5 years in the Subsystem.
- Screening Validity period: 3 ½ years .
- Rescreening tests: 100% of devices Visual inspection and Parameter measurement. From 7 years after 1st screening, Hermetically leak test is also carried out for Active parts.
- During certification, test report and certification slip mentions the date upto which the screening certification is valid or the component usage is valid.
- For Wires, cables, connectors, enameled wires, QC checking is carried out before card wiring. The shelf life for these passive parts are also 15 years from the date of manufacture.

VII. STANDARDIZED LISTING:

VSSC is maintaining a PPL (Preferred Parts List), which is an approved list of parts for usage in Launch vehicle system. The criteria for listing the parts in PPL are as below:

1. Hi-Rel spec. (MIL-883, MIL-38534, MIL-38535, MIL-19500 JTXV, Established reliability level etc.)
2. Available from multiple sources.
3. Ability to meet the environmental levels of our launches
4. Previous usage history
   - There must be sufficient usage experience either in house or elsewhere in hi-rel applications to provide reasonable confidence that the part will perform reliably meeting the launch vehicle requirements.
5. In the case of non-standard parts, satisfactory completion of qualification tests.

Three levels of quality are given in the PPL.
Part A: Qualified as per MIL/ESA-SCC/ISRO (Hi-Rel MIL specifications) and are available as standard parts from manufacturers.
Part B: Not qualified to the Hi-Rel MIL specifications but are included in the PPL based on experience in usage and qualification/screening tests conducted by VSSC and can be used for critical as well as non critical applications.
Part C: Not qualified to Hi-Rel MIL specifications but are included in the PPL based on experience in usage and qualification/screening tests conducted by VSSC. These parts are recommended only for Non-critical applications.

VIII. COMPONENT SELECTION:

Guidelines in component selection for assuring reliability of an avionic package :

1) Quality level of the Devices:

Only Mil-grade devices are used in mission critical NGC, Tracking and Tele-command on- board systems. Micro circuits are of Mil-883 Class B or QML class Q or equivalent. Discrete devices such as Transistors & Diodes are Mil-19500 JANTX/ JANTXV or equivalent.

If MIL-grade devices are not available, Mil equivalent devices from reputed manufacturers are made use of, after recommended qualification tests.

Only in very rare cases, where available Mil grade or equivalent devices are not adequate to realize the required function, usage of industrial grade devices, after qualification, are considered in these systems.

In Telemetry systems, industrial grade active parts are also used after qualification. Passive parts used are all of Mil-grade ER Type only, except in very rare cases of non-availability.

2) Technological Maturity

The production of the devices must have been in operation for a period sufficient to provide assurance that the design and process parameters have been identified and adequate controls have been developed. Also the technology must have demonstrated suitability for high reliability applications.

3) Component Derating

When components are selected, derating shall be taken into account. Mission specific stresses, such as temperature, radiation, etc., shall be reviewed as a means of assessing whether to apply additional derating.

4) Constructional Analysis

Constructional analysis is carried out on representative components. The primary aim of constructional analysis is to provide an early indication of a component's probability of meeting the evaluation requirements

5) Alert System

Batch failures are discussed in a Quality Management Board for Avionic parts and recommendations made. If the recommendation of the Board is to ban a specific lot, a type etc., the recommendation is immediately circulated.

IX. ADDITIONAL SCREENING PRACTICES FOR HIGH END DEVICES

a) Evaluation of Microcontrollers, Microprocessors :

The whole architecture is divided into functional blocks like ALU, memories, peripherals, timers, special interfaces if any. Test cases are written to cover the different functional blocks. Functional and parametric testing are carried out on the devices using VLSI tester.

b) Evaluation of Memories:

Standard patterns like March pattern, checker board pattern, address decoder test are developed for testing of memories. Additionally, software data protection algorithm tests are carried out for EEPROMs. Functional and parametric testing are carried out on the devices using VLSI tester. MIL 883B screening flow is followed for evaluating the data retention of the devices.

c) Systematic Evaluation of FPGAs:

Actels' One time programmable (OTP) devices are used in flight applications. Unlike other devices, FPGAs are fused with the application code and subjected to screening. The application code is designed using Hardware Description Languages (HDL) like VHDL and Verilog. The following processes are carried out as part of screening of FPGAs.

i. Verification and Validation

Verification of the FPGA design is carried out to bring out bugs in the code. This is to confirm the conformance of the code to the application requirements. Verification of FPGAs and ASICs are carried out for all HDL (Hardware Description Language) designs. Activities carried out for the above includes:

- **Functional verification:** by exhaustive RTL functional simulation to ensure that the design (VHDL or Verilog) is working as per the requirements by developing test benches to cover all input scenarios and possible error conditions and corner cases. Verification is coverage driven. The test bench is evaluated using code coverage matrices. The test bench is augmented till 100% of statement, branch, condition and FSM coverage are achieved; and more than 95% of toggle coverage is achieved.
- **Assertion based verification:** to validate the behaviour of the design by giving expected sequence of events, condition checks.
- **Independent code walkthrough:** to find whether the designs adhere to design /coding guidelines of ISRO for ASIC/FPGA
- **Independent QA Analysis of reports:** such as linting report on the HDL code, Static Timing Analysis (STA) results, timing constraint files, pre layout and post layout simulation results.

After successful completion of verification, the design is approved for programming.

ii. Configuration control

The approved code is configuration controlled. QA/Screening agency has to ensure that only the configuration controlled files are fused.

iii. Programming of FPGA

Fuse Files for programming shall be taken from the Configuration controlled files only. Fused FPGA shall be marked with design name and checksum with pencil. Programming is done in the presence of QA/Screening agency to ensure fusing of the correct file. QA/Screening agency ensures that the programmer used is calibrated. The calibration of the programmer is carried out by QA and a validity period is provided.

iv. Test vector generation

Test benches are written to cover all functional aspects as well as all corner cases. Code coverage analysis with respect to statement, branch, toggle, FSM (Finite state machine) are performed on the generated test vectors. The FPGAs/ASICs are then evaluated using these Test Vectors on a VLSI tester.

v. Electrical parameters

Functional and parametric testing like leakage, operating, standby currents, output low and high levels etc carried out on the devices using VLSI tester.

X. COUNTERFEIT BATCHES BROUGHT OUT:

Several batch failures were brought out during screening. A few cases are mentioned below:

i. AD704TQ opamp

The batch had a large number of electrical rejections. DPA (Destructive Physical Analysis) on samples revealed a different die compared to the die of a good batch

ii LT1086 regulator

The failed batch revealed a different die with the part numbering and date code being identical.

iii HI-506A8 multiplexer

There was a mixup of devices with input protection feature incorporated and without input protection feature in a single date code.

iv LM118H/883

Electrical parameters' deviations on 192 numbers and 8 catastrophic failures. Observed two different die configurations belonging to same date code.

v AD704AR Quad opamp

Two batches having same part number marking on the top of the devices. DPA revealed that DC:0735 has a single die but DC:0812 (counterfeit batch) has dual die of another manufacturer..

Precautions Incorporated:

i. Devices are procured only from the manufacturer specified authorized agent.
ii. Certificate of Conformance is mandatory.
iii. Top marking is verified with a marking ink.
iv. Sample device from every date code is decapped, and DPA (Destructive Physical Analysis) is carried out to verify for any die mismatch, internal corrosion etc.
v. Only after all the above are confirmed, the RV of the Purchase file is cleared.
vi. This has reduced the procurement of fake components to a large extent.

XI. COMPONENT FAILURES AT NASA

A study was made on failures observed at NASA. Some batch failures were brought out by NASA during the screening stage of batches. A few cases are mentioned below:

i. OP249 opamp

OP249 is a High speed opamp from Analog devices. The batch contained die for a voltage reference from PMI.

ii. DS14C232ES/883 Dual Driver Receiver

DS14C232ES/883 is a low power +5 Dual Driver Receiver from Texas Instruments. The part number indicates a CLCC package, but this package is a CDIP.

iii. CY7C1371B SRAM

CY7C1371B is a SRAM from Cypress Semiconductor. The device was fake and it was identified by external visual inspection. The documentation received with these parts did not include Certificate Of Conformance from either the previous distributors or the original manufacturer

iv. MD87C51 8-bit microcontroller

MD87C51 is a 8-bit microcontroller from Philips. The external marking was of Philips. But internal die was found to be of Intel.

NASA is additionally doing C-SAM (C-mode Scanning Acoustic Microscopy) and SEM (Scanning Electron Microscope) with 250 times magnification as light microscopy which will uncover defects such as delaminations, voids, damaged or displaced die, mixed die sizes and shapes, internal wires and bond pad defects etc. as part of initial screening

XII. CONCLUSION

a) The screening program consists of a series of electrical and environmental stresses; the weak devices are removed from the lot by subjecting each device to a failure detection test such as visual inspection, environmental tests, hermetic tests,

electrical measurements etc. This will detect unacceptable devices detected without degrading the quality of good devices.

b) The system explained in this paper is currently being followed for all launch vehicle programmes. As per statistics assessed every year, field failures after usage of screened components are mostly only application related failures or random failures.

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MMIC Device Reliability, Qualification Methodologies and Packaging Techniques for Satellite Applications

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Abstract: This paper compares various device technologies in MMIC fabrication in terms of material, application, power and frequency limitations. Common failure modes and associated failure mechanisms required to be understood for better reliability are described. Standard qualification test philosophy followed by MMIC manufacturers is also described. Reliability issues arising due to packaging the MMIC dice and solutions to such packaging effects are suggested in the paper.

Key words: MMIC, MESFET, HEMT, GaN, Space Qualification, Packaging

I. INTRODUCTION:

Microwave modules developed using packaged active devices and discrete passive components assembled on a dielectric substrate are standard products used in Satellite applications for a long time. With increasing demand of wider frequency-bandwidth performance, size & weight reduction in Satellites, focus is shifted to use Monolithic Microwave Integrated Circuits (MMICs). MMICs use semi insulating GaAs as substrate material as compared to Silicon in conventional devices. Thorough understanding of the failure mechanisms associated with various MMIC device technologies is required to ensure reliability of these components which is need of the hour to ensure satisfactory operation of Satellites over intended mission life. MMICs are packaged to meet electrical, thermal and environmental specifications of a Satellite subsystem. Various packaging techniques like chip scale, metallic and ceramic packaging technologies are adapted considering the application on hand. Packaging is expected not to reduce the reliability of bare die. Effects of Hydrogen, CTE mismatch and power dissipation of MMIC dice form major challenges.

II. MMIC DEVICE TECHNOLOGIES:

MMIC technology utilizes transistor as a basic element along with on-chip passive components to achieve complex circuit function. Various options exist in terms of materials, processes to obtain better performance in terms of low noise, power and high frequency applications. Following sections describe various device technologies available in MMIC process.

a) Metal–Semiconductor Field-Effect Transistors (MESFETs):

GaAs metal–semiconductor field-effect transistors (MESFETs) are most commonly used active devices in microwave circuits. GaAs MESFET structure is shown in Fig. 1. Buffer layer is epitaxially grown over the semi-insulating GaAs substrate. Buffer layer prevents the defects in substrate from propagating to other layers. Lightly doped n-type conducting channel layer is epitaxial grown over buffer layer. Highly doped n+ layer grown on the surface helps in the fabrication of low-resistance source/drain ohmic contacts of the transistor. Highly doped n+ layer is etched in the channel region and a Schottky gate contact is made using Ti–Pt–Au layers. Even though GaAs MESFET is the most mature technology, it is not particularly suited for low noise, high power and millimeter wave frequency applications. Random variations in carrier speed in the device channel leads to noise. Electron mobility in the doped MESFET channel is limited by ionized impurity scattering. Also Limited bias-range available in MESFET is another constraint to achieve minimum noise figure and maximum gain. High frequency and high power applications demand smaller gate length and channel thickness. Smaller channel thickness imposes doping concentration to be higher in order to maintain the I_{ds} performance. Smaller breakdown voltage and power are the result of high doping concentration. Despite of these limitations, reasonable Noise figure, power and high frequency operation characteristics are achieved with GaAs MESFET devices.

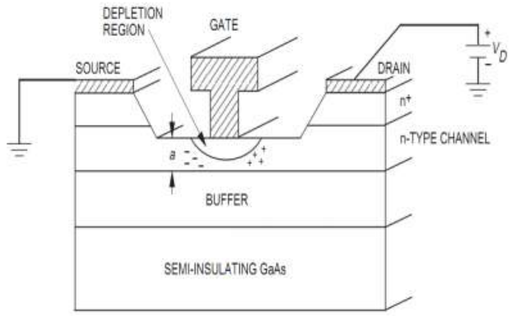

Fig.1 MESFET Structure (Reference 1)

b) High-Electron Mobility Transistors (HEMTs):

The principle difference between the MESFET and HEMT is epitaxial layer structure. Heterojunction formed in HEMT devices separate the moving carriers from their parent impurities to achieve high mobility. As shown in Fig.2, higher band gap of the AlGaAs compared to GaAS results in diffusion of electrons from donor n^+ AlGaAs layer to undoped GaAs layer. Electrons diffused to undoped GaAs layer are confined by a potential barrier in the conduction band and a thin sheet of two dimensional electron gas (2DEG) is formed. 2DEG enjoys higher mobility and having superior conduction properties. Another variant of HEMT

structure is pseudomorphic HEMT which uses InGaAs as undoped channel due to its superior electron transport, improved carrier confinement, sheet charge density and transconductance properties. InP-based HEMT devices provide low noise high frequency solutions. GaAs PHEMT devices offer high power and high frequency operation due to high sheet charge density and high current density. However, GaN based devices are increasingly used in high power applications in place of PHEMTs.

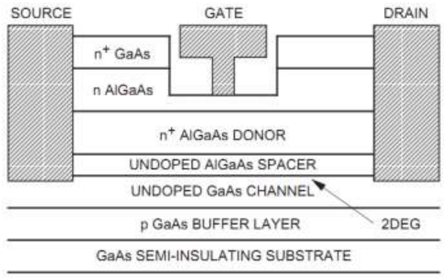

Fig.2 HEMT structure Epitaxial Layers (Reference 1)

c) Heterojunction Bipolar Transistors (HBTs):

HBT is a modified bipolar transistor used in microwave high power applications. In HBT, emitter and base are made with semiconductor materials with different band gap. Emitter is a wide band gap material, while base is a low band gap material. Heterojunction at the emitter-base prevents the hole injection from base to emitter while facilitating electron injection from emitter to base. A higher carrier injection efficiency is still feasible in HBT even with high base doping and light emitter doping due heterojunction. Base spreading resistance and emitter-base capacitance is minimum in HBT compared to its silicon counterpart. HBT device structure is shown in Fig.3. HBT find their application in microwave power amplifier, oscillators and mixer applications.

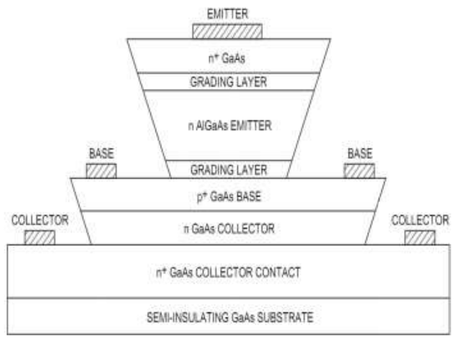

Fig. 3 HBT Structure (Reference 1)

d) GaN based devices:

GaN is a new technology compared to Si and GaAs, and is the most preferred choice for High power application. GaN has a band gap of 3.4 eV which is more compared to Si(1.1 eV) and GaAs (1.4 eV). Because of large band gap, GaN material has large breakdown voltage and operates at higher voltages. Higher saturation velocity and charge capacity of the GaN material gives best current density performance. GaN FET devices give maximum saturated current, Output power and high temperature performance. GaN family devices are the best choices for high frequency power application in Satellite sub- systems.

III. MMIC FAILURE MODES & MECHANISMS:

MMIC device failures are observed through degradation in parameters of the device like I_{DSS}, Gain and Power Output etc. Each failure mode has an associate failure mechanism through which the device can fail. Life tests reveal type of degradation to which the Particular MMIC technology is most susceptible. Common failure mechanisms in GaAs based MESFET, HEMT & HBT devices is described in the following sections. Failures arising due to hydrogen contamination, CTE mismatch and moisture are described in section on MMIC packaging.

a) Failures in MESFET:

Diffusion of the Schottky gate metal into the channel reduces the active channel thickness and results in decrease in I_{DSS} and reverse breakdown voltage. This phenomenon is termed as “Gate-Metal Sinking”. Industry standard gate structure consists of Au/Pt/Ti or Au/Pd/Ti metal layers. Gold gets diffused through barrier Pt/Pd metal grain boundaries at elevated temperatures and degrades the device performance. Ohmic contact degradation at the drain and source contacts is due to diffusion of contact Au metal into GaAs and Ga diffusion into Au metal contact. Increase in contact resistance is severe at temperatures above 150 °C. Diffusion of dopant atoms from channel and diffusion of impurities from the substrate to the channel reduces the carrier concentration. The increase in surface state density at passivation layer and GaAs interface causes change in depletion region and a change in the breakdown voltage. Another commonly seen failure mechanism in power MESFET devices is electromigration. Electromigration is the movement of metal atoms along metallic strip due to momentum transfer from electrons. Threshold current density for electromigration is greter than 2x 10^5 A/cm^2. Electromigration causes catastrophic failure due to shorting of gate to source/drain. Hot electrons are generated in power transistors operating under heavy gain compression. Electrons generated at the drain end get sufficient energy from high electric field and get trapped in the Si_3N_4 passivation layer forming permanent traps. These trapped electrons in Si_3N_4 passivation layer change the FETs drain current, transconductance, knee voltage and breakdown voltage. An output power drop of 1 dB over 1,000 hours of RF operation, commonly known as “Power-slump”, is the degradation due to hot electrons.

b) Failure in HEMT:

HEMT devices also suffer from the metal diffusion related failure mechanism at high temperatures. In HEMT devices lateral diffusion of Al into the gate recess region and Gold diffusion from the ohmic contact into channel changes the conduction band discontinuity and consequently the

confinement of the channel electrons. AlGaAs/GaAs heterostructure related failure mechanisms decrease electron concentration in the channel due to deconfinement of the 2DEG. Vertical diffusion of Al from the AlGaAs donor layer to undoped GaAs channel layer in HEMTs deteriorates the high electron mobility of the 2DEG. HEMTs and PHEMTs suffer the same reliability concerns as those of MESFET devices like electromigration and hot electron effects. A particular reliability issue with HEMT devices is formation of traps, called DX centers. These traps are deep donor levels that lead to reduced drain current, an increase in low frequency noise and photoconductivity. DX centers are avoided by keeping the Al_xAs content below x = 0.24 for n-type doped $Al_xGa_{1-x}As$.

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c) Failure in HBT:

Failures in HBT based devices occur at high current density operation. Diffusion of crystalline defects from the bulk semiconductor to the heterointerface in abrupt junction HBTs causes increase in base current. Contact of the emitter-base junction edge to the defect-laden implant region causes change in V_{be} and decreases in h_{FE}. Beryllium-doped AlGaAs/GaAs HBTs are more susceptible to V_{be} shift, current-gain decrease, and base and collector current change due to field-aided diffusion of Be atoms from the base into the AlGaAs emitter. C-doped HBTs offer better performance compared to Be-doped HBTs under high-current-density operation. In multifinger Power HBTs observed degradation is sudden decrease of collector current. This phenomenon is called “collector-current collapse”. Non-uniform distribution of current and temperature in the electrode fingers is the cause for this failure. Optimized HBT layout improves the power performance.

IV. STANDARD SPACE QUALIFICATION PHILOSOPHY:

Qualification methodology followed by MMIC manufacturers to assure reliability is addressed in the following sections. Qualification of MMICs for space usage is divided into three main categories namely process qualification, product qualification and product acceptance tests.

a) Process Qualification

Process qualification assures the quality, uniformity and reproducibility of MMICs fabricated in a specific manufacturing process. The first step in the process qualification is selection of suitable family of devices and the technology to be qualified and used in the MMIC fabrication. Subsequently development of various process steps involved in the selected technology like photolithography, active layer formation, passivation and gate metal layer formation etc is critical to ensure reliability and takes most of the resources and time. Process qualification also covers design rules and models of the standard components. Design rules for basic circuit components used in MMICs are minimum resistor size, the maximum capacitance, the minimum air-bridge width, the maximum air-bridge length, the minimum separation between via holes, and the active device geometry etc. Developing a model for standard components helps the designer in adapting them and increases chances of first time design success. Developed processing steps are documented along with practiced workmanship, management, material tracking, and design procedures as a part of process qualification documentation. Technology characterization vehicles (TCV) and Standard evaluation circuits (SEC) are fabricated, packaged and subjected to temperature-accelerated life tests for MMIC design validation and process reliability evaluation as a part of process-qualification. Packaged TCVs and SECs are characterized for thermal, electrical, and reliability to provide lifetime and failure rate of devices fabricated using the process. Technology characterization vehicle (TCV) is a structure fabricated on wafer and used for characterization of failure mechanisms in selected MMIC process Technology. Standard evaluation circuit (SEC) contains MMIC circuit design and electrical characterization performed on SEC to ensure process stability.

b) Product Qualification:

Product qualification is specific to MMIC design and performed each time a new MMIC die is designed & realized. Product qualification deals with understanding the limitations and characteristics of the design. Product qualification establishes the safe operating conditions to achieve desired electrical performance from MMIC design. Initial step in Product qualification is MMIC design verification by measuring die electrical parameters like noise Figure, gain, Power output and return loss etc. Any deviation in these electrical parameters requires redesign of the MMIC die. After achieving satisfactory electrical performance of MMIC die by design iterations, MMIC dice are subjected to product characterization tests. Product characterization includes Thermal Analysis and Characterization, Electrostatic Discharge Sensitivity, Voltage and Temperature Ramp, step stress and High/Low Temperature tests. Thermal analysis indicates hot spots in a MMIC die. Channel region temperature of the MMIC die is critical and establishes the life time of the die. GaAs devices are very sensitive to ESD damage and ESD characterization of MMIC design sensitizes the user in adopting standard clean room practices during handling, packaging, and testing of the MMICs. Temperature Ramp and Step Stress indicate the portion of the MMIC die sensitive to high temperature operation and give life test temperature values. Absolute maximum voltage ratings are determined during the voltage ramp test. High/Low Temperature Tests determine the percentage change in the electrical parameters and temperature limits.

c) Product Acceptance:

Product acceptance tests weed out faulty or underperforming devices fabricated on qualified process line resulted due to undetected variations in process and material. Product acceptance is further classified into wafer acceptance, lot acceptance and package device screen tests. The initial level of MMIC die acceptance is carried out in wafer acceptance

testing. Wafer level testing of MMIC die assures the uniformity and reliability of the fabrication process and reduces the production cost by earlier detection of bad wafers and dice, if any. All MMIC dice and Parametric Monitors (PM) in a single wafer are 100% DC & limited RF performance probe tested based on complexity. Parametric Monitors are test structures fabricated on specific locations along with MMIC dice are used for electrical characterization of wafer. Wafer level acceptance test results are used in Yield Analysis. Once the wafer is accepted, lot acceptance test is performed on MMIC dice on a sample basis from wafer lot. Sampled MMIC dice from a wafer lot are mounted in a carrier/package and subjected to burn-in test and also 10 MMIC dice per lot are subjected to steady-state life test of 125°C, 1000 hours at maximum RF stress power. Any failures observed in these tests leads to rejection of full lot. Full characterization of fabricated MMICs is not performed in lot acceptance test due to difficulty of unpackaged die characterization. Most of the MMICs are procured in die form, integrated into packages and used for end application. Reliability of the packaged MMIC dice depends on the selected package and packaging process. Responsibility of ensuring reliability of the end module rests with user and 100% package screen tests to be performed to address this issue. However, if the packaged MMIC die is procured, 100% package screen tests can be performed with manufacturer.

V. PACKAGING OF MMICS:

Packaging of MMICs provides mechanical support, environmental protection, and thermal dissipation path and connects the MMIC to other circuit elements in a system. Package optimizes the size, mass, complexity and ensures the reliability of the components present inside the package. Predominantly used packaging techniques in satellite subsystems are described in following sections.

a) Chip Scale Packages:

The size of the chip scale package is small, in the order of the die size. Chip scale packages have the advantage of ease of handling, assembly and mechanical robustness. Many of MMIC manufacturers supply high power internally matched FET dice in small package form to ease the customer in thermal design and to achieve shorter product design cycle. Varieties of chip scale packages are available in industry. Packaging of the MMIC die in chip scale package reduces the die performance due to multiple RF transitions. However, a good package cavity design with matched RF transitions gives the customer an additional choice of packaging technique to suit one's application.

b) Metallic packages:

Microwave Multichip modules are often made with metallic packages along with passive microwave components and hybrid circuits. Aluminum, CE alloy material are the most preferable choice because of Light weight, high thermal conductivity. Metal package provide good electromagnetic shielding and thermal dissipation. Also isolation walls inside the package reduce coupling between different sections of multichip module. MMIC devices are attached to CTE matched carriers/package base along with ceramic substrates and other passive components. CTE matched carriers eliminate die delamination and cracking problems. The material choice for MMIC chip carrier is CuW/10-90, CuMo/15-85 and CuW/15-90 etc. High thermal conductivity of the carrier and die attach material removes heat from high power MMIC devices and ensures the safe channel temperature. Au-Sn (80-20) and epoxies are the commonly used die attach materials in MMIC packaging. Au-Sn solder offer high thermal and electrical conductivity compared to epoxies and suited for high power dissipating MMIC designs. Epoxies offer lower curing temperatures and absorbs the stress developed due to thermo-mechanical effects to some extent. These assembled carriers are fastened to package base. Package and carrier are plated with Ni and Gold to facilitate soldering, wire/ribbon bonding and feedthru installation purposes. Hermetic RF/DC feedthrus provide required electrical connections to MMIC dice packaged inside the multichip module. Finally the package is sealed with lid to protect MMIC dice from moisture and other environmental contaminants. Hydrogen in hermitically sealed metal packages degrades the device performance by reacting with gate metal structure, where gate is made up of pt/pd metals. Increase in I_{DSS} and V_P, and decrease in g_m are the observed failure modes due to Hydrogen contamination. Main source of hydrogen is package material and plating layers. Use of getter material, thorough baking of the assembled package before the final sealing step, changing MMIC gate structure and using Aluminum Packages are some of the possible solutions to reduce hydrogen contamination effects.

c) Ceramic Packages:

Ceramic packages offer several advantages compared to metallic packages. Light weight, feasibility of mass production, reduced package resonance effects and close spacing of the MMIC dice are some of possible advantages derived from a ceramic package. Low Temperature Co-fired Ceramic (LTCC) technology comes under this category. LTCC packages are constructed from a thin ceramic films stretched in a frame. Initially ceramic layer is in "green" i.e unfired form. Conducting transmission structures are screen printed over the film, via holes are punched, cutouts are made with laser and finally these individual ceramic layers are aligned, laminated and fired between 800 to 1000°C temperatures. LTCC packages use three dimensions for MMIC die cavity and vias. Reliability issues arise due to shrinkage of ceramic films during firing process and amount of shrinkage depends on the number of via holes. Transmission line losses is high in LTCC due absence of continuous ground plane. Increasing number of LTCC microwave modules are used in satellite subsystem due to light weight and compact size.

VI. CONCLUSION:

A brief overview about the various GaAS MMIC device technologies, failure modes and space qualification test procedures is presented in this paper. Packaging techniques practiced in satellite microwave applications is described.

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Breakdown Constraints and Qualification Approach for RF and Microwave Devices in Space Applications

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Abstract — RF and Microwave components tend to be mission critical since all Spacecrafts and Launch Vehicles rely on RF Systems for Telemetry, Tracking and Commanding. These applications put their RF devices through an extreme ranges of temperature, gravitational force, shock, vibration and pressure changes. Further the catastrophic space environment makes it challenging for highly sophisticated RF devices to meet stringent specifications. So it is necessary to design these components with breakdown constraints such as Corona, Multipaction, Electro migration, Time Dependent Dielectric Breakdown, Negative Bias Temperature Instability and Hot Carrier Effect in mind. The mechanisms of these phenomenon, their effects on the performance of RF devices are discussed in this paper. These internal failure modes can be hard to detect or analyze by direct testing of materials or devices. A generalized scheme for risk assessment and management against these constraints and availability of simulator tools for analysis is discussed in this paper.

Index Terms — Corona, Multipaction, Electro migration, TDDB, NBTI, Hot Carrier Effect, Qualification

I. INTRODUCTION

Satellite telecommunication industry as well as planetary exploration missions are demanding Microwave devices that need to deal with large bandwidths, power handling capabilities and high density component integration. These requirements lead to higher electric field densities which increase the risk of electrical breakdown to occur within the Microwave devices on board of satellites or launch vehicles.

Failures in RF and Microwave devices can be classified as either catastrophic failures or degradation failures. The exact mechanism, which causes the failure in normally dependent on the material structure, processing methods, application and stress conditions. Device bias, junction or channel temperature, passivation and material interactions may all contribute to different breakdown mechanisms [1]. Further, device handling, choice of materials for packaging and the environment can also cause failures.

At platform level during launch, the whole range of pressure levels and electric field are imposed onto hardware which leads to Corona effect that often determines the power handling limit. During On Orbit stage in Spacecrafts, Microwave devices are subjected to very high electric fields in vacuum. Risk of discharge such as Multipaction can get triggered and become critical for system functionality. These fields along with elevated temperatures can accelerate the Time Dependent Dielectric Breakdown (TDDB).

Electro migration phenomena is related to material transfer due to high current density which degrades the conductivity of the metal layer and adversely affects both RF and DC performance of the device [2]. Extreme temperatures experienced in space applications can interface traps and oxide discharge by a negative bias which increases the absolute threshold voltage, degrades mobility, drain current and transconductance of Metal Oxide Semiconductor Field Effect Transistors (MOSFET).

Hot Carrier Effect is the major reliability issue in MOSEFTs for space applications due to solar radiation exposure. It dictates the long term reliability of the MOSFETs. This can permanently change the switching characteristics of the device since charge carriers can get trapped in the dielectric of gate terminal.

All these failure mechanisms can lead to RF breakdown which degrades the specific devices and the life time of the satellite mission. Therefore all Microwave devices have to be analyzed for their Breakdown behavior especially when they are used for high power space applications.

II. CORONA

Free electron emission in space can adversely affect when it comes in contact with the ionized atmospheric gas trapped in Microwave devices. If the energy of these electrons increases because of the field from spacecraft's Microwave electronics, the electrons can excite the gaseous molecules within the devices. If the energy of the excitation is high enough, additional electrons may be released. This local electron population growth could exceed the diffusion rate and subsequently cause coronal discharge of radiation. Increased power density and component integration also make Microwave assemblies more susceptible to corona effects.

The consequences of a corona discharge are extremely harmful with in a Microwave device since the electron cloud formed by the breakdown onset reflects the RF signal that can lead to the destruction of the power source [3].

The discharge can severely increase the temperature, resulting in either drastic degradation of S-parameters or complete destruction of the device, with subsequent danger of missing the complete mission if that circuit is in Telemetry or Telecommand Subsystem.

III. MULTIPACTION

Free electrons can get trapped in metallic structures under high vacuum condition. When these devices are open to electromagnetic field emission from other subsystems in satellite or solar storms, these free electrons get accelerated toward the walls of the device and with enough energy, their impact can result in secondary electron emission.

If a resonance condition is established between these free electrons and RF signal, it results in repeated secondary electron emission that leads to self-amplification of current and finally to a significant and potentially damaging discharge which is called as Multipaction. The wall material can be characterized for its potential to induce secondary electron

emission per impact called as Secondary Electron Emission Yield (SEY). This characteristic is one of the important specifications when selecting a material for a space grade Microwave device.

If Multipaction discharge occurs, it can generate noise and reduce the output power by increasing the mismatch loss due to return loss degradation. This also results in increase of the device temperature. A prolonged discharge can increase the pressure inside the unit by outgassing the walls and dielectric material. This will result in ionization in presence of the fields, which may further lead to corona discharge and cause catastrophic failure.

Therefore any device carrying high RF power and operating in vacuum is susceptible to Multipactor breakdown and must be proved to have Multipactor threshold well above the operating power by a comfortable margin, typically 6 dB [4].

IV. ELECTRO MIGRATION

The movement of metal atoms along a metallic strip due to momentum exchange with electronics is termed Electro migration. Momentum transfer is dependent on temperature and number of electrons. So, this phenomenon is generally seen in narrow gates in power devices where the current density is greater than $2X10^5$ A/cm^2, which is normally used as threshold current density for Electro migration to occur. This effect occurs both perpendicular to and along the contact edges of the source and the drain and also at the inter-connection of multilevel metallizations.

The metal atoms that migrate along the line tend to accumulate at the grain boundaries. The accumulation of metal at the end of the gate or drain contact can create fingers of metal that can short the device [5]. Material accumulation and void formation perpendicular to the source and drain contacts can cause shorting of the gate to the source or the drain leading to catastrophic failure.

Gold based interconnects are widely used for interconnects on GaAs based electronics such as metal semiconductor filed effect transistors (MESFET) and Hetero-junction bipolar transistors (HBT) for high power space applications like communication payloads. Electro migration in Gold film can lead to resistance degradation behavior of the interconnects resulting in sharp impedance mismatch and power loss.

V. TDDB

Time Dependent Dielectric Breakdown is a failure mechanism in MOSFETs in which the gate oxide breaks down as a result of long time application of relatively low electric field as opposite to immediate breakdown, which is caused by strong electric field. The TDDB process takes place in two stages [6]. In the first stage, the oxide is damaged by the localized hole and bulk electron trapping within it and at its interfaces. The second stage is reached when the increasing density of traps within the oxide form a conduction path through the oxide. This short circuit between the substrate and the gate terminal results in Oxide breakdown.

Constant Voltage Stress or Constant Current Stress tests can be applied to test the behavior of TDDB. In the Constant Voltage Stress test, a voltage slightly lower than the immediate breakdown voltage of the oxide is applied to the gate, while its leakage current is being monitored. The time it will take for the oxide to break under this constant applied voltage is called the time-to-failure. This time is degraded in space applications due to elevated temperatures. The test is repeated several times on several samples to obtain reliability plots for predicting TDDB behavior of oxide at other voltages [7].

Depending on the extent of TDDB, even though the device continues to work, S-Parameters and Noise figure of the device or the circuit degrade drastically.

VI. NEGATIVE BIAS TEMPERATURE INSTABILITY

Negative Bias Temperature Instability (NBTI) is a degradation phenomenon in MOSFETs, which are stressed with negative gate voltages at elevated temperatures. It exhibits logarithmic dependence on time and is critical in terms of estimating mission life. Its effects are more extreme in p-channel MOS devices, since they are biased in inversion region i.e. with negative gate to source voltage most of the times. The same mechanism affects n-channel MOS devices also when biased in the accumulation region i.e. with a negative gate to source voltage. It is attributed to the creation of interface traps and oxide charge. This oxide electric field is usually lower than that can lead to hot carrier injection.

'Reaction-Diffusion' Model of NBTI is most prevalent one. According to this, interface traps are generated at the Si/SiO_2 (Silicon / Silicon Dioxide) interface with a linear dependence on stress time. Hydrogen is released during this reaction phase. In the subsequent diffusion phases, the hydrogen diffuses from the interface into the oxide with time dependence. Hydrogen atoms can also diffuse into the substrate.

In Silicon substrate, each Si atom is tetrahedrally bonded to four Si atoms in the wafer bulk. An interface trapped charge often called interface trap, is an interface trivalent Si atom with an unpaired valence electron at the SiO2/Si interface. Some models propose that Nitrogen used for retarding Boron penetration may be responsible for increased NBTI. The exact reasons for NBTI are still not completely understood. There may be even certain coupling between different mechanisms proposed.

The stress conditions for this NBTI typically lie below 6 MV/cm for gate oxide electric field and temperatures ranging from 100 to 300 °C [8]. Higher electric fields can cause additional degradation due to hot carriers and should be avoided for the evaluation of NBTI. High Oxide electric fields due to oxide scaling, Higher temperature due to high power dissipation, replacement of buried p-channel MOSFETSs with surface devices and Nitride oxides with high permittivity are the factors which have been found to increase susceptibility to NBTI.

NBTI results in decrease of Trans-conductance, Linear Drain current, Saturation current, Channel mobility, Sub-threshold slope and increase of Off state current and absolute value of the threshold voltage. The consequences can be reduced circuit switching speed as charging times for interconnect and load capacitances are increased or even circuit failures. The device degradation caused by NBTI can anneal to a certain extent when the stress conditions are diminished.

VII. HOT CARRIER EFFECT

Hot Carrier Effect refers to the effect in MOSFETs, where a carrier gains sufficient kinetic energy to overcome high electric filed across a MOS Channel and jump from the conducting channel in the silicon substrate to the gate dielectric. Their high energy along with scattering effect causes different types of defects such as the breaking of Silicon to Oxide bonds in the crystal structure at the interface.

Such crystal defects results in many intermediate energy levels between valence band and conduction band in the crystal structure. These states alter electric field within the device causing degradations in threshold voltage, transconductance, drain current, drain conductance and source conductance [9]. Moreover, these effects are cumulative. When stressed for longer periods, they become increasingly serious and reduce the useful lifetime of device.

VIII. QUALIFICATION APPROACH

Qualification can be defined as the verification that a particular component's design, fabrication and workmanship are suitable and adequate to assure the operation and survivability under the required environmental and performance conditions.

A qualification approach for Microwave devices in space applications should account for the sample to sample variations in the performance because of sensitivity to packaging tolerances, non-uniformities in properties in dielectric materials or substrates, workmanship, ESD sensitivity, pressure effects and radiation effects. Considering all these factors for the specific application, manufacturer should frame a procedure with user customized specifications. The approach involves the following steps:

1. Process Qualification
2. Design Verification
3. Inspection of Packaging Quality
4. Characterization of Nominal Performance
5. Stress Tests
6. Characterization of Temperature effect
7. EMI/EMC Test
8. Unit specific pre-shipment test

Process Qualification specific to the device and the application includes the quality testing of substrate / dielectric material for, documentation of fabrication and handling procedures, statistical analysis of life time and failure data of devices fabricated using that process. Once the process is qualified, Periodical Monitoring of the production line is also to update the statistics is also essential. No component specific performance is involved in this step. User should get the details and actively understand this process if the manufacturer is using pre-qualified process.

Design verification includes the verifying results of simulation model, layout of the design in case of packaged devices. It requires the knowledge of simulation tools, layout tools and device physics over temperature and pressure.

Inspection of packaging quality includes visual inspection, mechanical measurements and x-raying of each of the units to rule out any non-uniformities, deviation in dimensions and connector joint defects.

Characterization of nominal performance involves the measurement of S-parameters and impedance in case of dies. It includes complete device related RF performance characterization like current, gain, noise figure, noise floor, spurious emissions etc. on selected number of samples from each lot.

Stress includes testing of selected number of samples upto extreme levels for environmental and launch related effects and breakdown mechanisms caused by electric filed related stress effects. It also involves testing of each of the units of the lot at scaled down levels. First kind of tests are done to find out the threshold levels of temperature, pressure, vibration and shock level independently below or above which the device can perform satisfactorily. Breakdown related test includes testing for the breakdown mechanisms applicable to the device at nominal temperature and acceleration of breakdown phenomenon at elevated temperature, electric field and radiation levels.

Characterization of Temperature effect includes testing of each of the samples over the temperature range and monitoring of the applicable performance parameters depending on whether the device is a die or a packaged one.

Electro Magnetic Interference (EMI) Test involves testing of specific number of devices from lot for spurious levels and radiation leakage to ensure it does not affect surrounding systems when used in system level. Electro Magnetic Compatibility (EMC) Test involves testing has to be done to find out the maximum level of unintended radiations in an integrated RF environment that will not affect nominal performance of the device.

Unit specific pre-shipment test includes nominal verification of performance parameters to inspect whether performance has deviated compared to that before stress tests.

The Qualification approach discussed above results in assurance of device performance as well as device life time related reliability to the user.

IX. SIMULATION TOOLS

Testing for breakdown mechanism of a Microwave device requires lot of of tests and qualification procedures, huge investment of time and money. By utilizing advanced electromagnetic and structural simulators, the prediction and analysis of breakdown mechanisms becomes easier.

Integrated simulation environments such as CST Studio Suite and ANSYS Multiphysics can provide simulation results closer to that of real world phenomenon [10]. The simulation environments includes models of different physical interactions to reveal their impact on highly detailed 3D structures. They can even bring out the masked internal failure modes which can be hard to detect or analyze in physical tests. SPARK3D is a Multipaction tool that uses the electromagnetic fields distribution obtained by full wave analysis and calculates Multipaction threshold for different materials with known Secondary Electron Emission Coefficient. ESA/ESTEC another Multipaction analysis tool that calculates Multipaction threshold and safety margin for some known structures given the frequency, power level, impedance, minimum gap and finish material [11].

For example, a recent application note details the use of CST Studio Suite and SPARK3D to investigate the effects of Multipaction and Corona within a three pole L-Band filter for Space applications. The first step is S-Parameter evaluation with the frequency domain solvers of CST Studio. The simulation uses conformal tetrahedral meshes for high accuracy. From the full wave simulation, the pass band is

obtained and optimized. The 3D electromagnetic field is also obtained from the same simulation. Assumption of parallel plate geometry in this simulation deviates the simulation results from real world results. More rigorous Particle in Cell simulation can be performed to include the dominating effect of fringing fields.

Once the design of the component is done in terms of S-parameter response, the high power analysis can be performed by exporting the field information to SPARK3D. Using the field information, material data, SPARK3D calculates the Multipaction breakdown threshold by sweeping automatically in power. Breakdown occurs if the electron population increases with time. For this particular example, the Multipactor breakdown power level computed was 27.5 W and the actual tested result was 32 W [12].

Similarly the breakdown power level can be obtained as a function of the pressure for a particular gas. In this example, the device was tested at the critical pressure with a breakdown power level of 1.9 W and the simulation result at the same pressure was 1.6 W, which shows the simulation tools have a reached a level of optimum sophistication that is necessary to reduce the time and cost consumed for qualification testing on each of the device units.

X. CONCLUSION

The qualification of a Microwave device for a space applications requires thorough understanding of the process technology, failure mechanisms related to materials or processes or operating conditions or environment, relevance to the application and methods for risk assessment and management. Also proper shielding and packaging of devices to mitigate radiation effects in catastrophic space environment are extremely important. The standards for qualification of Microwave devices need to be updated in parallel with the research findings on reliability and failure mechanisms; and device fabrication technologies.

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EEE Parts for Small Satellite Missions

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Abstract—Small Satellites are growing in popularity and utility. Global importance and development of Small Satellite Missions (SSM) has increased at a very significant pace over last decade. Small satellites offer valuable missions with current and emerging technologies, for new and revolutionary missions of science, military, space exploration and Earth observation. This is particularly important for countries emerging in space technology, which can then have access to space missions, applications and spin-off technologies. Together with quick turnaround time, the inherent reduction of launch costs offered by the reduced size and mass of the spacecraft and their more manageable proportions, small satellites become attractive ways to develop and establish a national expertise in space technology and to serve the needs of all countries in accessing new missions.

The Small Satellite Mission philosophy can be stated as essentially a design-to-cost approach, within strict cost and schedule constraints by taking full advantage of technological developments—the miniaturization of engineering components and the development of micro-technologies. Small Satellites has to meet a big challenge of high performance by means of miniaturized subsystems and especially with small budget. Affordable small satellites require a very different approach towards the management of Electrical, Electronic, Electromechanical (EEE) parts and technology, if performance, cost and delivery targets are to be met. Various EEE parts management approaches are required to meet the requirements of the SSM. One such possible option is to consider the usage of Automotive Grade EEE parts.

This paper is an attempt to bring focus on the EEE part option not often considered: high-reliability, high-production automotive technology to the high-reliability low-production market of space systems especially for SSM. These parts are qualified to Automotive Electronic Council (AEC) specifications and carry the advantage of known-good die, screened, shorter lead time, high production volume and low price. Automotive electronics undergo a qualification process beyond that of typical industrial electronics in exceptionally harsh environment of temperature, vibration, shock, life test and electrical faults. Usage of these parts have challenges in terms of Traceability, Hermeticity, Radiation, Outgassing, Green finish etc are addressed here. Complementary tests which may be required to perform on these parts are briefed. Of course, lot of further studies, testing & evaluation may be required to freeze this approach.

Keywords—Small Satellite Missions, Automotive, EEE parts, Screening, Qualification, Statistical Process control, ISO/TS-16949, Production Part Approval Process.

I. .INTRODUCTION

During the early phases of the space age, satellites tended to be small, being limited by both the available technology and launch capability. As the technology improved and as launchers became more powerful, the size of the payloads naturally grew apace. In the expanding economies of the time, there was a desire to explore the new environment, and a feeling that space activities were at the cutting edge of engineering and scientific development. A strong user interest in cheaper and more frequent missions, is forcing the established space agencies to rethink their approach to spacecraft procurement and mission design.

Improved launch access to space is the main drive for the small satellite market and is behind a new focus on using small systems. Now that it's possible to readily place small satellites on launch systems being sent up Low-Earth-Orbit (LEO) at a fraction of the cost compared to in the past – for hundreds of thousands of dollars now, rather than millions – and on a fairly regular basis.

Small satellite program develops and demonstrates new and revolutionary technologies and capabilities for science, exploration and Earth observation. By developing new methodologies and techniques, small satellites can spearhead pioneering advances in experiments and technologies that are later flown on major missions.

Cost effective and high performance mission can be achieved by using different approaches and methods. One of the possible approaches is to take the full advantage of cutting edge technology with miniaturized component engineering [9]. Many of the COTS technologies prevalent in today's low-cost ground applications are now being adopted for space and making their way into small satellites. This paper gives a brief overview of Small Satellite Mission trends, application and challenges; the historical approach of EEE parts and their challenges for implementation in SSM; Automotive grade devices advantages and reliability challenges.

II. . SMALL SATELLITE MISSION

There is no universally accepted definition of what constitutes a 'small satellite'[10]. Any artificial satellite of low mass and low volume can be considered as a small satellite. Even with small spacecraft, there is a large variety of size and mass that can be differentiated as following

- Minisatellite, 100-180 kilograms
- Microsatellite, 10-100 kilograms
- Nanosatellite, 1-10 kilograms
- Picosatellite, 0.01-1 kilograms
- Femtosatellite, 0.001-0.01 kilograms

However, the definition can be enlarged to any system designed with the small satellite philosophy. This may include features such as commercial off-the-shelf components, modular systems, less redundancy, open sourcing, incremental missions, etc. It focuses on cost consciousness and low power electronics.

Small Satellites and systems have assumed significant roles in the world's space marketplace. Once thought of as only the toys of experimenters, small satellites now find themselves solidly entrenched in the mainstream of space applications. Traditionally utilized for Low-Earth orbit (LEO) missions, small satellites are now involved in geostationary (GEO) and planetary mission applications. They facilitate quicker, cost effective and reliable access to space. Small satellites are encouraging spacecrafts to design, test and try novel methods and technologies (E.g. open source hardware and software, formation flying), which might not be under the purview of large scale satellites. This remains the reasons as to why small

satellites have been considered a disruptive technology by numerous space mission experts. Small spacecrafts do not imply low technology and short lifetimes: on the contrary, they may mean very advanced technology, offering larger payload mass in relation to the total mass of the spacecraft.

A. Trends, Advantages, Challenges and Applications of SSM

Small Satellite is supported by the following trends:

- Advances in Electronic component miniaturization associated with insertion of novel performance [9].
- Market of new small launchers through the use of modified military missiles to launch small satellites [9].
- Small satellites provide independence in space in affordable manner for many countries to achieve Earth Observation & defense capability without relying on major space faring nations.
- Ongoing reduction in mission complexity as well as in those cost associated with management [11].
- Development of small ground station networks connected with rapid and cost effective data distribution network [11].
- Cost effective management and quality assurance procedures [11].

The advantages of small satellite missions are:

- More frequent mission opportunities fasten the return of science and application data [9].
- Faster expansion of scientific & technical knowledge bank [11].
- Extremely smaller budget and more dedicated mission objectives [2].
- Shorter development cycle [2].
- Implementation of new technologies with high risk [2].
- Provides opportunity for affordable constellations
- Greater involvement of students and small industry.

High performance and Low cost budget of small satellite imposes the following challenges [2]:

- Use of state of art technology
- Mixed strategy of quality level of EEE parts
- Dedicated quality assurance plan
- Risk management plan
- Extensive redundancy strategies
- Large design margins/ over design
- Robust design principles

Small satellites are used for applications such as:

- Telecommunication
- Earth Observation
- Scientific Experiments
- Demonstration of new technologies
- Academics Training

B. Complementarities of Small Satellite and Large Satellite

Small satellite missions do not replace large satellite missions, as their goals and issues are often different. Large satellite missions and Small satellite missions are considered to be complementary rather than competitive. By developing new methodologies and techniques, small satellites can spearhead pioneering advances in experiments and technologies that are later flown on major missions. Small satellites have several advantages over larger ones, for both large and small countries: more frequent and more varied mission opportunities; more rapid expansion of the technical knowledge base; greater involvement of local industry; and greater diversification of potential users. The number of positions available in geostationary orbit is limited and a longer lifetime increases the return on investment. Some problems are better addressed via distributed systems, for example, constellations of microsatellites or small satellites (typically for global coverage), while others may require centralized systems [10].

III. CLASSICAL APPROACH OF EEE PARTS

EEE parts are the foundations of a satellite. Quality of the part is an important factor in the success of the satellite mission. There are many types of EEE parts made worldwide that give excellent reliability in various types of applications for which they were designed. However some unique characteristics are required for space quality parts that most commercial and industrial applications do not demand, individually or in combination [3]:

- Space Vaccum
- Outgassing
- Radiation
- Extremely low defect level (about 10 ppm)
- Very long reliability (1 to 15 FITS)
- Conservative derating & application practices

A. Space Qualified EEE Parts

Historically parts qualified to MIL/ESCC/JAXA are being used in Hi-reliability, Space application. These parts undergo 100 % screening & lot quality conformance Inspection (QCI) tests. Periodic qualifications are carried out on these devices and are reviewed by MIL/ESCC/JAXA agency. Space qualified components are expensive not only because of their rigorous qualification processes and extended test cycles, often repeated at extreme parametric limits and under harsh environmental conditions, but also because they have to comply with strict rules set by international bodies that define quality and other performance or manufacturing criteria.

Any change in a device's specification, or the materials used to produce it, will usually require a complete requalification of the component or at the very least customer acceptance of a detailed change notification. Add to this the need to maintain availability of mil-qualified devices for 10 years or more, and the arguments supporting an alternative approach can be readily appreciated. Some characteristics of these devices are:

- Qualified to highest quality level of MIL/ESCC/JAXA
- Driven by controlled performance Specification
- Rigorous Certification process
- Manufactured in space qualified line
- Known performance (reliability)
- Radiation Hardened/Tolerant
- Temperature of -55°C to +125°C
- Full Traceability
- Interchangeability between manufacturers
- Process/Part Change Notification (PCN)
- Public Failure Exchange Program

Hermetic package
Fly as it is

However, some challenges are encountered while using these space qualified parts in SSM

State of art technologies & functions are not qualified for space on time.
Storage of space qualified parts is not always feasible.
Export regulations prevent generation of strategic stocks.
Very Expensive for small budget missions
Longer Lead time
Long journey for parts to enter into QPL/QML listing
Very few manufacturers

B. Alternate EEE Parts Option

Small satellite missions come in the category of “faster, better, cheaper” programmes. Out of all aspects cost aspect is one of the important drivers for small satellite missions. Affordable small satellites require a very different approach towards the management of Electrical Electronic Electromechanical (EEE) parts and technology, if cost, performance and delivery targets are to be met [10]. The possible use of alternate grade electronics as a means of cost and performance can be explored as below:

Military Grade
Automotive Grade parts
Telecommunication Grade parts
Medical Grade
Extended Performance/Temperature Commercial (EP)
Commercially Off the Shelf (COTS) parts

a) Basic Military Grade Parts
These parts are typical JAN or 883B Class devices. Theses meet the military temperature. They do not undergo 100% screening tests.
b) Commercially Off the Shelf (COTS)
COTS are the implementation of commercial current technology for traditionally customized applications such as military, industrial and space. Manufacturer or vendor solely establishes and controls the specifications for performance, configuration, and reliability (including design, materials, processes, and testing) without additional requirements imposed by users and external organizations. Many of the COTS technologies are making their ways into space.
c) Telecommunication Grade
These parts are qualified to the Generic Requirements for assuring the reliability of components used in telecommunication equipment established by Telecordia (earlier Bellcore) or by British Telecom. These devices undergo re-qualification testing every 2 years like space qualified parts.
d) Medical Grade
These devices are qualified to Food and Drug Act (FDA) Class 3 to ensure the reliable function of implantable medical electronics products. These devices undergo series of Operational testing, Mechanical testing, Environmental testing, Electrical testing, and Radiation testing as part of qualification.
e) Automotive Grade
These parts high reliable and high quality electronic parts qualified and comply with AEC ‘Q’ EEE part qualification and quality system standard for use in automobiles by major automotive manufacturers.

IV. IV. AUTOMOTIVE GRADE PARTS

Aerospace and automotive are two major manufacturing industries - also old industries born over a century ago. They have drastically evolved in the past 30 years in terms of product performance, leveraging **high technologies** and significantly **reducing time-to-market.** Both industries rely on rigorous quality requirements, advanced materials, electronics and embedded systems, mechanical components. The automotive market needs zero-defect products because quality and reliability are the most important factors in the automotive business market. To ensure quality, performance, and safety of the end product, industry associations have developed multiple standards including the International Automotive Task Force’s ISO/TS 16949, the Automotive Electronics Council’s AEC Q standard, and the Automotive Industry Action Group’s Production Part Approval Process (PPAP).

The Automotive Electronics Council (AEC) is an organization based in the United States that sets qualification standards for the supply of components in the automotive electronics industry. AEC was formed in 1993 by Chrysler, Ford Motor, Delco Electronics. AEC’s goal is to establish common part-qualification and quality-system standards for the EEE parts used in automobile industry.

The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing.

A. AEC Standards

AEC has issued key criteria in respect to design, quality, test and manufacture products for use in an automotive application. Standards have been established by the AEC Component Technical Committee to define common electrical component qualification requirements. These documents contain detailed qualification and requalification requirements and include unique test methods and guidelines for the use of generic data. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component level qualification testing. Suppliers may advertise components meeting these specifications without restrictions, but the specifications cannot be changed without the approval of the Sustaining Members. AEC developed several notable specifications for automotive electronics like:

AEC Q100 - "Stress Test Qualification for Integrated Circuits"
AEC Q101 - "Stress Test Qualification for discrete parts"
AEC Q200 - "Stress Test Qualification for passive parts"
AEC Q001 – "Guidelines for Part Average Testing"
AEC Q002 – "Guidelines for Statistical Yield Analysis”

Automotive parts are classified based on the operating temperature as:

Grade 0 -40°C to +150°C
Grade 1 -40°C to +125°C
Grade 2 -40°C to +105°C
Grade 3 -40°C to + 85°C

Grade 4 0ºC to + 70ºC

Features of Hi-Rel Automotive Grade parts are:

- Hi-Reliability for automotive application
- Six-sigma process implementation
- Known Good Die (KGD)
- Mass Production: availability
- Manufactured, Assembled & tested in ISO certified Fabs and plants
- Large number of manufacturers
- Shorter lead time
- Zero defect quality system approach
- Many Space qualified manufacturers are AEC Qualified
- Low cost compared to space grade
- Part Change Notification (PCN) system
- Minimum Data Documentation of part is available

B. ISO/TS 16949

This is the global technical specification and quality management standard for the automotive industry. It brings together standards from across Europe and the US. It is also not a mandatory requirement by AEC but many manufacturers comply with this standard. ISO/TS 16949 outlines everything we need to know about achieving best practice when designing, developing, manufacturing, installing or servicing automotive products. It is certified by third party. Periodic auditing is done by automobile manufacturers. A periodic internal audit, Full assessment of the quality system is performed typically every 3 years and partial assessment is carried out typically once a year [12].

C. Production Part Approval Process (PPAP)

Production Part Approval Process (PPAP) is used in Automotive Supply chain for establishing confidence in Part vendors and their production process. Automotive Industry Action Group (AIAG) has developed a common PPAP standard. The PPAP process is designed to demonstrate that the component supplier has developed their design and production process to meet the customer's requirements, minimizing the risk of failure by effective use of quality system. The purpose of any Production Part Approval Process (PPAP) is

- to ensure that a supplier can meet the manufacturability and quality requirements of the parts supplied to the customer
- to provide evidence that the customer engineering design record and specification requirements are clearly understood and fulfilled by the supplier
- to demonstrate that the established manufacturing process has the potential to produce the part that consistently meets all requirements during the actual production run at the quoted production rate.

PPAP is not mandatory as per AEC but many manufacturers have PPAP adopted in their system. PPAP is a document which has the record of the design, manufacturing process flow, Engineering change, process monitor parameters, Design & process failure mode and effects analysis, summary of tests performed on the part etc. Most importantly it contains a summary of every test performed on the part. This summary is usually on a form of DVP&R (Design Verification Plan and Report), which lists each individual test, when it was performed, the specification, results and the assessment pass/fail and any customer specific requirements. It needs a formal certification/sign-off by the supplier and approval/sign-off by the customer. The form that summarizes this package is called PSW (Part Submission Warrant). PPAP requirements are typically distinguished by level as follows:

- Level 1 – PSW only submitted to the customer.
- Level 2 – PSW with product samples and limited supporting data.
- Level 3 – PSW with product samples and complete supporting data.
- Level 4 – PSW and other requirements as defined by the customer.
- Level 5 – PSW with product samples and complete supporting data available for review at the supplier's manufacturing location.

Generally PPAP Level 3 is ordered by Automobile manufacturers.

C. Fabrication and Assembly of Automotive Parts

AEC Qualified devices are fabricated in either ISO-TS 16949, ISO 9001, ISO14001 certified foundry. All assembly and tests are carried out in ISO-TS 16949 certified locations. Most of the foundry and assembly sites are located in Malaysia, Japan, Taiwan, Korea and China.

D. Qualification of Automotive Parts

All the automotive parts undergo a set of stress tests mentioned in AEC'Q' specification like AEC-Q100, AEC-Q101, AEC-Q200. This contains a set of failure mechanism based stress tests and defines the minimum qualification requirements and reference test conditions for qualification of part [13]. An automotive grade device undergoes all the Qualification tests of a space grade device in addition to other important tests. A typical Integrated circuit chip has to undergo the set of tests like

Group A – Accelerated Environmental Stress Tests
Group B – Accelerated Lifetime Tests
Group C – Package Assembly Integrity Tests
Group D – Die fabrication Reliability Tests
Group E – Electrical Verification Tests
Group F – Defect Screening Tests
Group G – Cavity Package Integrity Tests

The below Table-1 tabulates the Gross differences in the Qualification of Integrated Circuit Automotive Parts and Space Qualified Parts.

Description	Space Qualified	AEC Qualified
Electrical	Group A of Mil-Prf-38535	Group E of AEC-Q100
Environmental	Group B of Mil-Prf-38535	Group A of AEC-Q100
Mechanical Test	Group B of Mil-Prf-38535	Group E of AEC-Q100
Life Test	Group C of Mil-Prf-38535	Group B of AEC-Q100
Package	Group D of Mil-Prf-38535	Group C/G of AEC-Q100
Radiation	Group E of Mil-Prf-38535	Not performed
Generic Data	Lot specific	Generic data is accepted
Requalification	Every 2 Years	Only when there is a change in Fab, design, process, assembly or Quality Assurance procedures
Sample Size	22-116 devices	5-77 devices

Table -1: Space Qualification Vs AEC Qualification

E. Screening of Automotive Parts

The automotive parts undergo 100% Electrical screening at wafer level as well as at finished part level. The screening is carried out as per AEC-Q001. The screening is based on a statistical method, called Part Average Testing (PAT), for removing parts with abnormal characteristics in a lot. The intent of PAT is to increase the quality and reliability of the parts as early in the part manufacturing sequence preferably at wafer level [14]. This method of screening provides "electrically" Known Good Die (KGD). A device specification defines the requirements of a part to work in the application. All the parts are tested to its electrical specification like Standby current, operating current, High and Low leakage currents , Switching characteristics like Propagation delay, Rise/Fall time, and extended operating tests like Low/High temperature, Low/High voltage operation, Dwell time at high voltage, Operating frequencies above/below specification, Safe operating capability for power devices. PAT uses statistical techniques to establish the limits on these tests. These PAT limits can be set in either a static or dynamic manner. Figure 1 shows the graphical representation of PAT limits and outliners.

Static PAT Limits = Mean $\pm$ 6 Sigma

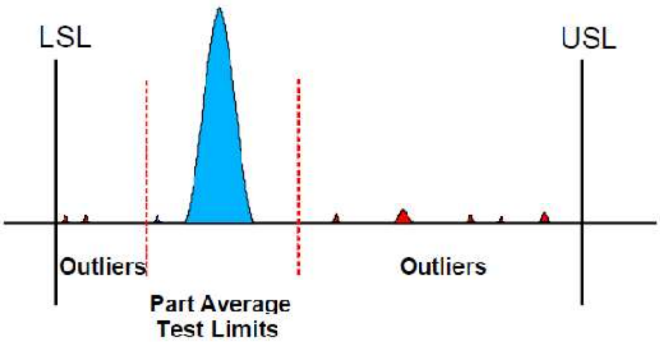

Figure 1: Graphical Representation of Part Average Test Limits and Outliers

PAT test analysis results are analyzed using AEC-Q002. It provides the guidelines for detecting and removing abnormal lots of material and thus ensuring the quality and reliability of the parts. It uses statistical techniques based on Statistical Yield Limits (SYL) and Statistical Bin Limit (SBL) for identifying a wafer, wafer lot or assembly lot that exhibits unusually low yield and unusually high bin failure rate [15]. The difference in the screening between Space grades and Automotive is tabulated in Table-2 below:

Test Description	Space Grade	Automotive
External Visual Inspection	100 % of lot	Most of the Vendors do 100 %
Environmental	100 %	Done only at the time of Qualification
Mechanical	100 %	Done only at the time of Qualification
Electrical	100 %	Most of the Vendors do 100 %
Burn-in with PDA	100 % for 240 hrs	Done only at the time of Qualification
Statistical Process	3 Sigma	6 Sigma
Screening Data	Available	Available if PPAP level 3 is ordered

Table-2: Space Grade Screening Vs Automotive Screening

F. Beyond AEC Specifications

Some manufacturers supply parts beyond the AEC specifications in terms of maintaining the quality system of ISO-TS 16949, providing PPAP document to customers, audit by customers, developing customer specific requirements of Source Control Drawing (SCD) with unique qualification tests and screening tests and graded as Automotive grade "plus" [12]. Many automobile manufacturers prefer to go for SCD based automotive grade plus quality parts with PPAP Level 3 documentation in support of the parts supplied.

V. RELIABILITY CHALLENGES OF AUTOMOTIVE PARTS

Automotive parts are designed, manufactured, qualified and tested for automobiles hence there are some challenges in adopting them for space application. The most important challenges are:

- Traceability
- Pure Tin Finish
- Outgassing
- Moisture absorption
- Cu bond wires
- No Radiation test data
- Large Minimum order quantity (MOQ)
- Storage & Handling
- Shorter product life cycle
- Interchangeability between manufacturers part

Automotive Parts are Hi-Rel parts meant for use in automobiles. In view of considering these parts for Space application some reliability concerns are to be understood & proper test and suitable mitigation to be adopted. The following section discusses the reliability issues & some mitigation techniques are suggested.

A. Mitigation to Tin Whisker growth

Most of the automotive parts come in pure tin (Sn) finish which is called by different terminologies as Eco Friendly or green molding finish or Restriction of Hazardous Substances (ROHS). Their terminations are made of lead-free metal alloys (often of pure tin) that are susceptible to growing whiskers. AEC-Q005 contains a set of tests and defines the minimum requirements for qualification of lead free (Pb-free) metallurgy for parts to be used in any automotive electronics application [16]. When a part involves Pb-free materials, certain tests must be performed and resulting data submitted for review before the part is approved for use. These tests are in addition to all electrical/mechanical testing required in the applicable part specification and include solderability, resistance to solder heat (if applicable), moisture sensitivity and Sn whiskering testing.

The science of whisker growth, including growth models and accelerated test methods, is not fully understood [16]. The following measures can mitigate the risk of whisker's growth:

Soldering with Sn/Pb alloys containing 40% of lead might change the composition of the finish, increase the concentration of lead at the terminations, and minimize whiskers' growth.

The risk of whiskering is lower for parts having a sufficiently thick, more than 7 µm, nickel plating at terminals.

Usage of conformal coating with a thickness of 100 µm or more can also lessen the whisker's problem.

Refinishing of the parts to replace the lead-free alloy can cause damage to the parts and is not recommended. This option if deemed necessary requires extensive additional testing and analysis.

Specifics of the composition of the lead-free solder, used flux, and the presence of contaminations on the board can also greatly affect the propensity for whiskering [17].

B. Outgassing

Most of the automotive parts are non-hermetic plastic encapsulated which inherently brings the advantage of small foot-print, less weight, more rugged to shock and vibration when compared to their counters parts of Hermetically sealed package. But there is a concern on the quality of the plastic used with respect to outgassing (vaporize). Gaseous emission from a material when exposed to reduced pressure and /or Heat is called as Outgassing. Certain materials used in PEMs outgas in vacuum environment where the material itself actually evaporates which not only jeopardizes the PEM integrity, but also poses a threat to sensitive surfaces such as optics. Outgassing materials can degrade sensors. The plastic molded parts should meet the National Aeronautics and Space Administration (NASA) outgassing requirement for space application of maximum Total Mass Loss (TML) of 1% and maximum Collected Volatile Condensable Materials (CVCM) of 0.1 %. Outgassing can be overcome by conformal coating the circuit board in a urethane derivative which will not outgas.

C. Moisture Absorption

Majority of the automotive components are plastic molded which inherently absorbs the atmospheric moisture within a very short period. If the moisture carries with it any ionic contaminants, the die metallization may corrode. When it occurs, corrosion of the metallization typically begins at the bondpads that are left exposed in order to permit wirebonding. High temperature and applied voltage can accelerate this mechanism. The interconnection wirebonds themselves are also susceptible to corrosion in the presence of moisture and contaminants. For production, dehydrate bake for PEMs (typically, 24 hours at 125C) is required to assure that the total absorbed moisture level is less than 0.05% of the total package weight and place in dry-pack packaging (desiccant and moisture indicator card in package), or nitrogen storage. A total absorbed moisture level of 0.11% of the total package weight is a recommended maximum limit (see ANSI/IPC-SM-786). Moisture ingression in PEMs can be minimized by the application of a MIL-I-46058 or IPC-CC-830 conformal coating. MIL-I-46058 coating types are AR (Acrylic Resin), ER (Epoxy Resin), SR (Silicone Resin), UR (poly Urethane Resin), and XY (paraXYlylene (parylene)). Urethane and parylene coatings have low moisture permeability with parylene being preferred due to its lower moisture permeability and its ability to cover sharp edges and transitions and to penetrate into PWB and PEM pinholes and cracks.

D. Storage and Handling

Non-hermetic, plastic-encapsulated surface-mount devices are particularly sensitive to moisture-induced stress during printed wiring board assembly. These moisture sensitive devices cannot be stored for a duration which depends on their sensitivity levels. If the device has absorbed moisture during storage, heating can cause this excess moisture in the IC package to vaporize and escape. This rapid vaporization can cause damage, such as package or die cracking, bond wire damage, and "popcorning", whereby the surface of the plastic encapsulation appears to bubble as a result of moisture escaping under pressure [18]. Automotive parts have large Minimum Order Quantity (MOQ) typically greater than 1000 pieces. These moisture sensitive parts cannot be stored for a longer duration. Buying in large quantity & storage may have reliability issues due to moisture absorption. These parts need to be stored in sealed Moisture Barrier Bags (MBB) and each bag contains a Humidity Indicator Card (HIC) in desiccants. These devices may require a regular inspection schedule to assure that all product bags maintain an adequate seal, as well as a re-baking and re-bagging.

E. Copper (Cu) wire Reliability

Copper wire bonds have replaced gold wire bonds in the majority of commercial semiconductor technologies for the latest technology nodes. Although economics has been the driving mechanism to lower semiconductor packaging costs for a savings of about 20% by replacing gold wire bonds with copper. Automotive AEC qualified parts have implemented the use of copper bond wires instead of Gold bond wires [12]. It has materials property advantages over gold. When compared to gold, copper has approximately: 25% lower electrical resistivity, 30% higher thermal conductivity, 75% higher tensile strength and 45% higher modulus of elasticity. Copper wire bonds on aluminum bond pads are also more mechanically robust over time and elevated temperature due to the slower intermetallic formation rate – approximately 1/100th that of the gold to aluminum intermetallic formation rate. However, there are significant tradeoffs with copper wire bonding - copper has twice the hardness of gold which results in a narrower bonding manufacturing process window and requires that the semiconductor companies design more mechanically rigid bonding pads to prevent cratering to both the bond pad and underlying chip structure. Furthermore, copper is significantly more prone to corrosion issues. Also, the selection of the device molding compound is critical because use of environmental friendly green compounds can result in internal CTE (Coefficient of Thermal Expansion) mismatches with the copper wire bonds that can eventually lead to device failures during thermal cycling [8].

F. Radiation

Radiation is the invisible specter of the satellite world, the unfamiliar menace to the EEE parts [1]. EEE parts are prone to radiation effects such as Total Ionizing Dose (TID), Single Event Upset (SEU), Single Event Latchup (SEL), Single event Burn-out (SEB) and Single Event Gate Ruptures (SEGR). Radiation is handled by cognizant architecture. Radiation data for automotive parts are not available. As the technology is shrinking EEE parts become inherently immune to TID. The concern is about the SEU and (SEL). Proper mitigation like Triple Modular Redundancy (TMR), Error Correction and Detection (EDAC), Watchdog Timer, Scrubbing can be implemented to mitigate SEU errors. Current monitoring circuit must be incorporated to mitigate SEL. SEB and SEGR are concerns for power devices. These devices should be used under sufficient derating conditions.

G. Traceability

Traceability is important when needing to demonstrate compliance to specification given to regulators/customers or to locate specific parts exhibiting particular symptoms. It is important to be able to track complete **part creation history**: when it was made, how it was made, what were the requirements, where it was made and by whom (supplier), what components were used, what was changed and why, but also traceability of the complete **part validation records**: operations status, original test data, intermediate and final test results, certification and compliance reports, test parameters records, dependencies, etc. Traceability is also achieved by using serial or **part numbers**, and including all of the data for future review and analysis. PPAP may provide part creation history. “AEC plus” parts may contain the traceability and all electrical data of the parts ordered by the customer.

VI. AUTOMOTIVE EXPERIENCE

IHI (formerly Nissan) Aerospace of Japan, in partnership with AeroAstro Inc., has developed OBCA, the On-Board Computer Architecture using automotive electronics. OBCA is an embedded processing system designed for use in spacecraft and other high-reliability environments. Much of its electronics, particularly the central microprocessor, are taken from an automotive screening process. OBCA is based on a Hitachi SH7055 embedded microprocessor, a 40 MIPS/ 40MHz RISC machine with 16 bit native register width and a plethora of hardware support features [1].

VII. SPACE AGENCIES INVESTIGATION

Many Space agencies are into the investigation of other quality EEE parts for the space application. One among them is the consideration of automotive grade parts. Many brain storming discussions and presentations are happening among many space agencies for use of automotive parts for space application as an alternative to space qualified parts. National Aeronautics and Space Administration (NASA) and European Space Agency (ESA) are exploring and evaluating the usage of automotive parts for low-risk space application. Many presentation & discussions have taken place regarding automotive parts at various international Space EEE conferences such as

NASA EEE Parts & Packaging (NEPP) Electronics Technology workshop [20], [21], [22],
Microelectronics Reliability and Qualification working meeting [23],
European Space Components Conference (ESCCON) [19], [24]
Microelectronics Workshop, JAXA [26].
EEE parts for Small Missions Workshop [25]

VIII. FUTURE WORK

Exhaustive study of the manufacturing, assembly, qualification and screening by various manufactures is required. Extensive study on Failure Modes Effects Analysis (FMEA) on these parts is required. Sufficient reliability data for these parts have to be established. Derating guidelines has to be established for these parts for space application usage. The accelerated testing is a valid tool to obtain confidence on the parts hence automotive parts should be evaluated through accelerated testing. These devices have to be characterized for Radiation and Outgassing. The exact match of the space qualified devices in this grade has to be explored. The interchangeability of parts between the manufacturers with respect to form, fit and function is to be studied. Understanding of customized Data deliverable as part of PPAP from manufacturer is required. The study, evaluation and analysis of the automotive parts can only give the solution to take a view on automotive parts for low-risk space application.

IX. CONCLUSION

Automotive parts are important candidate for non-critical small satellite application because of the significant improvement in the Quality and Reliability of the parts available today at low cost. An attempt has been made to address the various challenges & way forward in using these parts for small satellite non-critical application.

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Reliability Estimation for Wear out Failure Mechanisms in 180nm CMOS Process

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Abstract—This paper focuses on estimation of reliability lifetime for wear out mechanisms of EM, HCI & NBTI in 180nm CMOS process. Paper presents test structures used, testing methodology, and failure data analysis using statistical distribution and estimation of lifetime at use condition by extrapolation from stress conditions. Test structures with different design rules fabricated at SCL using 180nm standard CMOS process were tested on Cascade Microtech 1164 Reliability Test System for reliability estimation. SCL standard 180nm CMOS process is four layer metallization process with two types of transistor variants; High Voltage (HV) MOSFET with operating voltage of 3.3V and Low Voltage (LV) MOSFET with 1.8V. For EM testing, test structures covering contact, all metallization level and via levels were analyzed for both upward and downward current flow. HCI and NBTI testing was performed on both LV and HV MOSFET. Paper also brings out data analysis approach covering ranking the failure data, fitting the data, model parameter extraction, voltage and temperature acceleration factors, extrapolation at use conditions using statistical distributions such as Weibull and lognormal. Estimated lifetime evaluated was more than 10 years for EM. Similar results were evaluated for HCI & NBTI also. TDDB is also a prominent failure mechanism but its testing details are not covered under the scope of the paper.

Index Terms—**180nm CMOS process, EM, HCI, NBTI, MOSFET.**

I. INTRODUCTION

CMOS semiconductor industry is in persistent pressure to improve performance, increase functionality, reduce cost and decrease design & development phase of a microelectronic devices. As a result, device feature sizes are now in nanometre range, metal densities are high, layouts are complex, operating voltages are low, and frequencies are high. All together, device scaling has created a negative impact on device reliability. Hence, reliability requirements have become more stringent because of the dominant wear out failure mechanisms, coming in picture with scaling of CMOS devices. Major failure mechanisms known for CMOS based microelectronic devices are Electromigration (EM), Time Dependent Dielectric Breakdown (TDDB), Hot Carrier (HC) effects, divided into Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI).

Electromigration degradation is impact of aggressive interconnect scaling and associated thermal effects. It's migration of metal atoms due to momentum transfer from conducting electrons to metal atoms in the presence of electric field**.** Grain structure, grain texture, interface structure, film composition, current density, thermal stresses etc. are among many factors that influence EM [1-3]. High Temperature and current density are critical among them. Electromigration degradation is characterized by change in resistance, as it's associated with formation of hillocks and voids.

Hot carrier effects are primarily due to slower voltage scaling in proportion to dimensional scaling; as a consequence there is increase in peak internal electric fields. High electric field generates high energy carriers, referred as "hot-carriers" which can get injected into surrounding dielectric films such as the gate and sidewall oxides [1-3]. This results into degradation of device characteristics over prolonged period of time & eventually causing circuit to fail. Hot carrier degradation is studied separately for n type and p-type transistors. Phenomenon occurring in p-MOSFET is termed as Negative Bias Temperature Instability (NBTI).

SCL 180nm CMOS process has been experimentally evaluated for all the prominent failure mechanisms mentioned above. As dominant CMOS failure mechanisms are wear out mechanisms, hence their simulation on devices require accelerated testing. Testing conditions (current, temperature, voltage) are selected in order to accelerate the physics behind failures and bring the time to failure (ttf) close to few hours. This is called accelerated life testing [4]. Testing is done on specially designed test structure which allows only one failure mechanism to dominate at a time.

Rest of this paper is organized as follows: section II dedicated to details of experiments done to estimate lifetime for the three wear out mechanisms EM, HCI & NBTI. All experimental testing has been done using Cascade Microtech 1164 Reliability test system. Section III covers the experimental results and their interpretation. Section IV concludes the paper by expressing the way forward.

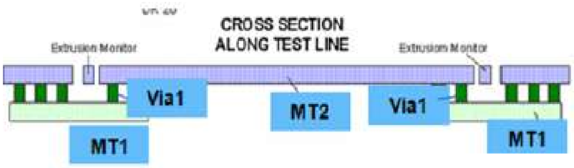
II. RELIABILITY TESTING & DATA ANALYSIS

Reliability estimation of SCL 180nm CMOS process for EM degradation and HC effects on test structures fabricated using standard 180nm CMOS process has been done through two main steps:

1. Reliability testing as per stress conditions to find time to failure (ttf) data.
2. Data analysis of failure data; which can be further divided as
   a) Ranking &Fitting the failure data
   b) Estimation of distribution parameters, followed by failure data.
   c) Calculation of lifetime at stress conditions.
   d) Transformation of results to Use condition (operating voltages, current & Temperature of technology node)
   e) Extrapolation of lifetime to targeted Cumulative failure fraction.

A. Electromigration testing

180nm CMOS process at SCL is four layer metallization process; each layer is a stacked metal layer, with Titanium (Ti) as bottom layer, Al with 0.5% Cu as main metal and top layer of Titanium & titanium nitride (TiN). All interconnects beginning from contact, metal level-1(M1), M2, M3 & M4, Via2, Via3 & Via4 were tested through eight types of test structures. (GMG_a, M212_a, M212_b, M121_a, M323_a, M434_b, M343_c & M343_d.) Every metal line to be tested has 5 pads, two for current sourcing, two for voltage monitoring and one for extrusion monitor. These devices under test (DUT) vary in metal line lengths, line width, overlap dimensions and number of contacts or vias [8]. Cross sectional view of typical EM structure has been shown in Fig. 1 below.



Courtesy: TSL

Fig. 1. Example of cross sectional view of EM test stuture.

a) Reliability testing – testing was performed referring Black's model [4] written as Eq. 1.

$$t_{50} = A/J^n * \exp(Ea/kT) \qquad (1)$$

Where A is process and material related constant, J is average current density, n is current density exponent, k is Boltzmann's constant, T is temperature in Kelvins, and Ea is temperature activation energy [3]

- For calculation of 'Ea', three sets each of 25 packaged structures were tested at three temperatures 220ºC, 235ºC & 250 ºC, using same current density J_{stress} =20mA/um^2. Ea calculated for eight different structures varied from 0.82eV to 1.1eV. [6-7]
- Current density exponent 'n' was calculated by testing set of 25 DUTs each at three different current densities J_{stress}=10mA/um^2, 15mA/um^2 & 20mA/um^2 at temperature=250ºC. Value of 'n' came around 1.7
- Time to failure (ttf) for each DUT was defined as time taken by DUT to report 10% change in initial resistance considering joule's effect. [6-7]

Figure 2 shows resistance versus time output of reliability test system for one type of test structure M212_b (metal level 1) for 16 devices under test at 250ºC. Calculation of Temperature Coefficient of resistance (TCR) [5] for each DUT & Joule's heating was done through 1164 test system.

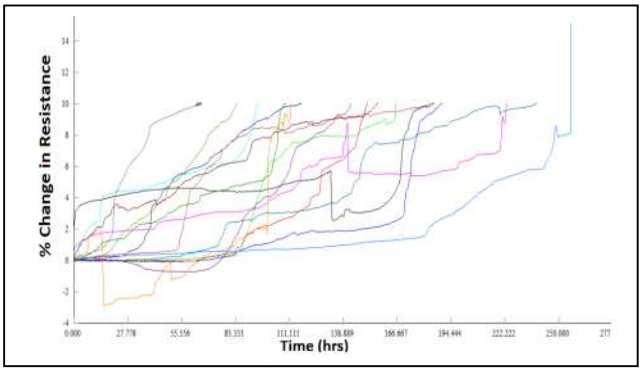


Fig.2. Plot of % change in resistance with time for EM structures of Metal-1, with downward current flow from M2 through Via2 for 16 different samples.

b) Data analysis-- Time to failure value of each DUT for every single experiment (T_{stress} & J_{stress}) was recorded and statistically analyzed as follow:

- Order of failure time was ranked using Median ranking [(i-0.3)/(N+0.4)], where i is order of failure & N represents total number of samples. Ordered failure time was expressed in Cumulative Failure percentage (F (t)). It was observed that the F (t) for EM degradation followed lognormal distribution with time to failure.
- Cumulative failure percentage F(t) was normalized and plotted to find parameters of distributions (shape parameter (σ) & location parameter (μ)) as expressed in Eq.2 to Eq.5. NORMSINV function returns inverse of standard normalized logarithmic cumulative distribution. z is called as probit and F(z) is identical to normal distribution.

$$F(t,\mu,\sigma) = \frac{1}{2} erfc\left[-\frac{(\ln t-\mu)}{\sigma\sqrt{2}}\right] = \Phi(z) = \Phi\left[\frac{(\ln t-\mu)}{\sigma}\right] \qquad (2)$$

$$\Phi^{-1}[F(t)] = \frac{\ln(t)}{\sigma} - \frac{\mu}{\sigma} \qquad (3)$$

$$normsinv[F(t)] = \frac{\ln(t)}{\sigma} - \frac{\mu}{\sigma} \qquad (4)$$

$$\ln(t) = \sigma * normsinv[F(t)] + \mu \qquad (5)$$

Plot for one of metal line structure (M212_a with metal line length as1000μm & width=0.23μm) has been shown in Fig 3. Estimated values of σ, μ have been tabulated in table I. Median time to failure ttf_{50} can be represented as exp (μ).

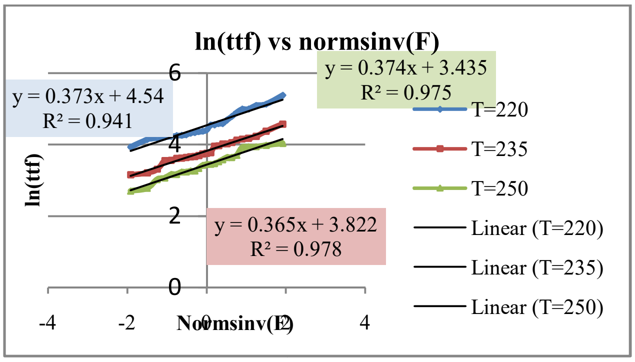


Fig 3. Plot of ln(t) with Normsinv (CFF) at three stress temp.

Temp	220°C	235ºC	250ºC
σ	0.373	0.365	0.374
$\mu = \ln t_{50}$	4.54	3.822	3.435
$t_{50\ (hrs)}$	93.6908	45.69551	31.03141257
$t_{0.1\ (hrs)}$	29.58724	14.79169	9.769381104

TABLE I. ESTIMATED PARAMETERS FOR EM TESTING

- From ttf_{50} at stress conditions estimated by experiments, ttf_{50} as Use conditions. (T_u=110ºC & J_u=1mA/um^2) was calculated using Black's expressed in Eq 6. Use conditions are tec node specified voltage, current and Temperature (6)

$$t_{50_u} = \frac{t_{50_s}\left(\frac{J_s}{J_u}\right)^n}{e^{\left[\frac{E_a}{k}\left(\frac{1}{T_s}-\frac{1}{T_u}\right)\right]}}$$

It was estimated to be around 75 years at use conditions for the structure M212_a with metal line length=1000µm & width=0.23µm

- Final step was extrapolation to desired Cumulative Failure Function (CFF) i.e. 0.1%, using Eq.7.

$$ttf_{0.1} = ttf_{50} * \exp[\sigma * Z(0.001)] \quad (7)$$

Time to fail for 0.1% population at use conditions (J_u, T_u) was estimated around 24.28 years

Using similar methodology reliability was estimated for rest of seven types of EM structures and results have been tabulated in next section.

B. Hot Carrier Testing

SCL 180nm CMOS process has two variants of transistors: Low voltage (LV) transistor with operating voltage of 1.8V and High voltage (HV) transistor with operating voltage of 3.3V. LV MOS is generally used for core circuit design and HV MOS for input/output circuit design. Hot carrier effects on test structures are studied as HCI for n-MOS and NBTI for p-MOS.

a) Reliability testing for n-MOSFET: - Hot carrier degradation was studied on SCL fabricated MOSFETs both low voltage and high voltage [9

TABLE II. STRESS CONDITIONS FOR HCI TESTING

- Three stress conditions were selected. Each stress condition is a unique set of Gate voltage (V_g) & drain voltage (V_d); as listed in Table II.

LV	Vg (V)	1.25	1.30	1.35
	Vd (V)	2.5	2.6	2.7
HV	Vg(V)	1.75	1.80	1.85
	Vd (V)	3.8	4.0	4.2

- Devices were initially characterized at normal operating conditions; using B1500-Semiconductor Parametric Analyzer for all parameters of MOSFET (I_{dsat}, V_{th}, I_{off}, I_{sub}).

- For reliability evaluation; LV devices with aspect ratio W/L= 10/0.18 & HV devices with aspect ratio W/L=10/0.35 was selected and packaged.

- For both LV & HV; three sets of 10 DUTs each were tested at three stress conditions as stated in table II above using Advance HCI module of 1164 Reliability test system. It has feature of on-the-fly testing required to minimize relaxation time.

- Time to failure for each DUT was defined as the time taken to observe minimum 10% degradation of saturation current (I_{dsat}t) from initial value. Figure 4 shows the change in I_{dsat} with time at one of the stress condition V_g=1.3V, V_d=2.6V for LV nMOSFET

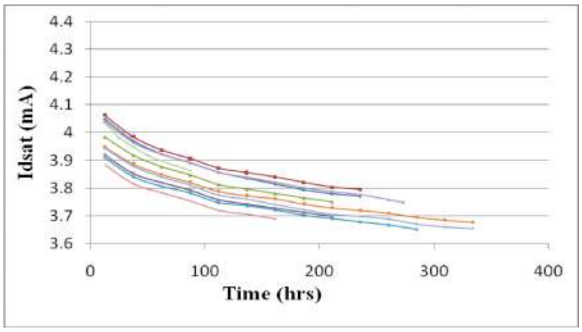


Fig.4. Variation of I_{dsat} with time for 10 samples of LV nMOSFET at stress condition (V_g=1.3V, V_d=2.6V)

Data analysis –

- Recorded order of failure time was ranked as per median ranking [(i-0.3)/(N+0.4)] and it was observed that time to failure with respect to cumulative failure fraction followed lognormal distribution.

- Parameters of lognormal distribution, µ and σ were estimated through the plot of Normsinv[F(t)]versus natural log of time to failure as explained in Eq 2 to Eq 4. Plot for LV n-NMOS at (1.3V, 2.6V) has been shown in Fig. 5 and related parameters covered in table III.

1/σ	3.084
µ/σ	16.53
σ	0.324254215
µ(intercept*σ)	5.359922179
ttf (50%) hrs	212.7083926

TABLE III. ESTIMATED PARAMETERS FOR HCI TESTING

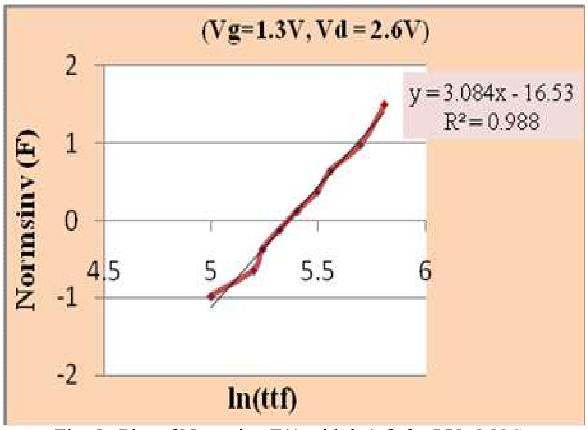


Fig. 5. Plot of Normsinv F(t) with ln(ttf) for LV nMOS

- Transformation from stress conditions to use conditions was done using model described in Eq 7 & Eq.9. Parameters of model (A&B) were estimated through plot between ln(ttf) and inverse of drain stress voltage as per Eq 8.

$$ttf_{stress} = A \exp(B/V_{dstress}) \quad (7)$$

$$\ln(ttf) = \ln(A) + B/V_d \quad (8)$$

$$ttf@\ use = A*\exp(B/V_{duse}) \quad (9)$$

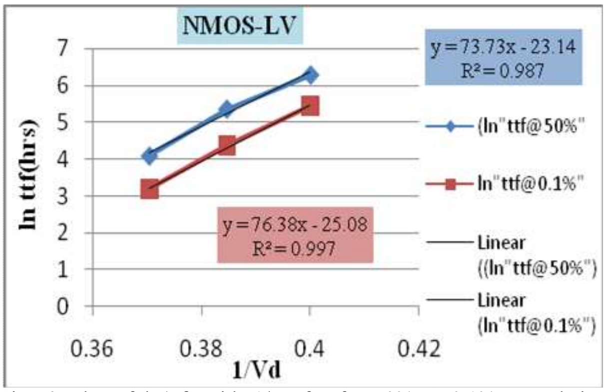


Fig. 6. Plot of ln(ttf) with $1/V_d$ for for 50% & 0.1% Cumulative failures

b) Reliability testing for p-MOSFET: - Effect of energized holes was experimentally studied through NBTI testing. In NBTI test, pMOS devices were initially characterized using B1500 parametric analyzer and 20 good samples of both LV and HV p-MOSFET were selected for reliability testing. Devices were biased only at gate terminal $V_{gstress}$ = 1.1 Vg keeping all other terminal at zero potential. For LV p-MOS $V_{gstress}$ =1.98V and for HV p-MOS $V_{gstress}$ =3.63V.

Under these gate bias conditions, devices were kept for 168 hours at 150ºC. Due to injection of energized holes into gate oxide, degradation in saturation current and increase in threshold voltage (V_{th}) was observed [10]. Change in threshold voltage was monitored, for change more than 10mVafter 168 hours, devices were considered to be failure otherwise not.

III. RESULTS

A. Electromigration results

TABLE IV. ESTIMATED RESULTS FOR EM TESTING

Structure Name	Tested for (current flow)	Stress conditions (J or I)	σ	E_a (eV)	Use Cond. (J or I) Tuse :- 110ºC	Life time estimated at Use conds in yrs ($t_{0.1\%}$)	Test Results
GMG_a	Contact	0.48mA	0.39	1.16	0.58mA	7.42	Fail
M212_a	Metal 1	20mA/um²	0.37	0.82	1.0mA/um²	27.4	Pass
M212_b	Via 2 (down)	0.48mA	0.46	1.07	0.28mA	18.61	Pass
M121_a	Via 2 (up)	0.48mA	0.33	0.99	0.28mA	64.45	Pass
M323_a	Metal 2	20mA/um²	0.25	0.99	1.0mA/um²	58.52	Pass
M434_b	Via 4 (down)	0.78mA	0.36	0.83	0.7mA	3.77	Fail
M343_c	Metal 4	18mA/um²	0.12	0.93	1.6mA/um²	1672.3	Pass
M343_d	Via 4 (up)	0.78mA	0.47	0.92	0.7mA	46.32	Pass

Estimated lifetime (t $_{0.1\%.}$ specifies the period of time that would elapse before 0.1% of test structures report failure; if operated under nominal current density and temperature.

Estimated lifetime for all 08 EM test structure except contact (CS) and Via 4 (V4) was more than 11.4 years, the reliability target set for 180nm technology node.

Failure analysis for failed test structure (CS &V4) was done to highlight the cause behind not meeting reliability target. The aim was to bring necessary changes in the process & ensure that the reliability target is met during final qualification of process. Details of failure analysis are not covered in this paper.

B. HCI results

1) $t_{0.1\%}$ for NMOS LV test structure is ~39.18 yrs
2) $t_{0.1\%}$ for NMOS HV test structure is ~1.22 yrs

Both test structures lifetime was more than the specified reliability target of 0.24 years

C. NBTI results

For, SCL fabricated p-MOS two samples out of 20 LV p-MOS reported Vth more than 10mV & no failures were observed for HV p-MOS.

IV. CONCLUSION

First ever attempt was made to estimate the reliability of SCL 180nm CMOS process for prominent wear out mechanisms. Electromigration degradation and Hot carrier effects were experimentally evaluated at test structures. Failure data of experiments was analyzed and the estimated lifetime at technology node defined operating voltages, current densities and temperature was verified. Estimated lifetime met the reliability lifetime target set for SCL 180nm CMOS process. The expertise gained in performing reliability tests and doing data analysis will useful for the SCL CMOS process qualification both at level-1 and level-2. It will be also useful in qualifying the upcoming variants of

SCL process like 5V process, process with six-layer metallization, etc.

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Characterization of space grade connectors for corona effect

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Abstract: Connectors used in high altitude applications are prone to corona discharge. A corona discharge is an electrical discharge brought on by the ionization of air surrounding a conductor that is electrically charged. Spontaneous corona discharges occur naturally in high voltage systems unless care is taken to limit the electric field strength. Corona occurs when the strength of the electric field around a conductor is high enough to form a conductive region, but not high enough to cause electrical breakdown or arcing to nearby objects.

Corona discharge usually forms at highly curved regions on electrodes, such as sharp corners, projecting points, edges of metal surfaces, or small diameter wires. The voltage at which corona occurs depends on the altitude/ atmospheric pressure and the distance between the conductive elements.

In space application corona can lead to failure of the mission itself. So the selection of the component for the required voltage is one of the prime factors. In satellite, various types of connectors are used for different applications. In connector, corona discharge can occur between the contacts and between the contact and the shell.

This paper analyses the tests conducted on different types of space grade connectors at high attitude under vacuum condition.

I. INTRODUCTION

Corona is a phenomenon that has the capability for degrading insulators, and causing systems to fail. Corona, also known as partial discharge, is a type of localized emission resulting from transient gaseous ionization in an insulation system when the voltage stress, i.e., voltage gradient, exceeds a critical value. The ionization is usually localized over only a portion of the distance between the electrodes of the system. Corona can occur within voids in insulators as well as at the conductor/insulator interface [1].

Corona can be visible in the form of light, typically a purple glow, as corona generally consists of micro arcs. Darkening the environment can help to visualize the corona.

The presence of corona can reduce the reliability of a system by degrading insulation. While corona is a low energy process, over long period of time, it can substantially degrade insulators, causing a system to fail due to dielectric breakdown.

High voltage connectors for ground operation (ambient pressure) are available in many variants for voltages up to a few ten kV, for higher voltages as single pin for moderate and low voltage as multi pin connectors. For operation in vacuum the choice of suitable connectors is very limited. The main problem for the design of such a connector is the interface between the interlaced insulation of the plug and the receptacle.

Three strategies for the design of this interlaced interface should be taken into consideration:

- Gapless interface of plug and receptacle insulation, by using slightly conical structures with a soft insulation material in between
- Interface with vented gap
- Interface with hermetically sealed gap

The gapless interface is difficult to achieve as it requires high precision of the manufacturing and a suitable soft insulation material for the interface.

Using a connector with a vented gap will operate stably, only if the critical pressure range in the interface can be avoided, i.e. by sufficient outgassing time in a high vacuum environment before applying high voltage. The vented gap becomes critical under ambient environment if the inception threshold for partial discharges is exceeded and especially if an AC voltage is applied.

A hermetically sealed interface can grant stable operating conditions for short term independent of probably critical pressure outside, however, can reach a critical pressure due to leakage after long term exposition in space vacuum [2].

II. CORONA PREVENTION

Corona can be avoided by minimizing the voltage stress and electric field gradient. This is accomplished by utilizing good high voltage design practices, i.e., maximizing the distance between conductors that have large voltage differentials, using conductors with large radii, and avoiding parts that have sharp points or sharp edges. Corona inception voltage can sometimes be increased by using a surface treatment, such as a semiconductor layer, high voltage putty or corona dope.

Ensure that steps are taken to reduce or eliminate unwanted voltage transients, which can cause corona to start.

The large quantity of existing connector and cable designs make it very difficult for the engineer to make a good choice when faced with selecting connector for high voltage applications. Today it is often common practice to consider high voltage and corona free as synonymous.

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III. DETAILS OF TEST PERFORMED

A test was performed on three types of space grade crimpable connectors namely D-sub 5pin Combo connector with power contacts, D-sub standard density 9pin connector and DBAS Circular 37pin connector. These three types of connectors do not fall under any category of gapless interface, interface with vented gap or hermetically sealed. These are the general purpose space grade connectors which are suitable for low voltage applications.

Presently in our space programme, connector usage is well within the rated working voltage. Due to the new requirement of connector usage with high voltage of 600V at high altitude test was conducted to know the suitability of present connectors. Scope of the test is to find out the voltage at which corona occurs at different vacuum levels.

As per ESCC specifications, rated DWV (Dielectric Withstanding Voltage) for D-sub connectors is 1000Vrms and working voltage is 300Vrms. For Circular 37pin connector rated DWV is 1500Vrms and working voltage is 300Vrms. In general, these connectors are not suitable for high voltage application of 600V at high altitude condition [3].

3.1 Test setup and procedure

Test was performed in transparent vacuum chamber to visualize corona occurrence. Test setup is as shown in below figure 1.

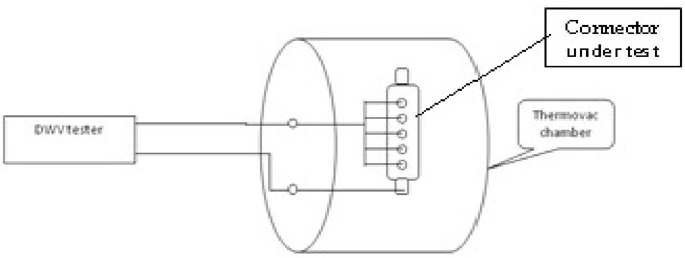

Figure 1: Test setup

Sample size: Test performed on one connector of each type with required contacts.
Sample preparation: Contacts were crimped with space qualified wires and inserted in the connector. The connector was then placed inside the vacuum chamber.

Test procedure: Connector was wired and placed inside the vacuum chamber. Test voltage is applied using DWV tester. Corona effect or leakage current was monitored with visual leakage indicator of the tester. Initially at room condition connector was tested for 1000Vrms. Later vacuum increased to 10^{-6}torr and tested by applying voltage in steps till corona occurrence observed. Test was repeated as above at 10^{-2} torr, 1 torr and 8 torr vacuum levels and results are recorded.

Test was repeated again with connector potted using RTV3145 material to find out that potting can improve the performance.

3.2 D-sub Combo connector with power contacts

Separate test performed on connectors without potting and on connectors with potting. Space grade 10AWG wire crimped in the contacts and inserted into the connector.

Part details:
Plug connector: 311P10-10P-B12
Socket connector: 311P10-10S-B12
Pin contact: 340104007B
Socket contact: 340104008B
Manufacturer: ITT

Table -1: Test results on Unmated Plug connector without potting

Sl. no	Vacuum level (torr)	Voltage applied between (Vrms)			Result
		Adjacent pins	Pin and shell	All contacts shorted and Shell	
1	At room ambient	1000	1000	1000	No corona
2	10^{-6}	1000	1000	1000	
3	10^{-2}	1000	700	640	Corona observed
4	1	280	280	260	
5	8	300	400	380	

Table -2: Test results on Unmated Plug connector with potting

Sl. no	Vacuum level (torr)	Voltage applied between (Vrms)			Result
		Adjacent pins	Pin and shell	All contacts shorted and Shell	
1	At room ambient	1000	1000	1000	No corona
2	10^{-6}	1000	1000	1000	
3	10^{-2}	1000	1000	1000	
4	1	280	280	260	Corona observed
5	8	400	340	340	

Table-3: Test results on mated connector with potting

Sl. no	Vacuum level (torr)	Voltage applied between (Vrms)			Result
		Adjacent pins	Pin and shell	All contacts shorted and Shell	
1	At room ambient	1000	1000	1000	No corona
2	10^{-6}	1000	1000	1000	
3	10^{-2}	1000	1000	760	Corona observed
4	1	520	480	360	Corona observed
5	8	440	360	320	Corona observed but not visible

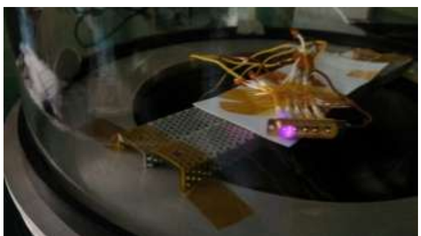

Figure 2: Corona observed when voltage applied between two contacts

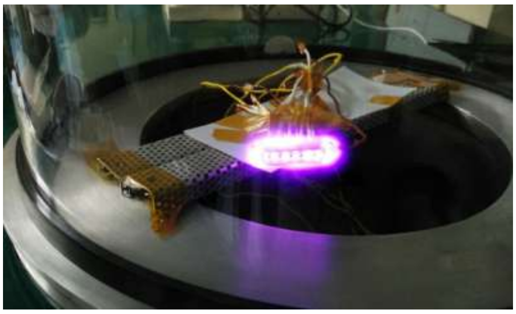

Figure 3: Corona observed when voltage applied between all contacts shorted and shell

3.3 D-sub standard density 9pin connector

Contacts are crimped with space grade 20AWG wire and are loaded in the connector.

Part number details:
Plug connector: 311P409-1P-B12
Socket connector: 311P409-1S-B12
Pin contact: G10P1
Socket contact: G10S1
Manufacturer: ITT

Table-4: Test results on mated connectors without potting

Sl. no	Vacuum level	Voltage applied between (Vrms)				Result
		Adjacent pins	Between row	Pin and shell	All contacts shorted and shell	
1	At room ambient	1000	1000	1000	1000	No corona
2	10^{-6}	1000	1000	1000	1000	
3	10^{-2}	780	840	780	720	Corona observed
4	1	600	580	400	380	
5	8	380	420	380	400	

Table-5: Test results on mated connectors with potting

Sl. no	Vacuum level (torr)	Voltage applied between (Vrms)				Result
		Adjacent pins	Between row	Pin and shell	All contacts shorted and Shell	
1	At room ambient	1000	1000	1000	1000	No corona
2	10^{-6}	1000	1000	1000	1000	
3	10^{-2}	1000	1000	1000	1000	
4	1	600	580	560	400	Leakage

5	8	380	400	440	400	indication. Corona not visible

3.4 DBAS Circular connector 37pin connector

Because of the limitation of wires from the vacuum chamber, only 7 contacts are used out of 37 contacts. Contacts are crimped with space grade 20AWG wire and are loaded in the connector.

Part number details:
Plug: 340100801BDBAS76-37-0-PN
Socket connector: 340100801BDBAS70-37-0-SN
Pin contact: 0641-10-2059B
Socket contact: 0603-34-2059B
Manufacturer: Deutsch

Table-6: Test results on mated connectors

Sl. no	Vacuum level (torr)	Voltage applied between (Vrms)			Result
		Adjacent pins	Pin and shell	All contacts shorted and Shell	
1	At room ambient	1500	1500	1500	No corona
2	10^{-6}	1500	1500	1500	
3	10^{-2}	1400	1300	400	Leakage indication. Corona not visible
4	1	600	400	400	
5	8	750	650	500	Corona observed

Table-7: Test results on unmated socket connector

Sl. no	Vacuum level (torr)	Voltage applied between (Vrms)			Result
		Adjacent pins	Pin and shell	All contacts shorted and Shell	
1	At room ambient	1500	1500	1500	No corona
2	10^{-6}	1500	1500	1500	
3	1	380V	350V	400V	
4	8	400V	420V	480V	Corona observed

Figure 4: mated circular connectors

Figure 5: Corona observed when voltage applied between all contacts shorted and shell

IV. TEST RESULTS SUMMARY

1. Connectors are meeting DWV specification at room ambient (sea level) and at hard vacuum of 10-6 torr.
2. Critical pressure range observed from 8 torr to 1 torr.
3. D-sub combo connector with power contacts, corona was observed at 260V under 1torr and 300V at 8 torr.
4. D-sub standard density 9 pin connector, corona was observed at 380V under 1torr and 8 torr.
5. DBAS 37pin circular connector, corona was observed at 400V under 1torr and 500V at 8 torr.
6. No considerable improvement observed with potting.

V. CONCLUSION

In general, it should be highlighted, that the availability of space qualified connectors is very limited.

The appropriate connector design (if available) is depending on the intended use. Gapless interface and hermetically sealed gap interface can be suitable for short term applications (more) independent of the pressure environment, whereas vented gaps for long - term operation are better if used after a good outgassing in a high vacuum environment.

In addition to the interface between plug and receptacle, the interface between plug/socket and the attached cable is very essential. Typically a gap free interface should be achieved, for example by a suitable potting/gluing process. As this interface is very critical and requires a very well defined process it is mostly unavoidable to procure a connector assembly together with the cable from one supplier.

ACKNOWLEDGMENT

The authors thank Dr. M. Annadurai, Director, ISAC, Dr. M. Ravindra DD RQA, ISAC for their encouragement in carrying out this work. The authors also thank Smt V K Padma, Ms. Harinakshi, and members of UHV lab, ISAC for their extensive support.

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Transient Thermal Analysis of RWR-80 resistor onboard Mars Orbiter Mission

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Abstract— Power Distribution packages are very widely used in industrial, aerospace and other fields. The reliability of this subsystem package is dictated by the thermal performance of the PCB assembly it contains. Overheating is the key factor in affecting the reliability of the package because of the packaging density of the devices mounted on it. In order to obtain the temperature field contours of PCB assembly at different temperature level, a simplified 3D computational model accounting all thermal interfaces has been built, and steady-state and transient thermal analysis results of RWR-80 resistor are presented. Also sensitivity of thermal conductance of lead material of the electronic component is studied.

Index Terms—Resistor, PCB, transients, thermal analysis.

I. INTRODUCTION

A spacecraft consists of a number of electronic packages to meet the functional requirements. An electronic package is generally an assembly of printed circuit boards placed in a mechanical housing. Many varieties of electrical and electronic components are mounted on the printed circuit board (PCB) as per electrical design requirements. PCB along with components is known as PCB assembly. Electronic devices such as integrated circuits, resistors, capacitors and Quad Flat Packages (QFP) demand high quality and reliability. Failures of electrical and electronic components can occur due to variation of material, flaws in design and overheating [1]. According to Arrhenius' Law, chemical reaction rate exponentially increases with increase in temperature: when temperature increases by 10^{o}C, the reaction rate and consequently failure rate doubled. Suitable thermal design is required to ensure good thermal performance of the components and also that of subsystem [2]. With advancement of packaging technology, the number of components soldered in a given area increases multifold. Owing to the increase in packaging density in recent times, the heat flux of these components poses critical issues from thermal point of view and thermal failure becomes a major failure mode. Consequently, this calls for the detailed study of local hot spots due to thermal loading in order to ensure reliable thermal design [3].

In some situations, the subsystem package operating environment temperature and the working state are not fixed, but changes periodically. For example, temperature cycling test of subsystem package, environment temperature in which the subsystem has been tested changes periodically: the electronic package whose components operated intermittently, their working state changes periodically. Subsystem packages onboard spacecraft also have a periodically changing environment due to the variation in external heating. This way the electronic components will be heated and cooled alternately either due to change in heat dissipation or change in the onboard operating environment. Transient thermal analysis is essential to obtain the peak temperatures experienced by the critical components.

Power Distribution package is mounted internal to the Mars Orbiter spacecraft. This package is subjected to various temperature regimes right from clean room to Mars orbit and is critical from power distribution point of view. Before the Mars Orbit Insertion (MOI), the load profile was needed to be simulated on ground. The profile starts with orientation of the spacecraft in such a way that there is no generation in solar array and the profile ends where the reverse orientation takes place thereby resuming the solar array generation. Hence during the whole course of this activity, there is no power generation from solar array. Therefore the entire spacecraft power requirement is met by the onboard battery. When the fully charged battery starts discharging, the battery voltage falls gradually and hence the load current increases. The discharge current passes through the Battery Current Sensor (BACS) circuit, which is a part of power distribution module. The telemetry derived from this current sensor circuit, indicates the actual battery charge/discharge current of the spacecraft. Hence proper functioning of this circuit is essential during such a critical operation.

Prediction of temperature distribution for PCB assembly due to fluctuations in heat dissipation of critical components is essential for good thermal design and reliability of electronic packages. The modeling and analysis of PCB assembly is required for accurate prediction of temperatures in order to establish the design margins. It is required to perform thermal analysis to get the temperature distribution of the components, the PCB and to check the effectiveness of heat transfer path from the components to the base of the package. The present thermal analysis is performed to estimate steady-state temperatures of the components, temperature transients and to verify the predicted values are within the acceptable temperature limits specified.

II. RWR-80 RESISTOR

Figure 1 shows 3D geometric model of 2W RWR-80 resistor and these resistors need to be maintained below 125^{o}C with 50% de-rating applied. Main body of the resistor is made of ceramic material and is cylindrical in shape. It has two leads which will be soldered to mount it on the PCB. These leads are made out of copper and part of the heat dissipation is conducted to the PCB through these pins or leads and the remaining is radiated to the ambient. Maximum operating temperature of the resistor is decided by the absolute conductance of the leads which are function of geometric and material properties and thermo optical property of the surface of the resistor body. To

enhance the heat transfer from the resistor to the PCB, suitable thermal interface material (TIM) will be employed.

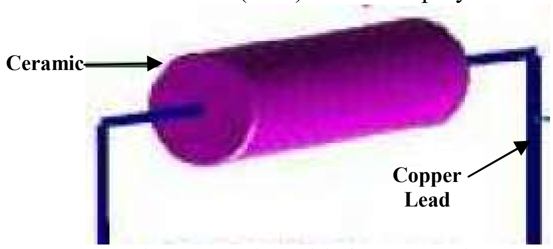

Fig.1 Geometric Model of RWR-80 resistor

III. DETAILS OF PCB

PCB card is multi-layered structures, wherein high thermal conductivity copper layers (k=385 W/m-K) are embedded to low thermal conductivity polyclad laminate. PCB base material is Polyclad Laminate/Prepreg Grade PCL-FR-370/PCL-FRP-30 with thermal conductivity of 0.36 W/m-K. Figure 2 gives the schematic of the PCB assembly and indicates only two modes of heat transfer; conduction and radiation. It mainly consists of RWR-80 resistors with turret mounting with the PCB. It is PCB with 10 layers and its effective in-plane thermal conductivity is estimated at 25.7 W/m-K [4-5]. The card has been given conformal coating to improve the moisture resistance and its IR emittance is 0.7 [6].

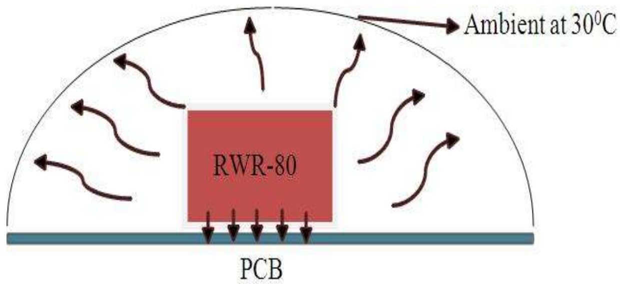

Fig. 2 Schematic of PCB assembly

IV. COMPUTATIONAL MODEL

Figure 3 shows the computational model of the PCB assembly developed using I-DEAS 13.0 software. It mainly consists of RWR-80 resistors of 20 numbers mounted with chotherm as thermal interface material (TIM) on PCB. PCB has been discretized using thinshell elements of appropriate thickness whereas resistors are modeled using solid elements. These solid elements are surface coated with shell elements in order to simulate radiative heat transfer from the component to the ambient. Table 1 gives the thermo physical properties used for developing the computational model. Interface thermal conduction factor for the TIM is considered as 1200 W/m^2-K [7]. To perform steady-state thermal analysis, total continuous heat dissipation simulated for the PCB assembly is 1.6 W. Figure 4 gives the lay-out scheme of the resistors on the circuit board. PCB is sitting on tray lugs with no interface material (interface contact conductance factor, h= 300 W/m^2-K).

Table 1 Model material parameters

	Material	Density (kg/m^3)	Conductivity (W/m-K)	Dimensions (mm^3)
PCB	FR4, Cu	1600	25.7	174.5×256.6 × 2.3
Resistor	Ceramic	6000	100	Φ 2.4 × 10.3
Leads	Cu	8900	385	Φ 0.5 × 13.0

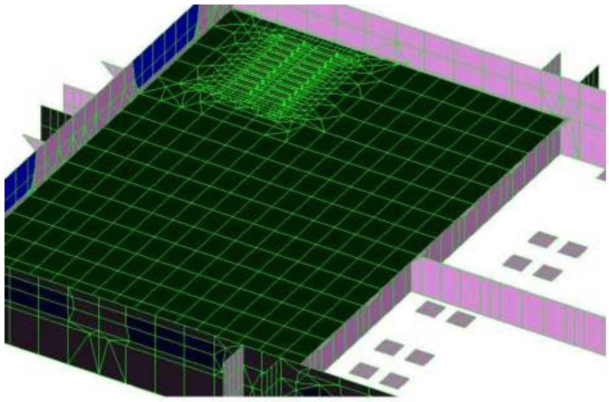

Fig. 3 Computational model of PCB assembly

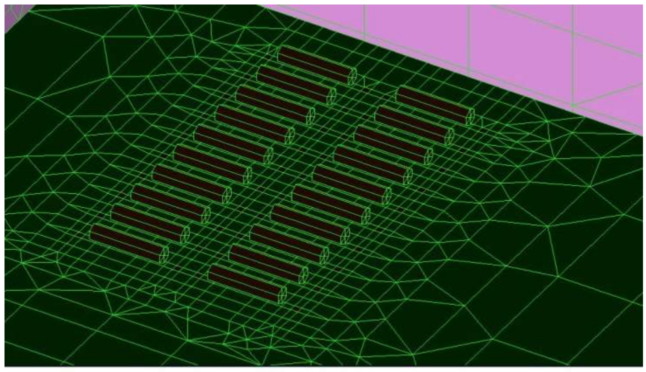

Fig.4 Layout of RWR-80 resistors

V. THERMAL ANALYSIS

Thermal analysis or thermal simulation is a kind of simulation technology, based on the principles of heat transfer and finite difference method. The purpose of thermal analysis is to obtain maximum operating temperatures of the components so as to ensure that operating temperatures will not exceed their allowable limits. Resistor elements are modeled as lumped masses indicating iso-thermal and there is no temperature gradient within. Steady-state thermal analysis can be applied to analyze temperature distribution of the PCB assembly and to validate the thermal mathematical model. Subsequently, transient thermal analysis has been performed to obtain the temperature rise of the resistor during Mars orbit insertion time. Table 2 summarizes the heat dissipation profile for each resistor. Initial temperature of the resistor is assumed at 25^0**C** for the analysis and two different case studied are performed to understand the sensitivity of thermal resistance of leads (0.006 W/K and 0.06 W/K) as there is uncertainty with length of soldering.

Table 2 Heat Dissipation

Phase	Dissipation (mW)	Duration (min)
Phase-1	484	21
Phase-2	1150	5
Phase-3	484	22
Phase-4	200	8
Phase-5	90	25

Figure 5 and 6 show the temperature contour of PCB assembly for the case of lead thermal conductance of 0.006 W/K. Rise in temperature of the resistor is purely controlled by its thermal inertia and depends on heat dissipation duration. Transient thermal analysis was carried out on the PCB assembly for two different lead conductances. In addition to this, ground test was done for the load profile as per mission scenario and the temperatures of the resistors were monitored. Main objective of the test was to ensure that the peak temperature of RWR80 resistor would not exceed its rated value even under worst case conditions. Figure 7 and 8 show the temperature rise of the resistor for given heat dissipation profile for case1 and case2 analysis respectively. Maximum temperature of the resistor observed during the test is 170^0C whereas thermal analysis prediction is at 190^0C. It can be seen that there is difference in peak temperature of RWR80 resistor between thermal analysis prediction value and the ground test data. This difference is attributed to two reasons; a) boundary conditions are not exactly similar and b) test was done for stand-alone configuration of the PCB assembly while the thermal analysis was performed at package level.

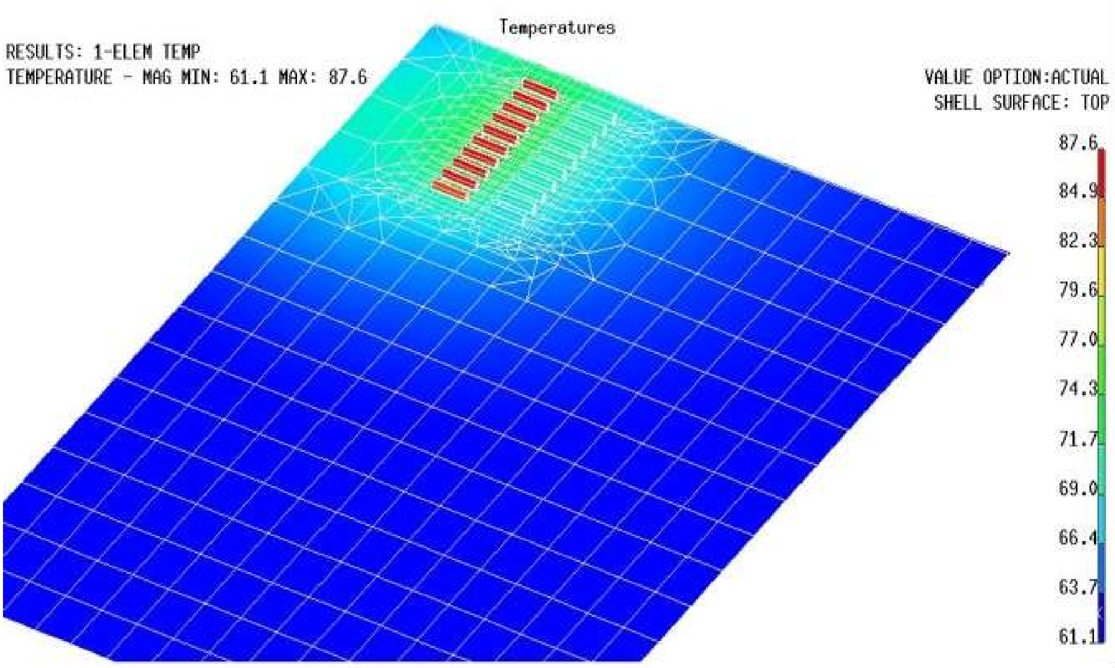

Fig.5 Temperature Distribution of PCB assembly

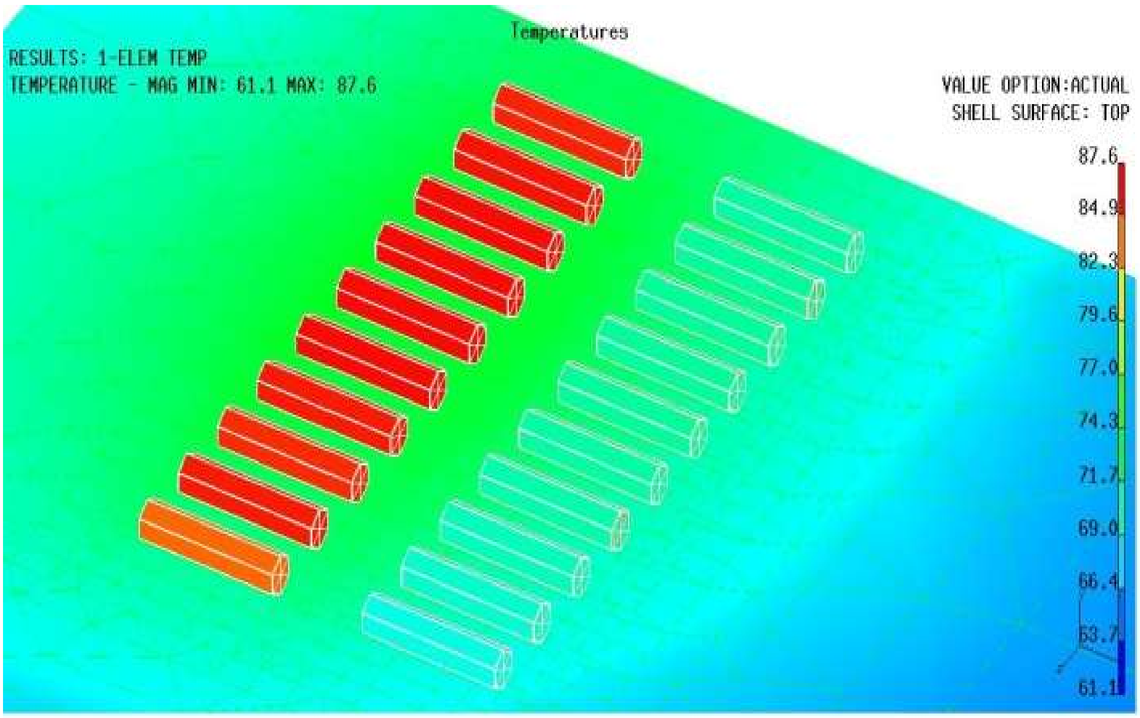

Fig. 6 Temperature Distribution of RWR-80 resistors

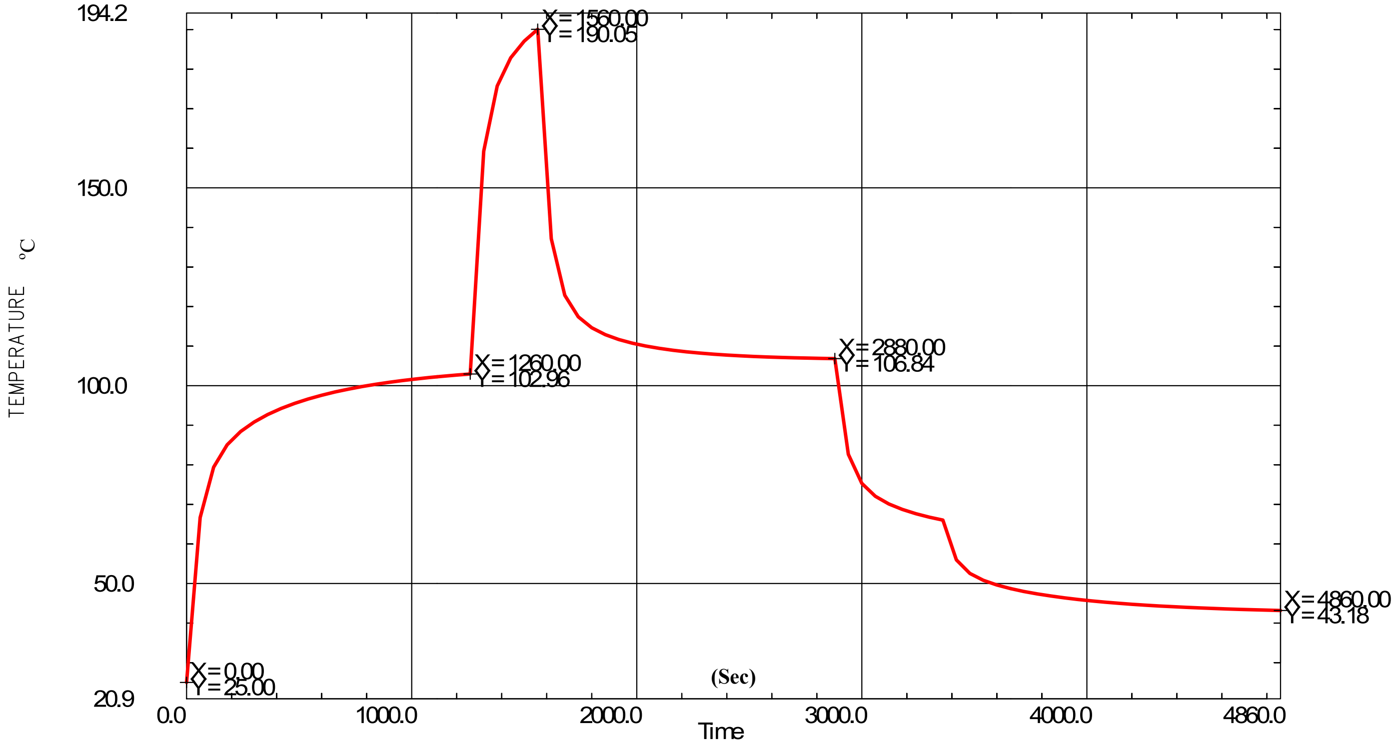

Fig. 7 Temperature transients of RWR-80 resistor for case1

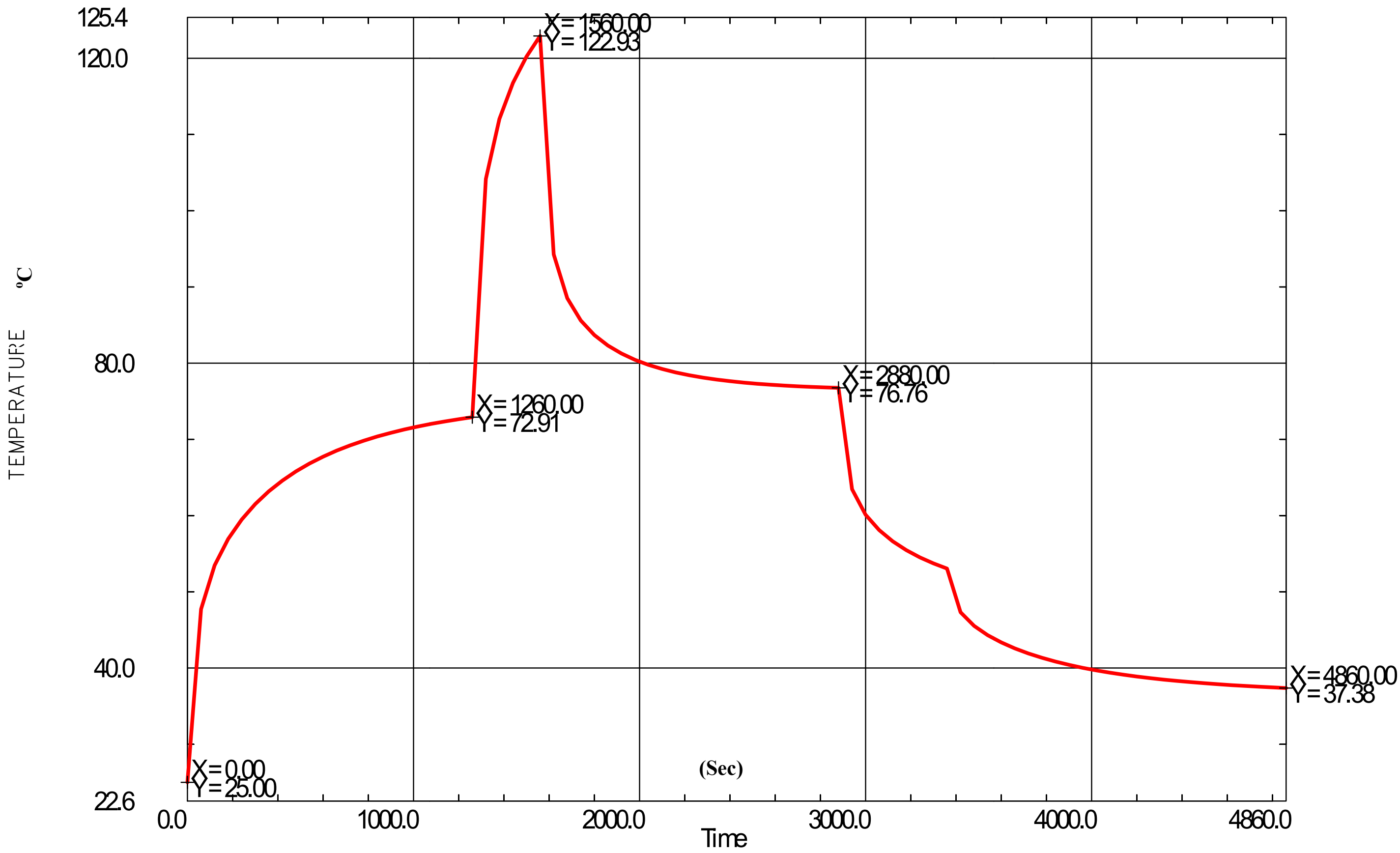

Fig. 8 Temperature transients of RWR-80 resistor for case2

VI. CONCLUSIONS

1. Thermal analysis is carried out for the PCB assembly under study for steady state conditions and temperature distribution plots for components as well as PCB are presented in this paper.
2. Maximum component temperature 87.6^{o}C is predicted for RWR80 resistor component for case1 and it is observed that the temperatures for the PCB assembly are well within the temperature limits specified.
3. Temperature transients of the resistor over the specified time interval are also studied for two different thermal resistance values.
4. Peak temperature of RWR-80 resistor will be **190^{0}C** in case1 and **123^{0}C** in case2. Its temperature will exceed the specified limit against de-rated value for short duration (≈ 5min) in case1. This is acceptable as this happens only for a shorter duration. However, it is within specified temperature limit as compared to rated value (250^{0}C).

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Dielectric Reliability of Thin Gate Oxide in 180 nm CMOS Technology

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Abstract— This paper reports on assessment of the thin gate oxide (40-70 Å) reliability lifetime for 180 nm standard Complementary Metal-Oxide-Semiconductor (CMOS) process at SCL. The concept of accelerated life testing is used to extrapolate the stress data at use conditions using voltage, temperature and area acceleration models. The Time Dependent Dielectric Breakdown (TDDB) tests are performed using Reliability Test System on specially designed test structures of MOS capacitors fabricated at SCL. In present work, we discuss testing methodology, failure data analysis and estimation of lifetime of gate oxide for test structure of low voltage p-poly/n-well gate oxide capacitor with isolation edge (gois_isof_plv_a). Estimated lifetime for gate oxide is approximately 20 years which meets the typical reliability target of gate oxides in this thickness regime.

Index Terms— Dielectric Breakdown, TDDB, Accelerated Life testing, Weibull Statistic, MOS Capacitor

I. INTRODUCTION

Over the generations, Complementary Metal-Oxide-Semiconductor **(**CMOS) technology has been facing an increasing demand of higher transistor currents and speeds. This require more and more transistors to be fabricated in a given die area. As a result of this scaling, the gate oxide thickness has steadily been thinning which aggravates the problems associated with the reliability of gate dielectrics. High leakage currents and short channel effects are some of the major concerns in thin dielectric films such as SiO_2 used as gate oxide (GOX) in CMOS devices. Since electric fields in the gate oxide are expected to rise with scaling, the long-term reliability of thin oxides becomes an important concern in modern, deep-submicron processes [1-4]. In case of memory applications, such as storage capacitors, a dielectric failure can result in a loss of information due to its high sensitivity to even a small increase of leakage current from specified functional level. Oxide film failure over time at lower electric field (EF) intensity (conditions of practical use) is a major cause of failures in CMOS devices which is termed as Time Dependent Dielectric Breakdown (TDDB) [2].

The TDDB test intends to model the intrinsic behaviour of gate oxide for the technology being qualified. According to accelerated life testing concept, the time to breakdown (t_{BD}) measurements of test capacitors are performed at high stress voltages and temperatures and the lifetime under normal operating conditions is then projected. This reliability projection involves the extrapolation of the dielectric lifetime based on three major components:

area/statistic scaling, voltage scaling, and temperature scaling. At the same time, it is equally essential to have measurement methods which can give a measure of the dielectric reliability in a relatively short time. The Constant Voltage Stress (CVS) is one of the frequently used methods for the measurement of t_{BD} [5-6].

Use of accurate techniques, methodology and statistical data analysis for reliability evaluation and projection is critically important for the development of a highly reliable technology. The dielectric reliability assessment has several applications e.g. process development and Built-in-Reliability (BIR), process characterization & control and reliability screening/burn-in etc [2].

There are 2 major categories of the test structures for dielectric integrity assessment in CMOS devices: MOS Gate oxide Capacitors and Poly-dielectric-poly capacitors. Present study is done on a small sample size of MOS test capacitors to estimate the reliability lifetime of SiO_2 being used as gate oxide in SCL's 180 nm standard CMOS process. A detailed discussion on test methodology, data analysis and interpretation of results is presented in the paper.

II. THEORETICAL BACKGROUND

The statistics of the devices under test (DUTs) failure time due to gate oxide breakdown is described by Weibull statistics [2, 7]:

$$F(t) = 1 - \exp\left[-\left(t/t_{63.2}\right)^{\beta}\right] \quad (1)$$

The total cumulative failures (F(t)) versus failure time (t) data when fitted with Weibull statistics yields the characteristics life-time (time to failure for 63.2 % population, $t_{63.2}$) and the Weibull slope (β) values which are required for reliability estimation.

The major extrapolations required to estimate the lifetime of gate dielectric from accelerated test data are briefly described below [2, 7]:

A. Temperature Acceleration

For a given stress voltage, the temperature dependence of t_{BD} is given by Arrhenius model:

$$t_{BD} \sim \exp\left(E_a/k_B T\right) \quad (2)$$

Where E_a is the activation energy; k_B is Boltzmann constant. To calculate E_a, breakdown of test capacitors of same area and oxide thickness is studied for same stress voltage at different temperatures.

The temperature acceleration factor (AF_T) can be calculated using above model as:

$$AF_T = \left(\frac{t_{BD,T_{use}}}{t_{BD,T_{test}}}\right) = \exp\left(\frac{E_a}{k_B}\left[\frac{1}{T_{use}} - \frac{1}{T_{test}}\right]\right) \quad (3)$$

Here temperatures are in Kelvin.

B. Voltage Acceleration

To study the voltage dependence of t_{BD} we use voltage acceleration model, given as:

$$t_{BD} \sim \exp(-CV); \text{ C=constant} \quad (4)$$

In this case, the samples are tested at different stress voltages but same temperature to find the voltage coefficient C.

The voltage acceleration factor (AF_V) can be calculated using above model as:

$$AF_V = \left(\frac{t_{BD,V_{use}}}{t_{BD,V_{test}}}\right) = \exp(-C[V_{use} - V_{test}]) \quad (5)$$

C. Extrapolation to lower failure percentiles

Lifetime at higher failure probabilities (63.2%) are projected to lower ones (100 ppm) using Weibull distribution using following relation that requires estimation of Weibull slope (β):

$$\frac{t_{100ppm}}{t_{63.2\%}} = \left(\frac{\ln(1-F_{100ppm})}{\ln(1-F_{63.2})}\right)^{1/\beta} \approx 10^{-4/\beta} \quad (6)$$

Here $F_{63.2}$=0.632 and F_{100ppm}=$F_{0.01\%}$= 0.0001.

D. Area Scaling

Area of the tested oxides is different than area of the gate oxide being qualified. Extrapolation for this is done using the following relation, which also requires estimation of Weibull slope:

$$\frac{t(A_{test})}{t(A_{use})} = \left(\frac{A_{use}}{A_{test}}\right)^{1/\beta} \quad (7)$$

The dielectric breakdown lifetime at use conditions; t_{use} is thus obtained by projecting the accelerated stress data to use conditions using the corresponding acceleration factors and is given by:

$$t_{BD,use} = t_{BD,test}\, AF_V\, AF_T \left(\frac{A_{test}}{A_{use}}\right)^{1/\beta} \left[\frac{\ln(1-F_{use})}{\ln(1-F_{63.2\%})}\right]^{1/\beta} \quad (8)$$

III. EXPERIMENTAL DETAILS

For dielectric reliability estimation "gois_isof_plv_a" test structure fabricated in SCL's 180 nm CMOS fabline was chosen. The test structure represents p-poly/n-well GOX capacitor with isolation edge. The test structure consists of an array of 9 unit capacitors, each with total area=2376 μm^2 and perimeter=21916 µm. Each one of these unit capacitors is treated as one DUT for present study. The test structure is packaged in 28 pin dual in-line packages (DIP) with 4 DUTs in each 28-pin DIP to perform TDDB testing using Cascade Microtech's Reliability Test System (Model 1164) at R&QA, SCL. The TDDB DUT board of reliability test system has total 16 sockets with provision of testing 4 DUTs in each socket, thereby testing total of 64 DUTs simultaneously in a single DUT board. All the tests were performed in controlled stress conditions as dictated in JEDEC standard (JEP001A: Foundry Process Qualification Guidelines) [7].

The TDDB tests were done at three different stress voltages viz. -3.6 V, -3.8 V and -4.0 V and constant temperature of 100° C to find the voltage coefficient (C) and three different stress temperatures viz. 100°, 110°, 125° C at constant voltage of -3.8 V to determine the activation energy (E_a) of dielectric breakdown. 20 DUTs for each stress condition were tested to find the statistical distribution of the observed data of time to breakdown for each set of stress conditions. Thus, a total of 20×5=100 DUTs were used to determine various acceleration factors from all stress conditions.

Following test procedure is used to measure the time to breakdown of DUTs [7]:

1. Initial screening/DUT verification is performed at 1.8 V to select good "unstressed" devices with controlled leakage currents.
2. During the stress cycle the device is biased using the selected stress bias conditions.
3. While stress, continuous monitoring of leakage current is done to find the percentage change in the Stress Induced Leakage Current (SILC) with respect to last reading; as the change exceeds 40% (End of Test: EOT condition), the device is considered to be failed and the test on the particular structure is stopped by program.
4. The time when the test stops at EOT is recorded as time to breakdown for the respective DUT.

IV. RESULTS & DISCUSSION

Figure 1 shows stress induced leakage current (SILC) versus stress time for one of the 20 DUTs tested at 100ºC and -3.6 V. The time to breakdown is marked when there is an abrupt increase (>40% from previous value) in leakage current. The typical time for DUTs to undergo dielectric breakdown, when tested at different stress conditions used in this experiment, ranges from few minutes to about a month.

At a given stress condition, the time to breakdown for all 20 DUTs is measured. The data are then ranked with median ranking [=(i-0.3)/(n+0.4)] to find the cumulative failures function F(t). Here, i represents the order number of the data and n represents the total number of DUTs. The Weibull slope (β) and characteristic time ($t_{63.2}$) are obtained respectively from the slope and intercept values of the linear plot of Weibit function (=ln{-ln[1-F(t)]}) versus ln(t_{BD}) using eq. (1).

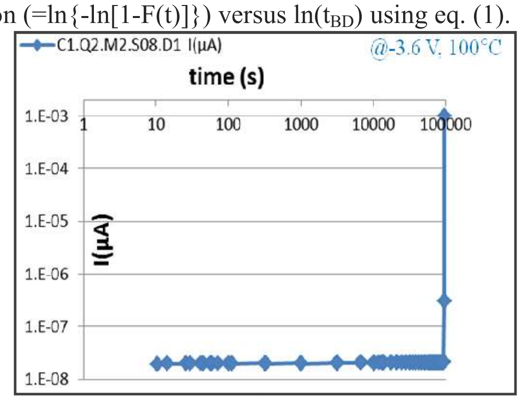

Fig 1 Leakage current versus stress time graph for a DUT at breakdown

Figure 2 shows the Weibull graphs for three different stress voltages and a given stress temperature. The linear fit to each stress data reflects that failures in the gate oxide being tested follow Weibull statistical distribution function.

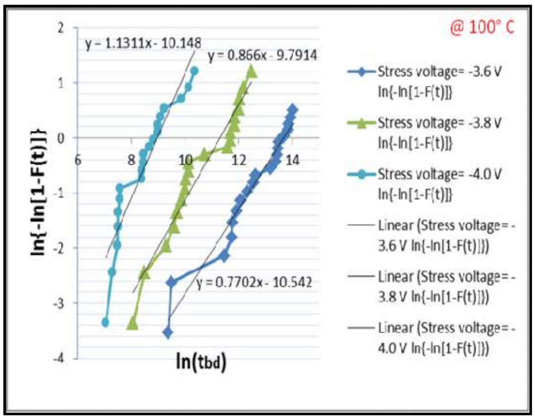

Fig 2 Weibull graphs for different stress voltages at constant stress temperature

A linear fit to characteristic lifetimes ($t_{63.2}$) at different stress voltages versus stress voltages (same temperature) confirms the voltage acceleration model (eq. 4) as shown in fig. 3. From this voltage acceleration model, the voltage coefficient (C) and voltage acceleration factor (AF_V) are estimated to be 11.8 and 1.8×10^{11}.

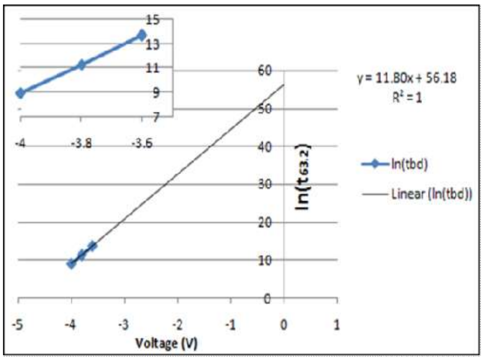

Fig 3 Verification of voltage acceleration model

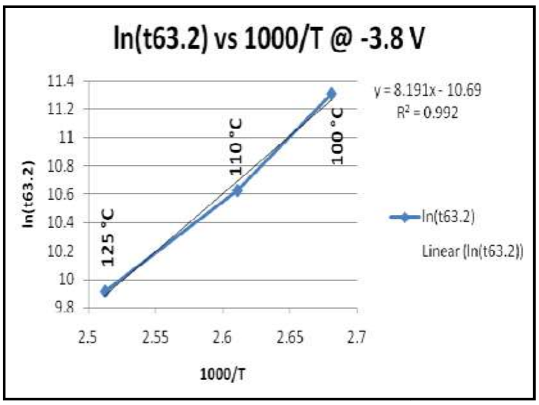

Fig 4 Verification of temperature acceleration model

The temperature acceleration model (eq. 2) is verified by linearly fitting the characteristic lifetimes ($t_{63.2}$) at different stress temperatures versus stress temperature (same voltage). This is shown in fig. 4. The slope of this plot gives the activation energy (E_a) of the dielectric breakdown and is estimated to be 0.7 eV. The reliability lifetime at normal operating conditions (-1.8V, 100º C) is projected from the stress data at -4V, 100º C using following projection scheme:

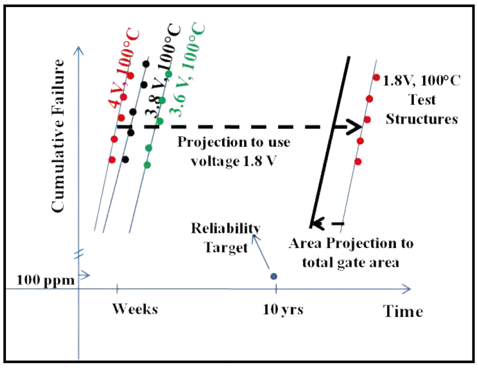

Fig 5 Schematic representation of dielectric lifetime projection from accelerated stress data to use conditions

Therefore, the area and percentile scaling factors as required in eq. (8) are calculated by taking β=1.131 (Weibull slope for -4 V, 100º C). The values of area and percentile scaling factors are respectively 4.78×10^{-3} and 8.841×10^{-5}.Having determined all the required parameters, the reliability lifetime at normal operating conditions (-1.8V, 100º C) is estimated from eq. (8) as:

$$t_{BD,use} = t_{BD,4V/100C} AF_V \left(\frac{A_{test}}{A_{use}}\right)^{1/\beta} \left[\frac{\ln(1-F_{use})}{\ln(1-F_{63.2\%})}\right]^{1/\beta}$$

$$= 7828.4\times1.88\times10^{11}\times4.782\times10^{-3}\times8.841\times10^{-5}s$$
$$= 6.22\times10^{8}s = 19.7\,years$$

The typical reliability lifetime target of gate oxide with total gate area of 1 mm^2 and 100 ppm total failures at 100º C, 1.8 V is 10-20 years. Therefore, the estimated lifetime of 19.7 years for gate oxide from “gois_isof_plv_a” test structure is meeting the reliability target for gate oxides in thickness regime of 40-70 Å.

V. CONCLUSION

The time-to-breakdown distributions for the DUTs under study are found to follow the Weibull statistics at different stress conditions. The voltage and temperature acceleration models are verified and corresponding acceleration factors are determined. The estimated breakdown activation energy is 0.7 eV which lies in range 0.6-1.0 eV reported in literature. Further the estimated dielectric lifetime as projected from highly accelerated stress conditions to use conditions is 19.7 years. The reliability lifetime estimated for the selected test structure meets the typical reliability target of 10-20 years for total gate area of 1mm^2 and 100 ppm total failures at 100º C, 1.8 V for gate oxides in thickness regime of 40-70 Å. However, since the present study was done on a small sample size, the results are only indicative. A large sample size and test structures with different design rules are required to be tested to qualify the process.

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Asymmetric High Performance Three-stage Cross-field Depressed Collector for Space TWTs

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Abstract — A high performance three-stage depressed collector has been designed to be used in space travelling wave tubes. The high performance has been achieved by introducing electrical asymmetricity and cross-field (electrical and magnetic fields are perpendicular to each other) within the collector. The asymmetricity has been attained by using few half-cylinder electrodes. Further, radially magnetized external ring magnet has been used to create the cross magnetic field and thereby to potentially minimize the back-streaming of electrons. Due to the combined effect of asymmetricity and the cross-field action, it offers high collector efficiency ~ 90% and low back-streaming with just three-stages itself.

Keywords— depressed collector, asymmetry, high performance, high collector efficiency, low back-streaming, space TWT;

I. INTRODUCTION

Travelling wave tubes (TWTs) are broadband microwave amplifiers being extensively used in strategic, military and civilian sectors. TWTs specifically used for satellite communication are known as space TWTs and they have several special space constraints to be met. Space TWT has to possess (i) highly efficiency, (ii) compact size, (iii) less weight, (iv) high linearity, (v) high reliability, (vi) long life [1] – [4]. In order to meet these space requirements, a high performance collector along with small size and less weight is needed [5].

Some of the space constraints are contradictory in nature demanding compromise to be reached. As the number of stages of depression in the collector is increased, the collector efficiency increases linearly till four. Beyond four stages, increase in collector efficiency is not very prominent (just ~1%). Rather, when the length of the collector increases more number of power supply modules are required for each additional electrode, thereby increasing both the size and weight of the collector, in turn. Hence, a compromise has to be made between efficiency requirements and size, weight constraints.

In a previous work, authors had proposed an asymmetric cross-field collector with very high collector efficiency ~95% for space applications [6]. But, the major limitation with that proposed collector had been in number of power supply modules required. As each half cylinder has been held at different potential to ensure better sorting of electrons, very high collector efficiency had been achieved but at the expense of increased weight and complexity, making it infeasible to be used for space applications.

Attempts to reach a compromise between collector efficiency and weight, size, complexity issues have resulted in the current three-stage asymmetric cross-field collector. Though collector efficiency has been sacrificed little bit, the power supply modules required has been reduced from eight to three – a huge saving in terms of weight, size and complexity.

II. MODELING

The high performance three-stage asymmetric cross-field collector has been designed for Ku band 140W space TWT which (under development at CSIR-CEERI with the sponsorship from ISRO-SAC) [7]. It modeled using CST particle studio [8]. The cut-view of the collector is shown in fig. 1. The collector consists of four cylinders with conically tapered tip, of which two are half-cylinders (cut along the axial direction). The geometry and potentials of the electrodes have been optimized for the high collector efficiency and low back-streaming current.

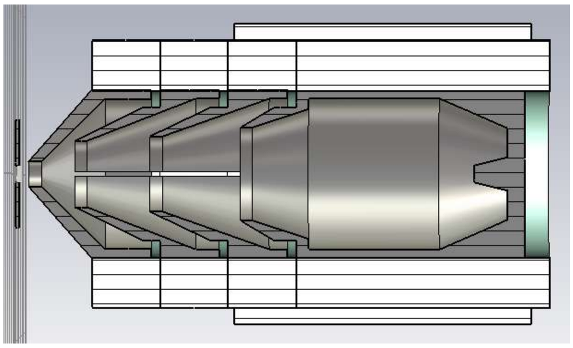


Fig. 1. Cut-view of the collector showing electrodes, ceramics and external ring magnet

The magnetic field is applied by the external radially magnetized ring magnet (fig. 2). The required magnetic field at the axis has been optimized for better performance. It has been found that remnant flux of 0.11T on the ring magnet provide the optimal performance. The 3D model of the collector shows that the second and third cylinders are axially cut into two halves with different potentials applied to each half-cylinder (fig. 3).

The first cylinder and second lower half-cylinder are applied a potential of 1500V. The second upper half-cylinder and third lower half-cylinder are applied a potential of 850V. The third upper half-cylinder and fourth cylinder are applied a potential of 680V. The potential distribution corresponding to these applied potentials (fig. 4) clearly depicts the electric asymmetricity introduced by the middle half-cylinders.

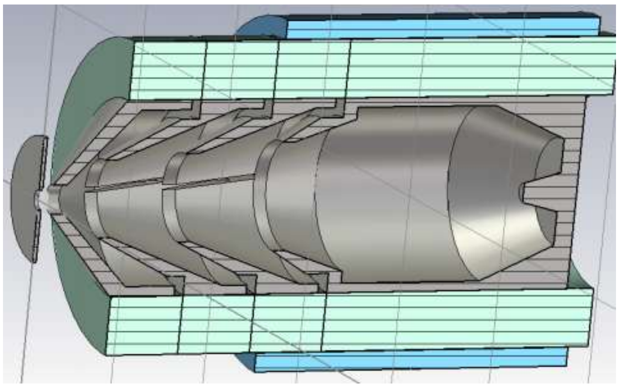


Fig. 2. Slant cross-sectional view of the collector

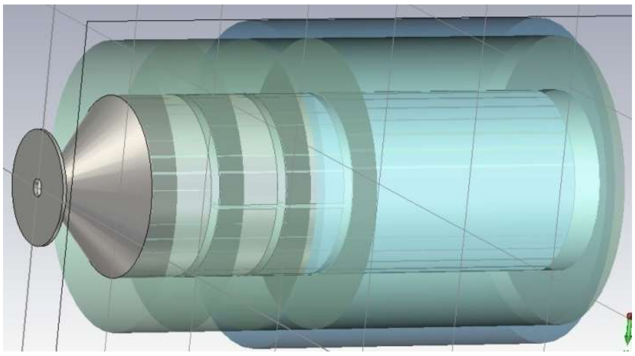
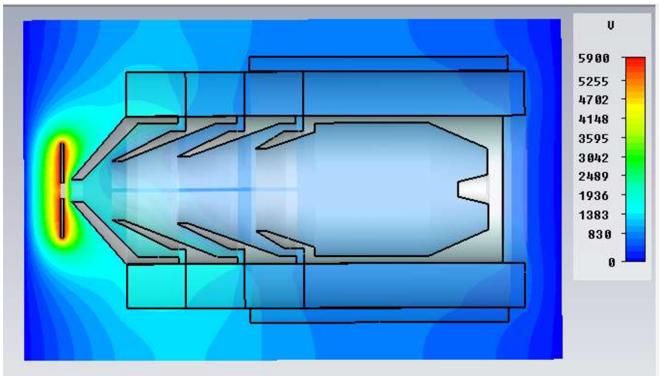


Fig. 3. 3D model of the collector showing half-cylinder electrodes (in second and third positions)



Potential distribution within the collector showing eqipotential regions

III. RESULTS AND DISCUSSIONS

The primary and secondary electron trajectories within the collector are shown for the saturated power output condition, in fig. 5 and 6 respectively. In these simulation, the electrode material is assumed to be made of OFHC (oxygen-free high-conductivity) copper with the secondary electron emission coefficient of 1.2.

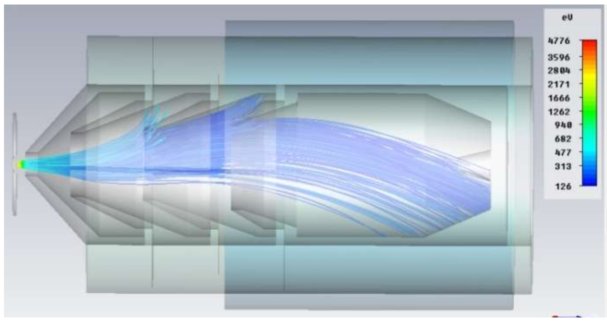


Fig. 4. Primary electron trajectories within the collector

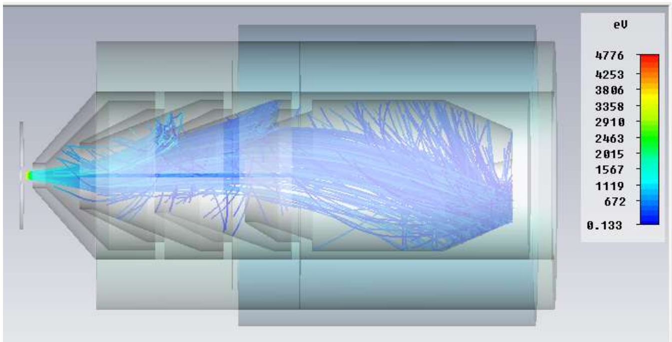


Fig. 5. Primary and secondary electron trajectories within the collector

It can be observed that most of the electrons hit the lower part of the collector. This is intentionally done so that better thermal dissipation of the waste heat will be possible as the lower part will be directly in contact with the convection cooled base-plate.

The comparison of the performance of the collector with other collectors have been summarized in table I, ignoring the effect of secondary electrons. The proposed three-stage collector yields 2% more collector efficiency as compared its symmetric (with full-cylinder electrodes) counterpart with four-stage depression. However, a degradation of ~4.7% collector efficiency has been observed with its eight-stage asymmetric counterpart. But, this compromise has to be done in order to make the collector feasible for space applications.

TABLE I. PERFORMANCE COMPARISON

Parameter	Symmetric four-stage collector	Asymmetric eight-stage collector [2]	Asymmetric three-stage collector (proposed)
Collector Efficiency (%)	88.63 %	95.53 %	90.78 %
Back-streaming current (mA)	1.60	0.00	0.00
Bod current (mA)	0.00	0.00	0.00

IV. ACKNOWLEDGMENT

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Challenges Encountered During Realization Of Hybrid Microcircuits For Space Applications

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Abstract— Hybrid Microcircuits (HMCs) are extensively used in Space Applications due to high reliability, reduced size, weight and volume. High reliability is achieved due to fewer interconnections, fewer intermetallic interfaces, usage of batch processed resistors, better immunity to shock & vibration. HMCs form an essential part of all spacecraft subsystems including Power Systems, Control Systems, Inertial Reference Unit, Digital Systems, Communication Systems, Sensor Electronics.HMCs employ fabrication processes comprising of thick film printing, die attachment, substrate attachment, die to substrate / substrate to package wire bonding and package sealing. HMCs are required to undergo exhaustive qualification prior to usage in Space. These HMCs are realized from the facility line which is Line Certified and Line Qualified as per ISRO standard "ISRO-PAS-206" - Qualification requirements for Thick Film Hybrid Microcircuits". Each new HMC undergoes product qualification comprising of Mechanical, Environmental and Endurance tests. Each batch of a qualified HMC which is fabricated with identified in-process checks undergoes 100% Screening. During the course of product qualification/ screening of HMCs, several observations/ challenges are encountered. This paper summarizes three case studies detailing the challenges faced during realization of HMCs. These case studies cover issues observed as Hermetic Package Failure, Electrical Deviations in DC-DC Converter HMC and Metallization Peel off in Multilayer HMC.

This paper also details the corrective measures taken and improvements made in the procurement specifications, fabrication process and acceptance testing methodology to overcome and prevent such observations in future.

Index Terms—Hybrid Microcircuits, Lot Acceptance Tests, Converter Stability, Metallization Peel off, Test Methodology

I. INTRODUCTION

Hybrid Microcircuits are circuits in which chip devices of various functions are electrically interconnected on an insulating substrate on which conductors & resistors have previously been deposited. These chip devices could be active, passive. Conductor and resistors are deposited using thick film printing process.

Each HMC part is critically selected/tested and qualified to meet space application requirement. Package is the first choice made in selecting HMC parts. Packaging provides defined external lead configuration and standard shape to facilitate assembly & testing along with providing adequate environmental, thermal and mechanical protection. A package should be carefully selected with respect to basic requirements as construction, size, material, number of pins before finalizing for production. HMCs are required to undergo or meet stringent requirements for usage in space application. The philosophy adopted for qualification of HMC for space application is explained as below.

II. HMC QUALIFICATION PHILOSOPHY

Hybrid Microcircuits are realized from the facility line which is Line Certified and Line Qualified as per ISRO-PAS-206 "Qualification requirements for Thick Film Hybrid Microcircuits". All the materials and components which are used in the fabrication of HMCs undergo Lot Acceptance Test (LAT). Every new HMC design is subjected to Circuit Type Qualification prior to usage for Flight Model (FM).

All HMCs used for FM are 100% Screened. The typical tests HMC is subjected during screening/Circuit type Qualification include Stabilization Bake, Temperature Cycling, Particle Impact Noise Detection, Constant Acceleration, Mechanical Shock/Vibration, Burn-in, Active Temperature Cycling, Electrical Verification, Seal leak tests, Mechanical/ Environmental / Thermovaccum/ Endurance tests viz. Operating life test and High temperature storage test.

For all the qualified HMCs, Derating Analysis requirements are met. Thermal Analysis requirements are met for high power HMCs. Layouts are inspected and these meet the layout requirements. Performance on proto for each HMC at temperature extremes is verified and approval is provided. Typical HMC internal diagram is as per Figure1.

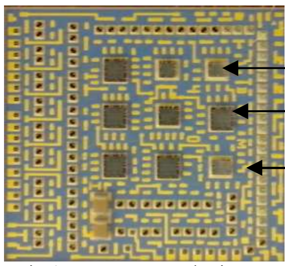

Fig 1 : HMC Internal Diagram

This paper discusses the challenges encountered during realization of HMCs. Corrective measures / improvements made in specifications, process and testing are also discussed. Following three case studies are considered: Case Study 1: Manufacturing defect in HMC package resulting in loss of package hermeticity. Detailed analysis of the failure is discussed and improvements made in test methods are discussed. Case Study 2: Electrical deviation as oscillations in DC-DC Converter HMC due to marginal value of selectable chip resistor. Detailed study carried out to pin point the root cause of oscillations is discussed. Also improvement made in the test method is discussed. Case Study 3: Analysis of thick film conductor metallization peel off and improvements made in the printing process are discussed.

III. CASE STUDIES

Three case studies are as discussed below:

a. Case 1 Hermetic Package failure

Hermeticity is effectiveness of the sealed package to prevent entry of moisture, oxygen and other ambient contaminants. These are detrimental to HMC reliability in long term as these may result in corrosion, dendrite growth etc. Entrapped material may also deposit onto the active surfaces resulting in HMC malfunctioning. A package is considered Hermetic for space applications if it meets the minimum leak rates of less than 5 X 10^{-8} atmcm^3/sec as established in Test Method Number 1014 of MIL-STD-883 Test Method Standard for Microelectronics. Seal leak failures observed in one of the HMC package involving brazing process are discussed here.

i. Package Construction

The package structure typically consists of Molybdenum base & Kovar ring frame and is used for realization of Power HMCs.Molybdenum is used as a base due to its good thermal dissipation property. Molybdenum base is joined to Kovar ring frame using brazing process. Brazing is a metal-joining process whereby a filler metal is heated above melting point and distributed between two or more close-fitting parts by capillary action. Filler metals are generally alloys of silver, aluminium, gold, copper, cobalt or nickel. A good braze joint is supposed to have uniform flow of braze filler between the base materials. Figure 2 depicts the package construction.

There are two lugs with six mounting holes provided on both the sides of the package for mounting the HMC onto the required base. Guidelines for mounting this package while

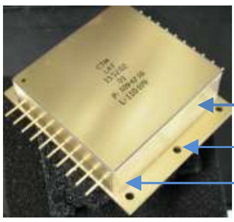

Fig 2 : Package Construction

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One Batch of Power HMC packages failed to meet the seal leak requirements post screening. Visual inspection carried out on these packages revealed crack at the package braze joint. Figure 3 shows the braze joint crack.

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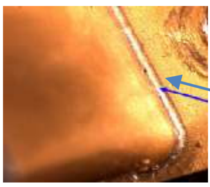

Fig 3: Braze joint crack

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a) This HMC undergoes Mechanical Shock test during screening wherein the HMC is mounted on to the shock test fixture through lugs provided on two sides of the package.

- Approved guidelines were followed for mounting the HMC onto the shock test fixture but details were not logged.
- Flatness and mapping response of the shock test fixture was verified and was found satisfactory.
- Improper torquing could have stressed the braze joint and would have resulted in seal leak failures. Hence simulation tests were carried out on dummy packages with different torquing sequences as zigzag torquing and regular torquing followed by shock test (1000g Shock Response Spectrum – SRS, 5 pulses), visual inspection and seal leak test. These samples passed the seal leak test.

b) Hence failure due improper torquing /mounting onto shock test fixture for these HMCs was ruled out.

- Package lot integrity

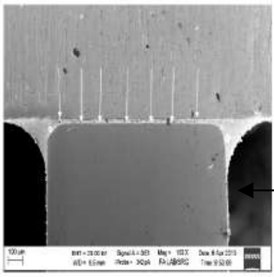
c) These failures were observed in new lot of packages which was used for realisation of this HMC.This lot had successfully undergone Lot Acceptance Tests (LAT) consisting of mechanical/environmental tests. Below said analysis was conducted to assess the lot integrity:

- Two LAT samples were subjected to post shock seal leak test and these met the seal leak requirements.
- Flatness measurement for the failed HMC package base was carried out using 3-Dimensional Co-ordinate measuring machine and the value was observed between 70-90 microns at the edges against the acceptable limit of 50 microns. This value was compared with packages from old lot wherein the observed flatness value was maximum 20 microns.
- One bare package from this lot was drawn and was subjected to flatness measurement. Observed value was between 20-60 microns from centre to edges. In order to study the effect of torquing on package flatness & braze joint integrity, this sample was torqued as per standard procedure for 24 hours. This sample met post torquing visual inspection/seal leak requirements.
- Weight simulation of this sample and torquing for 24 hours revealed crack at the braze joint. This sample met seal leak test requirements.
- Flatness measurement was carried out for all the screened samples from the lot and the maximum value was observed as 130 microns against the acceptable limit of 50 microns.
- When subjected to vibration test, the sample with worst flatness value of 130 microns met seal leak test requirements post vibration.
- A piece of package was cut from each lot (failed and old good lot) to verify the braze joint integrity. The packages were cross-sectioned in such a way that the braze joint is preserved.
- EDAX (Energy Dispersive X-Ray) and SEM (Scanning Electron Microscope) analysis was carried out on cross sectional portion of the braze joint for each of the cut pieces to identify the elements present.EDAX analysis revealed presence of Gold (Au) and Germanium (Ge) elements.

- SEM analysis revealed that braze material flow was not continuous from one side of the joint to the other side for failed lot. Continuous material flow was observed for the good package lot. Braze joint material coverage was good and uniform for good previous package lot while this was not the case with failed package lot.

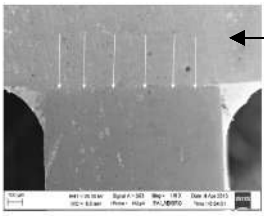
From the above analysis conducted, root cause of the failure is attributed to variations in the package base flatness and improper brazing process.

Figures 4 depicts good braze joint indicating continuous flow of braze material. Figure 5 shows defective braze joint with discontinuous material flow.



Continuous braze material

Figure 4: Good Braze joint

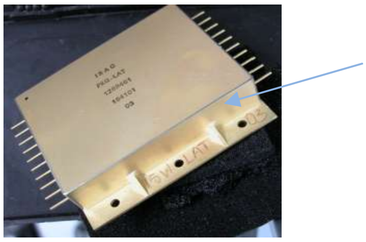


Discontinuous braze material

Figure 5: Defective Braze Joint

iii. Corrective Measures & Improvements

- All Power HMCs which failed to meet the requirements of Seal Leak test as per MIL-STD 883 Method 1014 were rejected for Flight usage.
- One assembled Power HMC which had worst flatness deviation was subjected to vibration test followed by seal leak and visual inspection. On successful completion of these tests, batches of HMCs which successfully completed screening tests were cleared for FM usage.
- Lot Acceptance Test methodology for packages with molybdenum base/ braze joint was modified to include
  - Flatness measurement on 100% basis and
  - EDAX/SEM analysis for verification of braze integrity on sample basis for each lot.
- Checklist is generated for logging shock test details including location wise HMC serial number, operator details, sequence of torquing. The checklist is signed by the operator and duly approved by the concerned supervising engineer.
- Package construction is changed to single mould for realization of subsequent power hybrids. Ribs are also provided on both sides for additional support as per Figure 6.



Ribs for additional support

Fig 6 : Single mould package

b. Case 2 Electrical deviations in DC-DC converter HMC

Medium Power DC-DC Converter HMCs are realized and qualified for space applications. Electrical testing of these converters include verification of parameters as output voltage, stability of output voltage, load/line regulation, cross regulation, current limit, short circuit, transient verification etc. DC-DC Converter HMC described in this case study is a Medium Power DC-DC Converter with power dissipation of 4.5W. This converter is also used for lower power applications of around 2.4W.

i. HMC Failure Details & Analysis

Stable DC output is one of the important requirement criteria for any DC-DC Converter. Stability is verified at 50%, 70%, 100% and 120% load conditions. There were oscillations observed in the few of the HMC batches during various stages of screening with voltage and frequency (20mV, 2.5 kHz) as per Figure 7. Oscillations were observed at 100% & 120% load conditions across all three outputs. These oscillations were remarkably seen in converters with higher power dissipation compared to low power ones. Below said analysis was conducted to understand the root cause of this observation:

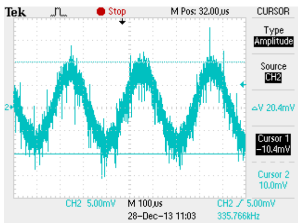


Fig 7: Oscillations in HMC output

- Verification of selectable resistor

There is a selectable resistor in the converter for tuning the HMC output with respect to stability. The value of this selectable resistor as per design can be any value above 100 Ohm. Tuning can be done via RC (Resistor Capacitor) network.

- Selectable resistor value is decided while tuning the converter at substrate level i.e. before packaging.
- This selectable resistor is accessible for measurement across package pins of the HMC. Hence, value of this resistor was measured for all HMCs fabricated in that timeframe to understand repercussion of selectable resistor value on oscillations.

- It was observed that oscillations in these converters were observed for lower values of selectable resistor ≈ 100 Ohm.
- Also oscillations were observed for converters with maximum rated power dissipation of 4.5W. No oscillations were noted in low power converters with lower dissipation ≈ 2.4W.

- Test set up verification
  - Functional electrical test socket was verified with respect to electrical interconnections, component values and was found satisfactory.
  - Test set up followed during tuning of selectable resistor as well as for electrical testing of converter was studied and it was observed there was a 1 Ohm resistor connected in series with the current meter while checking the converter output. The test set up is as per figure 8.
  - This resistor was introduced to measure the exact /accurate current value. Converter with oscillations was tested with both the set ups and it was noted that introduction of extra 1 Ohm resistor resulted in inadequate tuning and dampening of the oscillations.

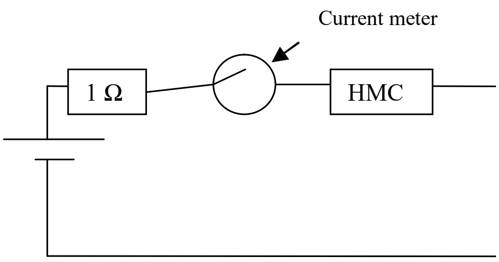


Fig 8 : Test set up used

Stability verification of the converters was carried out at 50%, 70%, 100% and 120% load regulation with one cross regulation combination. Output voltages are verified during Active Temperature Cycling at 100% load as part of screening.

- Performance Verification at temperature extremes

Performance of these converters was verified at temperature extremes of -30˚C to+65 ˚C. Some more converters which were working fine at ambient revealed oscillations at high temperature.

Root cause of these oscillations was due to usage of 1 Ohm resistor in the test set up as well as marginality in selection of selectable resistor at substrate level.

ii. Corrective Measures & Improvements

- Capacitor of value 1 Microfarad CKR style was connected across selectable resistor external to the HMC package and converters with oscillations were subjected to stability reverification at ambient as well as temperature extremes. No oscillations were observed.
- Hence, all these converters were cleared for Flight usage with external capacitor mounting with standard capacitor mounting method.
- Test Set up for tuning of selectable resistor or functional electrical testing of the HMC was finalized with connection of power supply to HMC supply via current meter. Figure 9 shows the improved test set up.
- Verification of converter stability for all output lines at all cross regulation conditions was introduced.
- Verification of converter performance was introduced at half and double of the selected resistor value prior to finalization to provide adequate margin.
- Verification of converter stability at 100% load for Active Temperature cycling test along with output voltage verification was introduced.

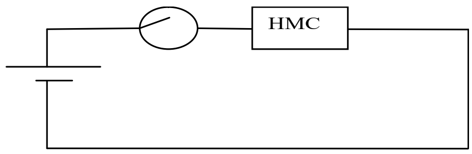


Fig 9: Improved test set up

No electrical deviations are reported during screening of subsequent batches after incorporating above said measures.

c. Case Study 3 Metallization Peel off in Multilayer HMC

Conductor Metallization peel off in Multilayer HMC resulting in non meeting of wire bond strength.

Multilayer printing involves printing of multiple conductor layers isolated by dielectric layer and interconnected through via fills in the dielectric as per HMC layout. Since there are multiple printing operations involved, uniformity in top layer is an essential requirement to ease wire bonding.

i. HMC Failure Details & Analysis

There was metallization peel off observed during pre-cap visual inspection in one of the HMCs. The wires corresponding to the peeled pads also failed to meet the Destructive Pull Test (DPT). This peel off is detrimental to the HMC wire bond strength and may result in complete functional loss to the HMC. Also non-uniform metallization was observed on wire bonding pads with a convex filling of vias. Figure 10 depicts typical metallization peel off observed in printed conductor.

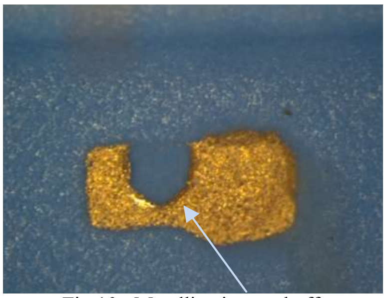


Fig 10 : Metallization peel off

To understand the root cause analysis as below was carried out.

- Thick film Conductor Paste

- HMC fabrication line was qualified for realization of Multilayer Printing using thick film conductor paste. Due to introduction of new material by the paste manufacturer the process was re-qualified using the same process steps as that followed for previous material.
- Visual inspection of the printed conductors in the failed samples revealed non-uniformity in the via fill pads and thinning of conductor metallization at the edges
- Also, it was observed that this new conductor paste is more porous compared to the earlier qualified one.

- Process
  - Process flow used multilayer printing was studied and no deviation was observed from the qualified process.It was verified that qualified equipments are used and qualified operators are only carrying out the process. The thickness of the emulsion used was 30 microns for gold conductor paste and 50 microns for dielectric paste. Firing was carried out with duration of 60 minutes.
  - Firing was carried out on dummy samples with firing duration as 30 minutes as an experiment. Less porous conductor were observed with a firing duration of 30 minutes. Firing profile is as provided in Figure 11.

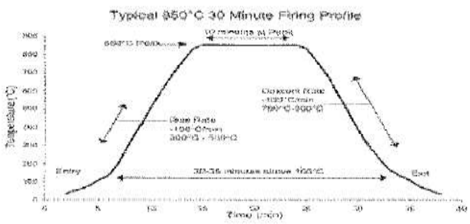


Fig 11: 30 minute firing profile

  - Printing sequence adopted for realizing this batch was 1st Conductor /1st dielectric/2nd dielectric/1st via fill followed by same sequence for second and third layers.
  - Experiments were conducted by modifying the existing printing sequence to 1st Conductor /1st dielectric/ 1st via fill/2nd dielectric/2nd via fill along with change of emulsion thickness to 15 microns. Uniformity in the via fill was observed with changed process sequence and modified emulsion thickness.

ii. Corrective Measures & Improvements

- The entire batch realized using this process was rejected for flight usage.
- Improvements were made in the printing process with respect to sequence of printing & also the thickness of emulsion.Firing profile of the conductor was changed to 30 minutes. This resulted in uniform metallization surface including the wire bonding pads and via fills. Sequence of printing for old process vs new process is given in Table 1.
- The new process with these process improvements was qualified and subsequently batches realized had no quality issues.

Table 1: Comparison of printing process sequence

Process Step no	**Earlier Process**	**New Process**
1	Conductor 1	Conductor 1
2	Dielectric 1	Dielectric 1
3	Dielectric 2	Via Fill 1
4	Via Fill 1	Dielectric 2
5	Conductor 2	Via Fill 2
6	Dielectric 2	Conductor 2
7	Dielectric 2	Dielectric 2

Failures discussed in this paper pertain to different areas related to HMC fabrication, HMC parts acceptance testing and HMC screening.

Improvements are made in the test methodologies for package acceptance, electrical evaluation. Improvements are also made in the fabrication process of Multilayer HMC. LAT for package with braze joint includes flatness measurement on total lot and verification of braze quality through micro sectioning/ EDAX & SEM analysis. Test set up for converter includes current meter directly connected to HMC supply input. Selectable resistor value is arrived at after verification of converter stability for half and double the value by providing adequate margin. Multilayer Printing Process sequence is changed with change of process sequence along with emulsion thickness and firing profile to meet quality requirements. Subsequent to the implementation of these improvements, there are no failures during screening.

ACKNOWLEDGMENT

Authors thankfully acknowledge the support and guidance received from Director, ISRO Satellite Centre for giving an excellent opportunity in bringing out this paper. Also, a special acknowledgment goes to Sri K.Venkatesh Group Director, Quality Assurance Group who guided us through the analysis. Authors also acknowledge team members from RAMD, PED, HMCD and Sri Aravindram, Engr MQAD for their valuable support.

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B

COTS FOR SPACE APPLICATIONS

Evaluation of Area Array CMOS Sensor for Indian Space Programs

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Abstract— Various types of Imaging Sensors (viz. Linear/Area Array CCDs, CMOS, TDI etc.) are being used in the Electro-Optical payloads for earth observation satellites. Development in E-O sensor technology has resulted in miniaturized and large format sensors. Increasing demand for new earth observation satellites with extended features and less development cost and time, requires selection of state of the art imaging sensors available off the shelf. Evaluation of space worthiness of these detectors is essential to ensure failure free onboard operation. First criteria for selection is based on E-O performance and secondly their ability to operate in space environment. The subject detector is a 4.2 Mega Pixel area array CMOS detector. This sensor is selected for its features like; large format with small pixel size, small package size, less power and weight. Exhaustive screening & qualification activities were carried out for evaluating the suitability of these commercial grade detectors to survive the harsh space environment. This includes tests based on MIL-883 and additional tests specific to the application environment. This paper describes the test plan followed for evaluation along with electrical & optical performance of these devices over the entire environmental tests.

IndexTerms—CMOS, Screening, Qualification, Stabilization Bake, Thermal Cycling, Burn-in, Life Test, Fine Leak Test, Sine Vibration, Constant Acceleration Test, Wire Bond Pull Test, Total Ionizing Dose (TID) Radiation Test.

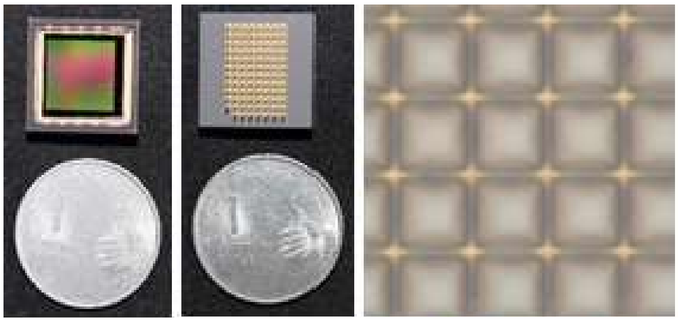
I. INTRODUCTION

With the advancement in technology, state of the art Imaging Sensors with advanced features like less weight and power and high pixel count are available in a very small package. One of these state of the art sensors meeting the required E-O performance was selected for use in current and future Earth Observation Satellites developed by Indian Space Research Organization. This is a large format (2Kx2K) area array CMOS Image Sensor available only in Commercial grade. Exhaustive activities were carried out for evaluating the suitability of these detectors to survive the harsh space environment. This includes Stabilization Bake, Thermal Cycling, Vibration Test, Accelerated Life Test etc. Integrity of these devices was evaluated by performing Visual Inspection, Leak Test & Electro-Optical Tests. Following sections describe the test plan for evaluation along with electrical & optical performance of these devices over the entire environmental tests.

II. DEVICE DETAILS

The selected detector is an industrial grade high speed CMOS image sensor with 2048X2048 pixels. The image array consists of 5.5x5.5µm2 pixels with global shutter feature which

allow exposure during read out, while performing CDS operation. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency. The whole sensor is packaged in ~19x19mm2 µPGA (90 pin) ceramic package and consumes only 600mW of power. Figure 1 shows the full device view and micro lenses deposited on pixels.



Front Rear Micro lens on Pixels

Fig. 1. Full Device View

III. SCREENING & QUALIFICATION

Nine available devices were screened as per MIL standards [1,2]. Stabilization bake, thermal cycling & burn-in were carried out as a part of screening. During each environmental tests, integrity of devices was evaluated by performing Visual Inspection, Fine Leak & Electro-Optical tests.

Three randomly selected devices from screened batch were subjected to extensive qualification tests under two different subgroups as given in Fig. 2. To evaluate any thermal and mechanical fatigue, one device was subjected to 100 Thermal Cycles followed by Sine Vibration Test under Subgroup-1. Under Subgroup-2, two devices were subjected to 2000 Hrs endurance life test at elevated temperature. Radiation tolerance of these devices was evaluated by subjecting all three devices from Subgroup-1 & 2 to Total Ionising Dose (TID) test. After successful completion of life test, one device was subjected to Constant Acceleration and

Wire Bond Pull test to evaluate the strength of die attach and wire bond.

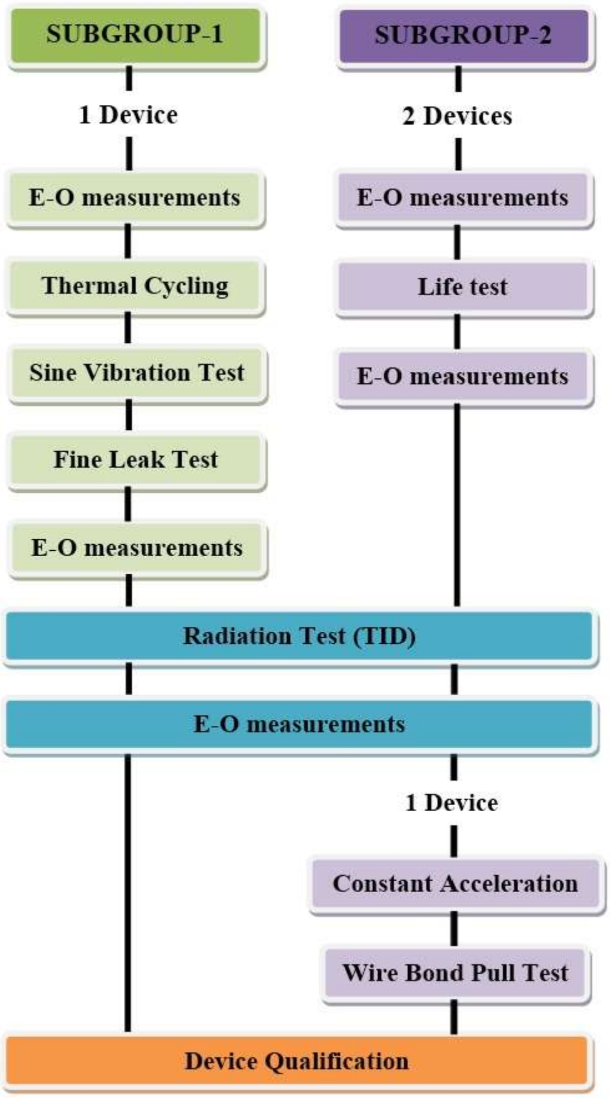


Fig. 2. Screening & Qualification Plan

Test setup and Burn-in Card used for Characterization and burn-in respectively was validated for consistency and repeatability before start of the Screening and Qualification activities.

IV. Measurement Results

A. Screening

As a part of screening, Electro-Optical measurement under Dark and Illumination was carried out for all devices at initial stage, pre burn-in and post burn-in. Parameter drift was calculated for pre to post burn-in measurements. Parameters measured were; Dark Offset, Dark Noise, Dark Current, Conversion Gain, Full Well Capacity, Signal to Noise Ratio (SNR) and RMS Non-Linearity. Figure 3 shows the drift in various parameters observed during pre to post measurements of 9 devices.

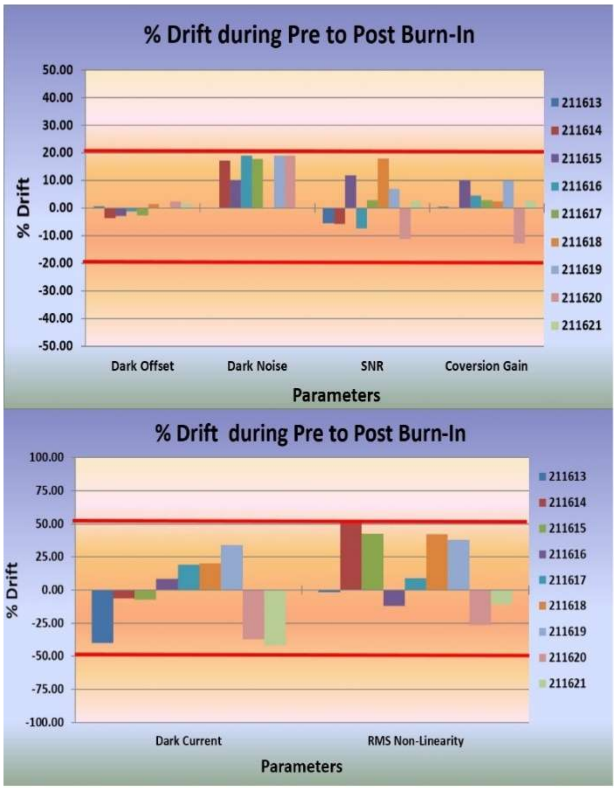


Fig. 3. Measured Drift during Screening

Drift in Dark Offset, Dark Noise, SNR & Conversion Gain was less than acceptable limit of ±20%, whereas, for Dark Current and RMS Non-Linearity it was less than acceptable limit of ±50%.

V. Qualification

Out of these nine devices, three were randomly selected for Qualification under two subgroups. Tests carried out under these subgroups are summarized in following sections.

A. Thermal Cycling:Evaluation for any thermal fatigue was evaluated by subjecting one device to 100 Thermal Cycles. Integrity of device was ensured by carrying out Visual Inspection, Fine Leak test and Electro-Optical measurements. Drift in pre to post measurement results of E-O parameters was calculated and as shown in Fig. 4. Drift in parameters due to thermal cycling was within acceptable limits and passed in Visual Inspection and Fine Leak test.

B. Sine Vibration:After successful completion of Thermal Cycling, this device was subjected to Sine Vibration Test to evaluate any Mechanical Fatigue. Figure5 shows the drift in parameters measured during pre and post vibration test. As can be seen from the plot all drifts are within acceptable limit.

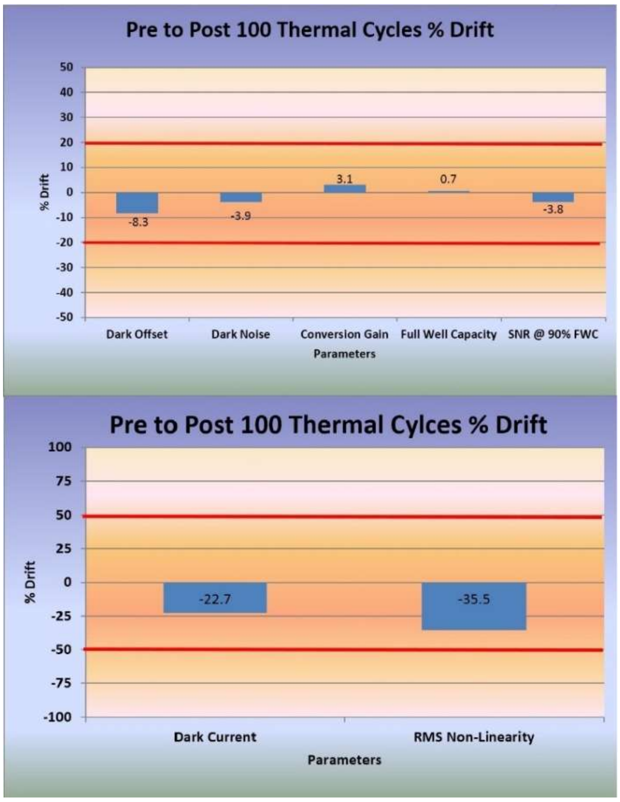


Fig. 4. Measured Drift during Qualification Thermal Cycling

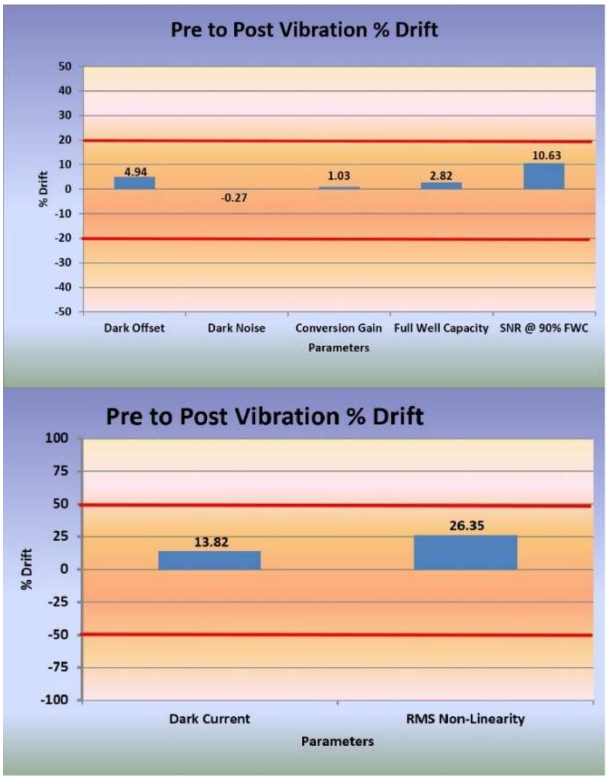


Fig. 5. Measured Drift during Qualification Sine Vibration Test

C. Life Test:Two devices were subjected to 2000 hours life test at elevated temperature. Figure6 shows the drift in parameters measured before/after life test. All parameters were within acceptable limit.

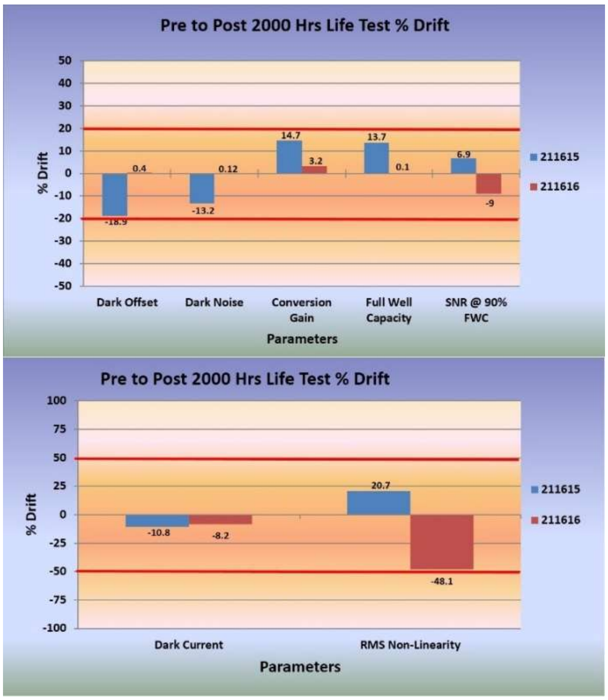


Fig. 6. Measured Drift during Qualification Life Test

D. Radiation Test:All three devices of above two subgroups were subjected to Total Ionising Dose test. A customized setup was developed to power the devices during radiation exposure. The detector was mounted on a card having limited number of passive components and was put inside the radiation chamber. The required bias was supplied from low noise power supply and clocks were fed through a custom developed card placed outside the chamber. This configuration prevents the active components from being exposed to radiation. During radiation exposure power supply current was continuously monitored. Post exposure dark measurement was carried out. First device was exposed up to 20 Krad in steps of 1, 3, 5, 7, 10, 15 and 20 Krad. After 20 Krad exposure device was subjected to annealing. Second device was exposed up to 150 Krad in steps of 5,10, 20, 30, 50, 70, 100 and 150 Krad. After 150 Krad exposure device was subjected to annealing. Whereas, third device was exposed up to 150 Krad in steps of 1, 3, 5, 7, 10, 15, 20, 30, 40, 50, 100, 125 and 150 Krad. After 150 Krad exposure device was subjected to annealing. Drift in measured parameters with exposed radiation dose is summarized in plots as shown in Fig. 7, 8 and 9. Up to 100 Krad no degradation was observed on second device. After 150 Krad exposure, bright line as shown in Fig. 10 was observed on Dark Image output of second

device.Same kind of pattern was observed on third device with increasing number of lines at 150 Krad as shown in Fig. 11.

From these results it was concluded that these devices are radiation tolerant up to 125 Krad exposure.

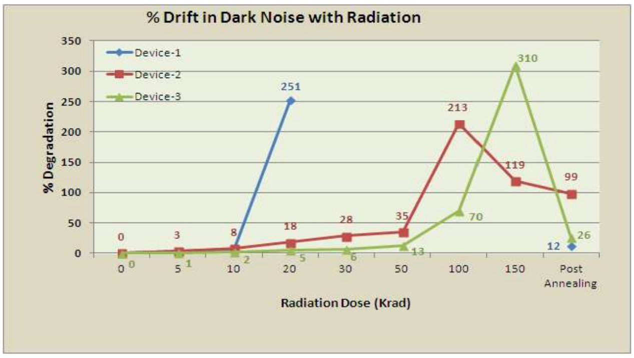


Fig. 7. Drift in Dark Noise with Radiation

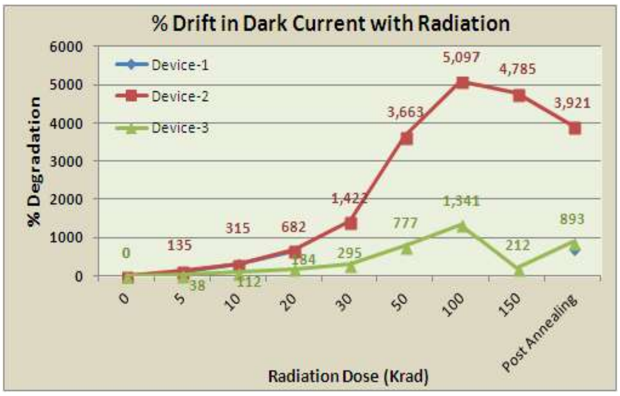


Fig. 8. Drift in Dark Current with Radiation

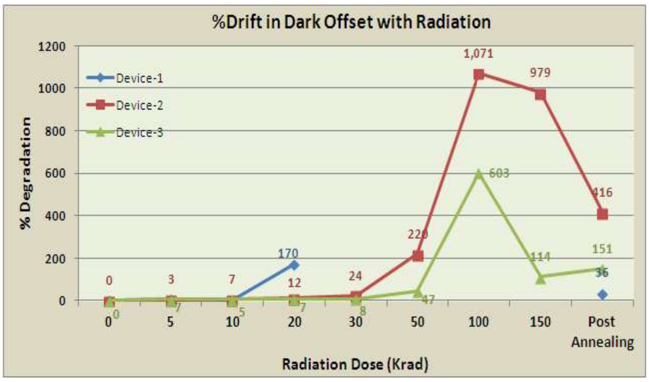


Fig. 9. Drift in Dark Offset with Radiation

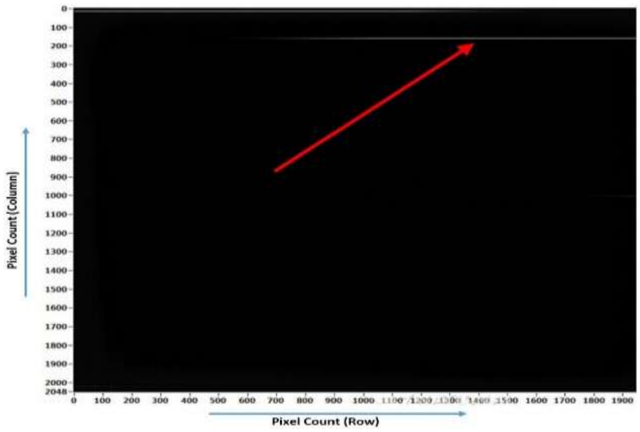


Fig. 10. Anomaly observed after 150 Krad exposure (Device-2)

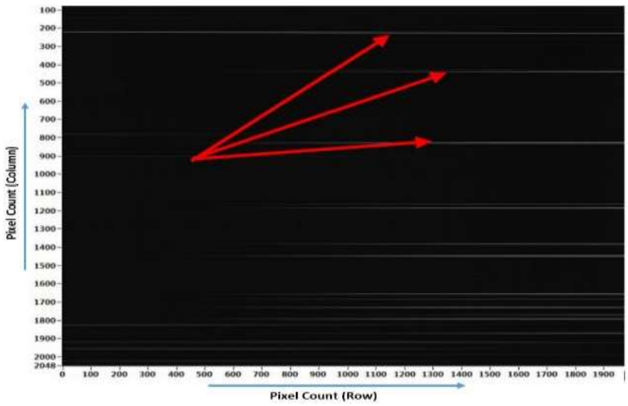


Fig. 11. Anomaly observed after 150 Krad exposure (Device-3)

E. Constant Acceleration Test:Constant acceleration test was carried out to evaluate the strength of die attachment. After radiation test one device was subjected to constant acceleration in steps of 3,000g, 5,000g & 10,000g in Y1 direction. Visual inspection was carried out after each level. Device has successfully passed the acceptable limit of 5000g. Post 10,000g constant acceleration, crack was observed on device package propagating from all corners to the centre of the device as shown in Fig. 12.

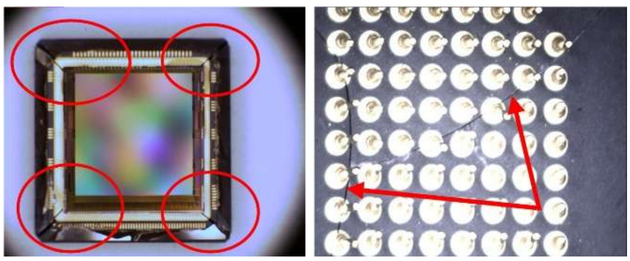


Fig. 12. Crack after Constant Acceleration Test

I. Wire Bond Pull Test:After Constant Acceleration, Bond Pull test was carried out on 22 bond wires. All bond wires had successfully passed the minimum requirement of 3gf for 1 mil Au wire.

VI. CONCLUSION

Devices have successfully gone through all tests during qualification. Based on their state of the art features and satisfactory performance during qualification exercise, devices are used in ongoing mission of ISRO and also planned for future missions.

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Experience during COTS Qualification

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Abstract- Commercial Off The Shelf (COTS) components are being increasingly used in various scientific and space programs due to the advantages ofstate-of-the-art (SOTA) technology. High Speed devices like Serializer/ deserializer, digitizers are available in COTS quality only. While COTS offer advantages in terms better performance, mass and volume, these devices have several issues related to reliability,consistent quality, environmental conditions etc. These devices do not have any traceability too and none or very little heritage. However, to meet the mission requirements several COTS are used in space after establishing the minimum R&QA requirements by selecting the COTS from the qualified and reputed vendors and thereafter rigorousupscreening. This paper describes the experiences during the COTS qualification at SAC.

COTS Peltier Thermoelectric Cooler (TEC), AFE have been used in MARS mission successfully. Besides these, mixed signal devices (ADC and DAC) are proposed for Chandrayan-2. The qualification of these mixed signal devices is in progress. Serializer/ deserializer (SerDes) has been proposed to be used in CARTO payload.

Keywords: COTS, reliability, Up-Screening, up-gradation, miniaturization

I-INTRODUCTION

Mostly MIL grade or ESA qualified components from QML certified vendors are used in space payloads. These Hi-rel devices are manufactured through the well qualified process and have good space heritage.
With State of the art performance, and advantagesin the terms of mass and volume, which are at premium for space payloads, COTS are being proposed for LEO orbit, scientific and experimental missions including deep space missions. The electronic components used in the payloads must perform in the harsh space environment. High temperature gradient, vacuumof the order of $<10^{-6}$Torr and radiation (TID & SEE) must not degrade the performance of electronic devices over the mission life.

Improvement in technology day by day improves product performance, higher gate density, lower supply voltage requirement, and lower mass and volume. Most of COTS are Plastic Encapsulated Microcircuits (PEM). The production cost of majority of COTS is significantly low due to non-hermetic packages, higher production volume and low material cost.

II-MAJOR ISSUES

A. Electrical

The core operating voltage has reduced to 1.3V. Subsequently the reduced voltage margins have raised the reliability concern.

B. Defects

The qualified parts are manufactured through matured and qualified process. These devices are also source screened before use in space program. Owing to qualified and well controlled processes, no defect is observed in qualified devices. In contrast, COTS are of SOTA, non-qualified processes and unscreened. So following defects could be observed in COTS

i. Thermomechanical defects: cracks anddelamination
ii. Die defects:semiconductor wafer fabricationdefects
iii. Package defects: voids, de-lamination, passivation cracks and metallization deformation
iv. Die attach defects: poor die-to-support adhesion, voids, inadequate filleting
v. Leadframe defects: overetching, skewedleads, bent leads, plating defects, solderability
vi. Wirebond defects: lift-off, contamination, shearing and fracture.

C. Failure Modes

The various failure modes are corrosion, popcorning, bondpad cratering, die cracking and metallization deformation.Hence a specific screening and qualification plan is required for such COTS devices, before incorporation into satellite payloads as they are non-retrievable and non-repairable.

III-SCREENING PLAN

The space payloads are not repairable. Any component failure may result in mission failure. Hence, it is mandatory that infant mortality is removed through the screening process. So,all the components used in the space program are 100% screened. The screening includes non- destructive tests. The screening plan has been defined Table-1.

Table-1: Screening Test Plan

Test No.	Test Name	Test Condition	MIL-STD-883 Test Method
1	External Visual		Method 2009
2	Serialization		
3	Stabilization Bake	24 hours at 150°C	Method 1008

Test No.	Test Name	Test Condition	MIL-STD-883 Test Method
4	Temperature Cycle	ConditionC, 20 cycles min.	Method 1010
5	X-ray/SAM Inspection		Method 2012 /2030
6	Pre burn-in Electrical	As per device spec. at 25°C	
7	Dynamic Burn-in	Min. 450 hours 105°C	Method 1015
8	Post Burn-in electrical	As per spec. at 25°C	
9	Percent Defective Allowable (PDA) calculation	5 percent (steps 7 to 9)	
10	External visual	Same as in step 1	Method 2009
11	Packing and storage	sealed in vapor barrier bags	

IV-QUALIFICATION PLAN

Qualification tests are destructive tests.These tests are carried out on samples selected from screened lot.The COTS used in Mars Orbital Mission (MOM) were configured to test in the application conditions and the type of tests were curtailed to meet the requirements.The card level qualification test plan is defined in Table-2. For COTS Qualification, following 5 subgroups were defined to detect all possible failure modes.

i. Construction Analysis Subgroup: defects due to workmanship of device assembly are detected.

ii. Radiation Subgroup:radiation sustainability of the device in the heavy energy particle environment is tested.

iii. Operating Life Subgroup: compliance to meet the mission life is tested

iv. Thermal Subgroup:all the thermal issues and package defects are detected.

v. HAST Subgroup: it is carried out specifically on PEM to accelerate and detect the defects like popcorning.

The detailed qualification plan has been tabulated in Table-3.

Table-2: Intensive Card Level Testing

No.	Test	Method/ Condition
1	Initial bench test	In Lab
2	Thermal cycling of the package/ PCB (PCB shall be subjected post-CC)	-20°C to 65°C, 25 cycles, 15 minutes each
3	Interim bench test	In Lab
4	Operational Temperature Test	24 hours each at -20ºC and +65ºC
5	Random Vibration	Qualification level as per ETLS
6	Sine Vibration	Qualification level as per ETLS
7	Thermo-vacuum	24 hours each at -20ºC and +65ºC
8	Final bench test	In Lab
9	Visual inspection of the package for device and soldering damage	As per ISRO-PAX-300
10	Life Test	2000 Hrs, at 70°C (may be extended upto 4000 hrs.)

Table-3: Qualification Test Plan

Test No.	Test Name	MIL-STD-883 or JESD-22 Test Method	Sample Qty.
1	External Visual	Method 2009/	23 (21 + 2 Control

Test No.	Test Name	MIL-STD-883 or JESD-22 Test Method	Sample Qty.
			sample)
2	Subgroup 1: Construction Analysis – Group A		6
2a	Resistance to Solvents	Method 2015	5
2b	X-Ray	Method 2012 (Die-mount & wire bond)	
2c	SAM	Method 2030	
2d	DPA & Micro sectioning	Method 5009	
2e	SEM	Method 2018	
2f	Out-gassing	Method 1034	1
3	Subgroup 2: Radiation Analysis		4
3a	Total Ionization Dose (TID)	Method 1019	2
3b	Single Event Latch-up & Upsets	ASTM F1192M-95	2
4	Subgroup 3: Operating Life Test		3 devices
4a	Life Test	Method 1005, Cond A, 3000 hrs at 70°C	3
4b	Electrical Test	As per device specification at 25°C	3
5	Subgroup 4: Thermal		5
5a	Temperature Cycling	Method 1010 Cond. C (-65°C to + 150°C), 500 cycles	
5b	Visual Inspection	Method 2009	
6	Subgroup 5		3
6a	HAST	As per JESD 22-A110, (500 hours, +105°C, 85% RH)	
6b	Visual Inspection	Method 2009	

V-CHALLENGES

Besides manufacturer datasheet, no other data is available for these COTS. The device performance over the time in extreme environmental conditions, radiation and electrical stress conditions are not available. The workmanship and manufacturing process of these devices are unknown too. Furthermore, no well-defined test philosophy is available as it depends on the mission and device technologies. A test philosophy was evolved to cater the mission requirements and available COTS devices.

AFE, Serializer/ Deserializer and TEC are highly complex devices. Understanding the technology and complexity of device, defining the test methodology, identifying the critical parameters, developing the screening and qualification test plans and designing the test setups are some of the challenging tasks carried out during the qualification process of these COTS.

VI-SCREENING AND QUALIFICATION OF COTS AT SAC

Following COTS have been screened and qualified:

i. Peltier Thermoelectric Cooler (TEC)-MAX1978
ii. Analog Front End (AFE)- AD9826
iii. Serializer- DS90UR241
iv. Deserializer- DS90UR124
v. ADC AD7492
vi. DAC AD5332

A. COTS used in MOM:

1) MAX1978

QFN-48 pin TEC is single chip temperature controller. Qualification was carried out on 3 samples which includes accumulated 30000 device hour life test. The reference voltage was the critical parameter. The acceptable drift is ±5% for parameter specification of 1.5V. All the devices exhibited measured reference value within the acceptable limit as shown in the Fig. 1

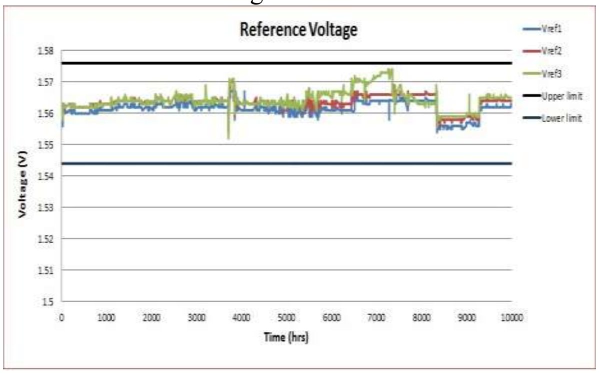

Fig. 1- TEC Reference Voltage

This device also met the Radiation (TID) requirement of 10Krad. As a part of SEE, single event latch-up test was carried out. Devices did not exhibit latch-up occurrence up to the tested LET of 50 MeV.cm2/mg. No degradation in device performance was observed during the qualification tests.

As can be seen from Fig. 2, during life test of 10000 hours, the input current IDVDD varies from 22mA to 27mA and output current IPDVDD varies from 359mA to 431mA (as defined in selected operating conditions). Datasheet specifications for these currents were 30mA and 3A respectively.

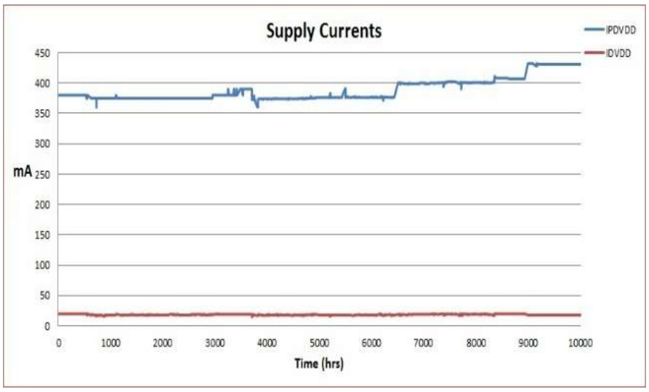

Fig. 2- TEC Life Test

2) AD9826

Qualification was carried out on 23 samples of 28-pins, SSOP packaged 3-channel CCD signal processor, including 30000 device hour accumulated life test. The device is meeting the project requirement of 10 KRadTID. However, devices exhibited latch-up occurrence even at LET of 10 MeV.cm^2/mg. Hence, the device was used with suitable mitigation in payload. No other performance degradation was observed during the qualification tests.

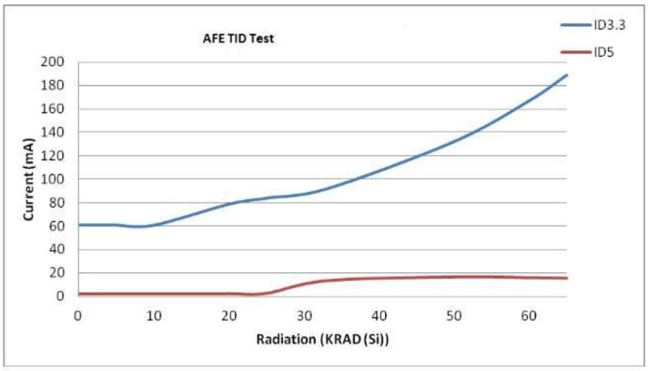

Fig. 3- AFE TID

From the Fig. 3, it is observed that degradation of supply current $I_{DD3.3}$starts after exposure of 10KRad and supply current ID5 after 20KRad.

B. COTS Proposed for Cartosat:

1) DS90UR241

2) DS90UR124

48-pins TQFN Serializer and 86-pins TQFN Deserializer were proposed to be used in Cartosat payloads. These devices are used in pair through LVDS transmission line. Besides supply currents and voltage levels, the PLL locking time, matching the transmitted and received data, Clock recovery and propagation time are some of the critical parameters identified for these devices. 30 samples of each type were subjected to Qualification tests. Accumulated life test of 20000 device-hours was carried out on 8 samples. After 1750 hours of operating life, failure was observed in two samples of serializer and one sample of deserializer. Dynamic drift behavior of the device after life test on 8 samples have been shown in the Fig. 4 & Fig. 5.

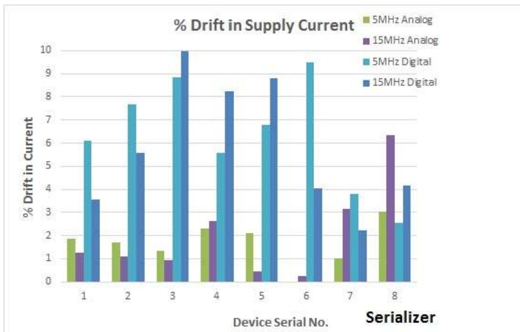

Fig. 4:Serializer-drift in supply current

SerDes pairs were meeting Electrical performance up to TID of 10K Rad (Fig. 6 & Fig. 7). The devices exhibited latch-up phenomenon even at LET of 10 MeV.cm^2/mg for Heavy Ion testing.

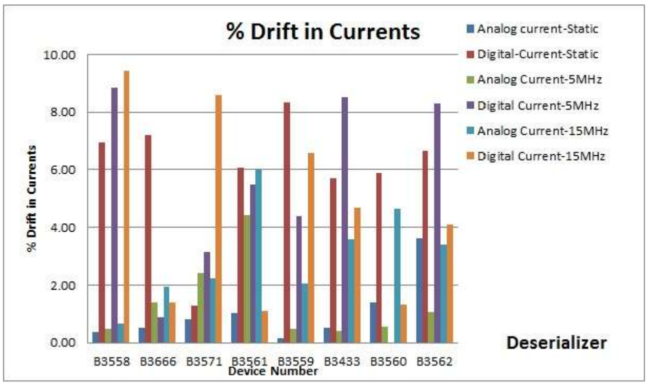

Fig. 5 Deserializer- drift in digital and analog supply currents

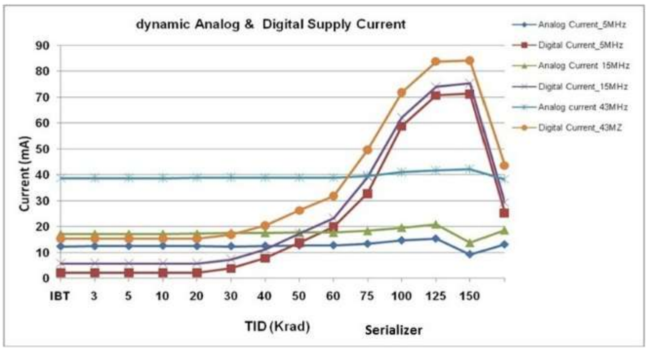

Fig. 6- Serializer TID

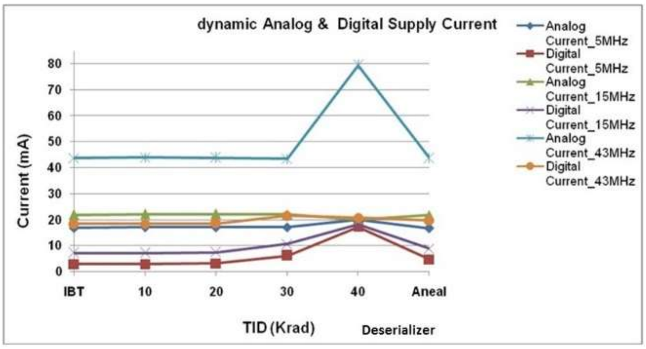

Fig. 7- Deserializer TID

C. COTS proposed for Chandrayan-2:

1) AD7492

2) AD5332

TSSOP-20, 8 bits DAC and TSSOP-24, 12 bits ADC are proposed to be used in Chandrayan-2. The qualification of these devices is in progress. 6 samples of each type were subjected for life test of 3200 hours. No device performance degradation was observed. Critical parameters are supply current, DNL, INL, monotonicity, SNR, SINAD, THD, ENOB, missing codes and fundamental frequency

VII-CONCLUSION

Six types of COTS have been qualified out of which AFE, SerDes and TEC are devices with highly complex circuit functionality. All the three types exhibited good performance during the qualification tests, however performance of AFE and SerDes under radiation environment was poor for single event effect (SEE).These devices could be used with suitable protection measures. The qualification of mixed signal devices is in progress. The screening and qualification test program were designed as per project specific and device specific requirements. Feasibility of using COTS devices was studied for various payloads and the devices were screened and qualified for the space missions. The above approach generated adequate information for assessment of COTS device reliability.

ACKNOWLEDGEMENT

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Usage of COTS/EEE parts in Space Applications - An overview

Harish H.V

Abstract - Many challenging space application requirements can be met using COTS. The time comes (better sooner than later) for the policymakers to reach a consensus on applying the COTS philosophy to space applications. This policy change is critical for the space industry. This paper attempts to suggest different issues to be tackled in order to meet technical, quality assurance, and cost requirements using COTS. A lighter package results in a smaller overall payload for the same board functionality, a concern of critical importance for space missions because the payload mass dictates the launch vehicle requirements. Costs can be potentially reduced by using screening, accelerated testing or partial qualification techniques to complement the existing commercial qualification as well as by the reduced package materials costs. Assessing the risk associated with potentially lower reliability devices, engineers within the commercial and aerospace industries are using trade-off and risk analysis to aid in reducing spacecraft system cost while increasing performance and maintaining high reliability

I. INTRODUCTION

For decades, military/space electrical, electronic, and electromechanical (EEE) parts have proved to be suitable for use in military and space applications. [NASA's Office of Safety & Mission Assurance (OSMA) evaluates newly available and advanced electronic parts for programs and projects under its EEE Parts program.] The traditional MIL-SPEC [U.S. defence standard/military specification] methodology is based on risk avoidance by testing the finished parts. Yet, global developments, like declining availability and budget constraints, have triggered the need to find an alternative solution. The alternative solution was officialised in 1994 by U.S. Secretary of Defence William Perry's directive imposing the use of commercial off-the-shelf (COTS) parts in military applications, exempting space applications. After decades of successful use of COTS in military applications, the above change has been proved viable. Many challenging space application requirements can be met only using COTS. The time comes (better sooner than later) for the policymakers to reach a consensus on applying the COTS philosophy to space applications. This policy change is critical for the space industry. This paper attempts to suggest different issues to be tackled in order to meet technical, quality assurance, and cost requirements using COTS. The term "COTS" in this paper refers to commercial EEE Parts, including plastic encapsulated active ones.

II. EEE parts control concepts

Director Spur India, Bangalore 560075MIL-SPEC	COTS
Risk Avoidance	Risk Management
Parts Testing	Statistical Process Control (SPC)
Small Volume Production	High Volume Production

U.S. Secretary of Defense William Perry's 1994 directive officially started the transition from the use of Military electrical, electronic, and electromechanical (EEE) parts in military applications to the use of commercial EEE parts (or COTS) in military applications. Space applications were exempted from meeting the directive requirements; however, the same drivers to this cultural change (like parts availability) apply also to the space industry.

III. MIL-SPEC VERSUS COTS

The following table compares the main principles of the two subject concepts.

For COTS, the main idea is:
– Risk Management: It is the Project responsibility to manage the risk. The risk cannot be zeroed, even by most stringent measures.
– Process Control: The Process builds reliability into the part.
– Production Level: High volume results in reliability.

IV. QUALITY VERSUS RELIABILITY

Quality and reliability are two different terms to be understood: Quality is the conformance to requirements at the start of use. Reliability is the probability of parts to meet the relevant specification over the time, under the worst operational conditions. Reliability is quality changing over time. In other words, quality is a snapshot at the start of the life and reliability is a motion picture over the life.

V. PART TESTING VERSUS PROCESS CONTROL

Given the above quality/reliability clarification, it is clear that reliability cannot be tested into the part. The qualification and screening are not considered as a substitute for manufacturing control, but rather as risk mitigation measures. Consequently, the way to address the reliability issue is by Statistical Process Control (SPC). The process (design followed by manufacturing) builds reliability into the part. In the environment of high-volume commercial EEE Parts

production, the SPC works well, resulting in very low failure rates at start of use timing. That does not mean that the part testing is worthless. The MIL-SPEC focuses on part testing, and much less on process control. The Statistical Process Control does not work for a low-volume production, like space/military EEE parts production. The testing mitigates the lack of statistics value. The reliability is built into the part. The quality is addressed by testing. That it is the positive side. Usually, the risk of damaging the parts during testing is ignored by policymakers. Any part level extra testing (outside the necessary manufacturer's inline testing) of the actual units to be flown results in higher risk than testing them. Selected sample testing is OK. The tested sample should not be used for flight. The manufacturer of military-qualified parts is not incentivized to improve the process. Changes involve time and money to meet the qualification requirements. The qualification addresses the quality. Process improvements addressing reliability may be skipped and the specification met anyway at parts delivery timing. This not the case with COTS; the focus is on process control. The high-volume production justifies the efficient implementation of statistics. Consequently, the reliability is addressed. The COTS manufacturer, freed from the MIL-SPEC restrictions, can continuously monitor the process and continuously improve it. The term "high-reliability" or "hi-rel" is used exclusively for space/military ones. It is wrong to conclude that by definition all COTS are non hi-rel parts. Decades of COTS use in military applications proved that COTS are reliable enough for the specific mission. The mission conditions in military are often more severe than in space, except radiation. The mission duration is often longer than a space mission.

VI. RELIABILITY PREDICTION

The leading document for reliability prediction has, for decades, been MIL-HDBK-217. This handbook, on the reliability prediction of electronic equipment, systematically suppressed the use of non-military parts in military applications. In spite of the wide usage of the above document, after the 1994 William Perry directive, it has been declared unreliable. On 15 Feb. 1996, a memorandum signed by Assistant Secretary of the Army/Research, Development, Acquisition Gilbert Decker stated: "In particular, MIL-HDBK-217, Reliability Prediction of Electronic Equipment, is not to appear in an RFP (request for proposal) as it been shown to be unreliable and its use can lead to erroneous and misleading reliability prediction." It has to be remembered that the reliability prediction model is based on the Arrhenius equation, a formula for the temperature dependence of reaction rates, considering one stress. Various experts claim that there is ample evidence that a straightforward application of the Arrhenius equation, with activation energies determined from high-temperature accelerated stress testing, is not the right way to deal with the matter.

VII. SPACE QUALIFIED

The term "space qualified" has to be fully understood in order not to be misused. The definition is: space systems, subsystems, and components which meet the specification relevant to their use. For example, often parts qualified to MIL-SPEC quality level "S" are called "space qualified". Quality level "S" is the highest quality level and should not be automatically interpreted as "S" = "space." Level "S", without specified radiation hardness assurance (RHA) for space systems requirement in the specific part specification, ignores fully or partially the radiation in space.

VIII. MILITARY VERSUS SPACE APPLICATION

The exclusive requirements for space are: radiation, outgassing, vacuum, microgravity, and atomic oxygen. Proper selected COTS (including nonhermetic ones) can meet these requirements.

COTS for space applications/issues to be revisited In order to progress in the process of massive introduction of COTS in space applications, well rooted requirements shall be revisited within the risk management philosophy, in order to save time and money. Following are some suggested revisit targets:

a. Reliability prediction

Too often, technical specifications/scopes of work (SOW) specify an absolute reliability limit to be met, penalizing use of COTS. The use of the term shall be revisited in order to use it within its limitations. MIL-HDBK-217F explicitly states its limitations: "a reliability prediction should never be assumed to represent the expected field reliability." A misinterpretation may lead to not justifiable extra cost. Anyway, as MIL-HDBK-217F admits, "those who view the prediction only as a number which must exceed a specified value can usually find the way to achieve their goal without any impact on the system."

b. Market driven availability

In view of the 2+ decades of official use of COTS in military applications, it is obvious that the apocalyptic prophesies did not materialize. The military-qualified and space-qualified EEE parts' share in the EEE parts global market is less than 0.5 percent in dollars. Nobody can stop a manufacturer from leaving a market found not to be profitable. Keeping the traditional approach means that we learn from history that we do not learn from history. The future EEE parts availability has to be secured for military applications and for space applications, as well. The business decisions are much stronger than any EEE parts policy.

c. Hermeticity requirement versus plastic taboo

The importance of package hermeticity is not arguable. The problems encountered in early stages (from the 60s) with nonhermetic plastic encapsulated semiconductors caused the military and space parts policy makers to taboo their use in military and space applications. Of course, the "hermeticity" of the plastic parts cannot compete with the hermeticity of the hermetic parts. The goal should be "enough" not the "best."

d. COTS post procurement testing

The needed COTS introduction into space applications is shadowed by the high non-recurring engineering (NRE) involved. The high NRE is driven by post-procurement testing requirements derived from the well-rooted traditional approach of part testing.

IX. RADIATION TID

It is the user's responsibility to find a way to assess the total ionizing dose (TID) withstanding capability of any part and use it accordingly. The following issues should be revisited:

a. Radiation Design Margin (RDM)

The RDM requirement provides a systematic approach to managing the mission risk posed by uncertainties in both the radiation model and hardware susceptibility to radiation. RDM takes into account traditionally an historic lot to lot variation that may be different today due to better manufacturing process control (SPC) and improvements. Revisit may lead to applied RDM reduction, leading to more COTS being able to withstand the radiation requirements.

b. Lot-by-Lot TID testing requirement

In view of the improved process control (SPC) and high-volume statistics validity, the lot-to-lot and within-a-lot variation issue is worth to be revisited. From the point of view of radiation testing, military-level qualified parts and COTS has the same lack of die traceability problem of not being wafer traceable. The space industry turns a blind eye on the lack of wafer traceability for the traditionally acceptable military level parts, but penalizes COTS in space because of same traceability issue!

c. Part TID tolerance level

The part TID withstanding capability level is established by radiation testing and is defined as the TID level at which the part goes out the specification limits for the first time. To relax the requirement, another practice is applied by those having a meaningful database. It is not a good engineering practice, because it relies on out-of-spec part operation toward the end-of-life phase of the mission. The higher level achieved is called Design Part TID Withstanding capability level. The design Worst Case Analysis (WCA) shall validate the above practice. Revisiting the above widely used practice may lead to new ideas of easing the introduction of relatively TID weak COTS in space applications. On the other hand, it may lead to the conclusion that when operating outside the spec the risk is too high.

d. EEE parts shielding

Use of more effective shield material lowers the predicted mission TID level seen by a part. Consequently, the required Part TID tolerance is decreasing and more parts become suitable for the space application (from TID point of view). There are better than aluminum materials (like tantalum), and there are more effective shielding techniques (like multilayer shields). Active shields (like magnetic) are in research stage.

X. RADIATION INDUCED LATCH UP (SEL)

SEL, one of the Single Event Effects, is destructive. The mitigation consists of a latch up protection circuit to quickly disconnect the damaging current. To implement such mitigation, the latch up current shall be known from the SEL testing. The SEL Testing is performed in heavy ions accelerators and involves high cost and a long time. In order to reduce cost and time, the following issues should be revisited:

a. SEL test method

Revisiting the traditional method versus another method may lead to cost reduction and time savings. Another SEL Test Method, worth being considered, is the less expensive Pulsed Laser SEL (and other SEE) testing, proved as efficient. By the way, the pulsed laser source may play an important role in bit mapping, mitigating Multiple Bit Upsets (MBU). Another known SEL Test Method is Californium 252, if used within its limitations.

b. SEL rate prediction

There is a practice, to be revisited for validity and increased use, based on comparison with the reliability figure of the part. It states that if the SEL probability is less than one tenth of the relevant reliability figure, the part may be used for flight as is.

c. Part technology/process

To help the rather complicated, difficult task of COTS SEL assessment, there is a strong need for knowledge of the relevant part technology/process basic data. The following information is needed: technology. Process, foundry, and die revision. Alliances in the space industry can substantially contribute to avoid testing duplications.

XI. DESTRUCTIVE PHYSICAL ANALYSIS (DPA)

The DPA, focusing on the process related issues, is a not a removable post-procurement activity. Saying that, it does not mean that the DPA testing depth should not be revisited for optimization.

XII. UPSCREENING

"Upscreening" means a raise of confidence level for using the part in the given space application. Upscreening traditionally is performed 100 percent, but it can also reach its goal by sample testing. The rationale behind sample (not to be flown) testing is the conviction that any handling of flight parts may damage them. It is worth paying attention to the NASA warning in official document PEM-INST-001: "There are numerous data indicating that improper handling and testing of the parts can introduce more defects than are screened out." The traditional post-procurement 100 percent upscreening requirement at part level needs to be revisited. MIL-STD-883, Method 1015, Burn-in Screen, states that "burn-in is performed for the purpose of eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which are evidenced as time and stress dependent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions." As seen above everything starts and ends within the manufacturing process of the die. Manufacturing defects may result in failures. The present COTS are manufactured in a rigorous statistical process controlled high-volume production regime. That results in a substantial better outgoing parts quality. The reliability cannot be addressed by upscreening. Extensive design, production, and operational use of COTS (as procured) in military applications in harsh environments, resulted in successful

experiences. As the technologies advance and the functional integration at part level increases, the electrical post-procurement testing becomes more and more difficult, inefficient, and costly.

XIII. QUALIFICATION

The successful use of COTS parts in military applications (very long operational life is often applicable) supports the viability of use of COTS in space applications. NASA PEM-INST-001 states: “For all PEMs, qualification by flight history or similarity is not acceptable.” It is not understood why NASA is still following the traditional way of thinking, imposing such a general restriction on all PEMs. Qualification and reliability monitoring are performed routinely by best in class parts manufacturers.

XIV. PROCUREMENT STRATEGY

Usually, the majority of the players in the space industry does not have all the skills and infrastructure to manage the EEE parts procurement alone. It is preferred to outsource these activities to specialized companies the so called parts procurement agencies. The procurement methodology for COTS can follow the one practiced for space parts. Centralization of the relevant activities is even more beneficial for COTS (reduction of duplicate NRE).

XV. SUMMARY

The 1994 Perry move meant reversal of EEE parts selection priority for military applications: First priority is given to use COTS. The focus went to process control, as the fundament of part reliability. The 1994 move to use of COTS in military has been proven successful. For space applications, there is a hesitating move to permit the use of COTS, keeping the traditional EEE parts selection priority: first priority to space parts. This methodology is a “no choice” permit to use COTS in space, within the 100 percent testing regime (moved to post-procurement phase) of the traditional (pre-Perry directive) philosophy. The minuscule military/space market life is finite and unpredictable. The present methodology viability depends on the EEE parts availability driven by business decisions. Consequently, the above methodology is not a secure solution. A revised, pragmatic space tailored COTS methodology has to be established and officially recognized. The methodology has to be based on the concept of process control rather than finished 100 percent part testing. There is a strong technical need for use of complex parts built using advanced technologies, available only as COTS. There is a strong need for cost reduction and schedule shortening. Educated decisions on eliminating not value added activities is a must for cost reduction. As per the present methodology the COTS part ownership cost is often higher than the procurement cost of space parts. There is no unsolvable technical issue to block the use of selected COTS in space applications.

Absolute reliability figure shall not be specified as a requirement to be met. Reliability prediction models shall be understood and not misused. The EEE parts availability assurance shall be considered a high-priority, critical parameter in their selection process. A new approach is needed to better secure the parts availability. COTS post-procurement testing shall be optimized, eliminating activities that do not add value. The present methodology has to be revisited for optimization and adaptation to the reality. Shared parts radiation databases shall be established to avoid duplicate resting. Focus on part types reduction and orders consolidation.

XVI. CONCLUSION

The time has come (better sooner than later) for policymakers to reach a consensus on applying a realistic COTS philosophy to space applications. There is no unsolvable technical issue to block the use of selected COTS in space applications. The resistance to change is the main obstacle to overcome.

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Cots, small cell lithium ion batteries for space application

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ABSTRACT

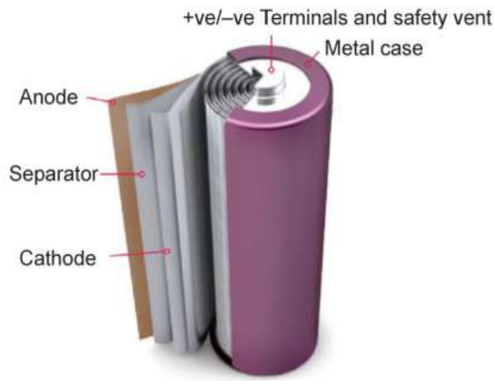
All Satellites need batteries to support during eclipse and peak loads. Advances in battery technology have led to lighter products that, in turn, allow spacecraft to carry heavier and more capable payloads. The lithium ion battery promises to revolutionise space batteries by providing a much better performance than what has been achieved by nickel based battery systems. This being the present scenario, we at ISRO are not far behind. Battery Division of ISRO has designed, developed and tested various capacities from 6Ah to 180Ah of lithium ion batteries. Micro Satellites and Nano Satellites always pose problems in terms of mass, volume and schedule. Battery Division took up the challenge and designed a battery with COTS (Commercially Of The Shelf) cells to meet the demands of first Micro satellite, HAMSAT. Since then many Satellites from Nano to Mini Satellites incorporated batteries using COTS cells. These cells offer great savings in terms of cost as compared to regular space grade cells. This paper attempts to cover how COTS batteries were designed developed and qualified meeting the minimum required reliability standards for Spacecraft applications by performing statistical process control and risk management.

I. INTRODUCTION

Many satellite batteries have successfully been made and flown using nickel cadmium/nickel hydrogen batteries. These batteries, however suffered with relatively low energy density with high mass penalty as power levels increased over time. With the advent of lithium ion batteries into space, the energy density of batteries were improved to nearly double over nickel hydrogen and three times of nickel cadmium. There are many advantages of lithium ion system over nickel system and this system adapts well with earlier power system configuration with minimal changes. Battery Division at ISRO had taken up characterising lithium ion cells during mid 90s and quickly designed batteries with space grade cells. Unlike in nickel systems, lithium ion cells are generally designed with one type of standard capacity as cells can easily be paralleled to increase the capacity which otherwise not possible with nickel based batteries. During the realisation of HAMSAT mission, it was realised that the area and mass available for battery was highly limited and accommodating a battery using space grade cells was almost impossible. An innovative approach was taken up to introduce COTS cells for evaluation and qualification. After successful evaluation on these types of cells, a battery was designed and qualified for HAMSAT Spacecraft. Typically life of these types of MicroSats varied from 6 months to 2 years. The life periods of MicroSats have increased overtime and reached 5 years and beyond. To meet the long life requirements and minimum reliability standards, many screening and other life tests have been introduced over time.

II. CELL DETAILS

Commercial lithium ion cells are of standard size (18650, 18mm dia and 65mm length) and typically having a capacity between 2 to 3Ah and voltage range from 3V to 4.2V. Since these commercial cells are mass produced, they reasonably have good uniformity over one manufacturing lot. Also these cells have many safety features to protect against overcharge and external short circuit on cells. Using these features, battery designers have configured cells in series parallel (s-p) configuration to meet voltage and capacity requirements with no cell balancing hardware attached. Typical lithium ion 18650 cell contains anode material of graphite (C) and Lithium cobalt oxide ($LiCo_2$) as cathode material. Lithium Hexafluorophosphate (LiPF6) is electrolyte dissolved with solvents like EMC, DEC and EC. Polyethylene is used as separator and case material is mild steel. The rated capacity varies from 2.2 to 2.8Ah based on the improvements made by the cell manufacturer in cell design from time to time. Internal resistance is about 80mOhm at room temperature. Table 1 gives the parametric values of 18650 cells. Fig. 1 shows the construction details of cell. The cost of the cells with an equivalent of energy density of 180Wh is at least 50 times lower than that of a space grade cell.



Cell Type	Cathode	Anode	Electrolyte	Central mandrel	Separator
LG 2600 mAh	$LiNi_xMn_yCo_zO_2$	Lithiated Graphite	EMC:DEC: EC	Absent	PE (monolayer)
LG 2800 mAh	$LiNi_xMn_yCo_zO_2$	Lithiated Graphite	EMC:DEC: EC	Present	PE with Coating of Alumina and TiO_2 indicating HRL separator

FIG.1: Cell construction and internal details

Sl.N.	Parameter	Value
1	LG 18650 cell	I2034F
2	Mass	45 g
3	Dimensions	Φ18mm,65mm
4	Nominal capacity	2.6Ah/2.8Ah
5	Max. Cell voltage	4.2V
6	Min. Cell voltage	3.0 V

Table 1: Parametric values of 18650 cells

III. CELL CHARACTERISATION STUDIES

The cells used in this type of batteries are commercial cells and they do not come with any performance data. In order to extend the use of COTS technology for longer missions, large data base needs to be generated. With adequate data base available, confidence of using these cells for longer missions including all LEO spacecraft missions will be very high. Fig.2 shows the flow chart of evaluation of COTS cells for space application.

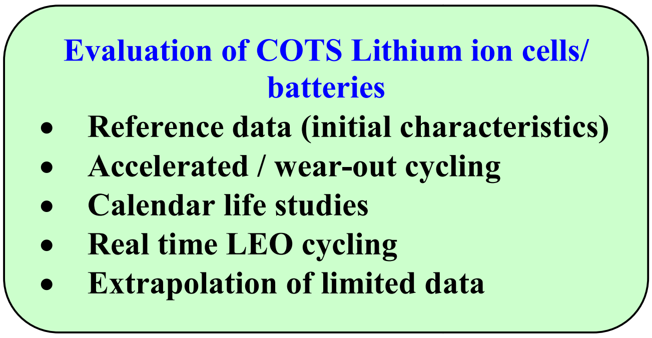
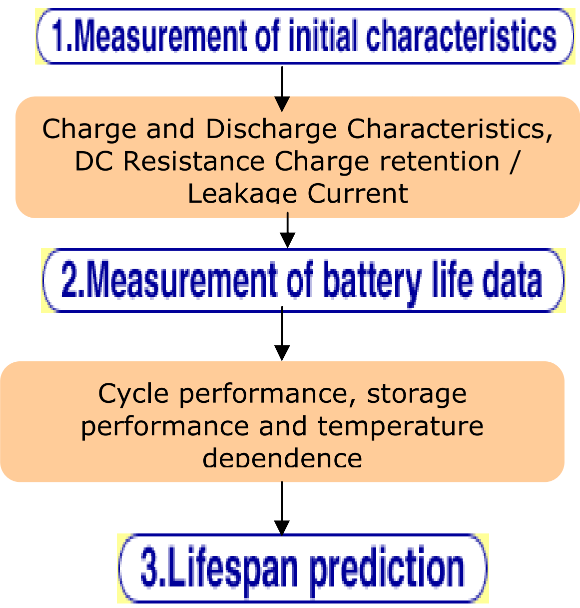


FIG 2: FLOW CHART ON EVALUATION OF COMMERCIAL CELLS



To generate data base on commercially available cells (say LG18650, 2.6Ah lithium ion cells), Battery Division of ISAC has entered into contract with M/s KHMD, Bangalore for setting up facility and running all the relevant tests and documenting the results as laid down in the contract. M/s KHMD has performed and continue to perform all the tests planned in the contract and document the results. Nearly 109 tests programmes were run on random selected cells as a part of initial characterisation covering standard capacity tests, internal resistance measurements, capacity tests at different charge voltages, charge & discharge rates and self discharge measurements at different voltages and durations. All the above tests were done at 3 temperatures. Typical charge/discharge characteristics at three temperatures and different rates are presented in Fig.2a, 2b, 3 and 4.

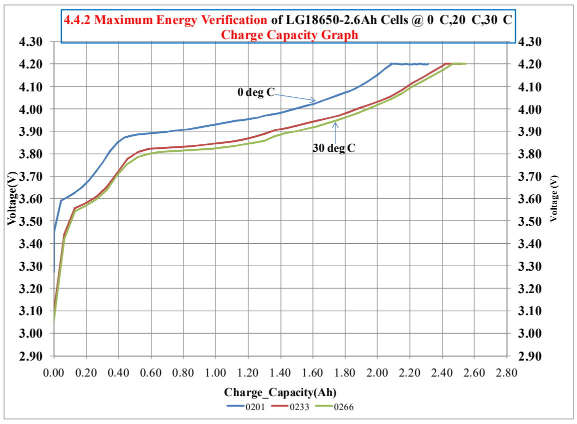


FIG.2a: Charge Characteristics of cell at different temperatures

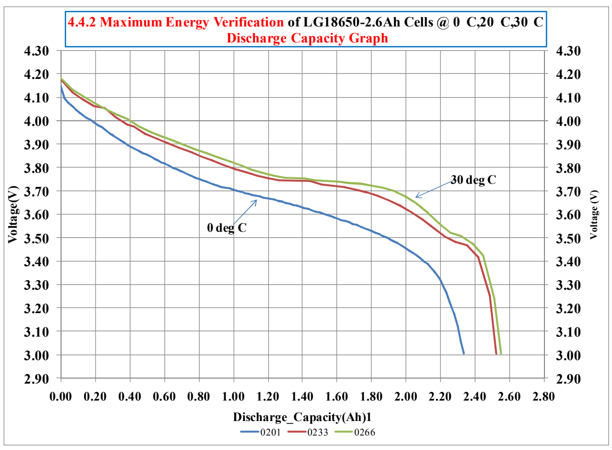


FIG.2b: Discharge Characteristics of cell at different temperatures

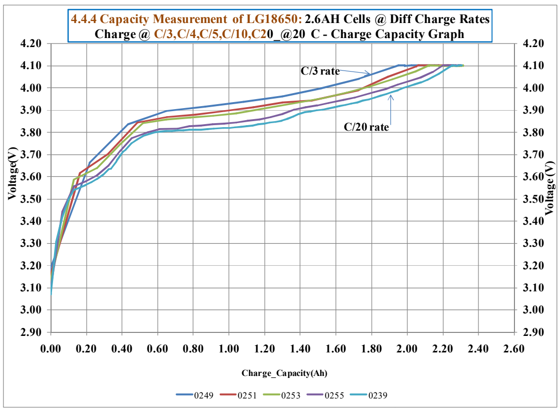


Fig.3. Charge characteristics of cells at different charge rates

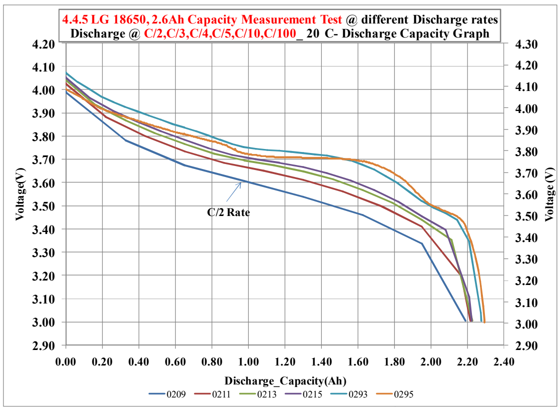


Fig.4. Discharge characteristics of cells at different discharge rates

IV. ACCELERATED LIFE TESTS

Accelerated life tests performed at three temperatures 10, 20 and 30 deg C covering 20% to 100% with high charge and discharge rates for 3 months to quickly assess the cells for any inherent defects in the cell before proceeding with the real time cycling. These tests are designed to evaluate for design defects which lead to sudden failures when exposed to high stress factors. Accelerated tests using elevated temperatures to accelerate cell ageing is not attempted here as the cells will experience higher capacity and power fading at elevated temperatures and the relationships are non linear. The entire duration of these tests have been limited to 3 months and test profiles have been formulated accordingly. Charge rates selected were C/2 rate and discharge rates were C rate. Typical capacity loss during cycling at 20degC is shown in Fig.5.

Accelerated life tests showed no sudden failures even at high depths of discharge cycling with high stress factors. Higher degradation was observed when dods exceeded 20% especially at 10deg C. The loss in capacity due to lithium loss at 100% dod(depth of discharge) is restricted to only 10% of initial capacity which is a good indicator for any commercial cell.

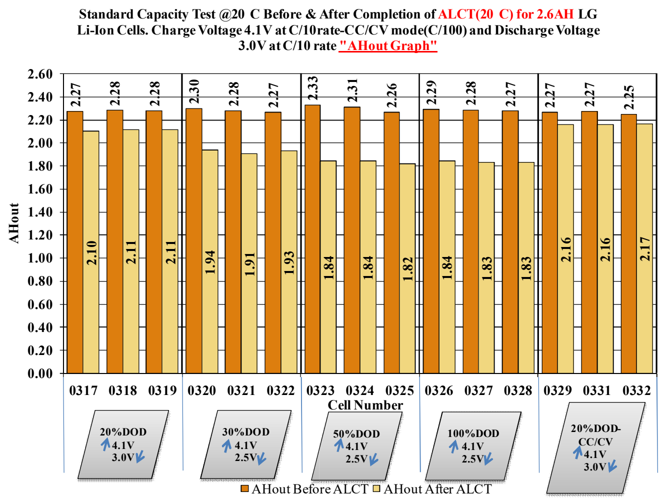


FIG.5: Standard capacity measurement at 20degC before and after cycling.

V. REAL TIME CYCLING TESTS

Real time cycling tests are necessary to understand the degradation mechanism which sets in cells over time during cycling. Generally all lithium ion batteries operate at about 20% dod for low earth orbit applications where batteries undergo large number of charge/discharge cycles. Real time cycling tests were planned some time during 2010 on randomly selected cells of two different capacities at different dods of 15%, 20% and 30% at three different charge voltages at two different temperatures namely 20 and 30 deg C. These tests were run continually (assessed the performance every 1000 cycles) for more than 5 years and still continuing. The performance is good at 20% dod and better than expected at 15%. More degradation is seen at 30% dod and not considered for design in present batteries. The degradation at higher dod is not due to dod per se but due to higher rates applied to cells to maintain the orbital duration. Figs.6 and 7 show the variation of cell characteristics over an orbit from BOL to 25,000 cycles. Fig 8, 9 and 10 show the end of discharge voltage, capacity and impedance performance over 25,000 cycles at 20deg C. Cells showed good voltage performance above 3.6V even after 25,000 cycles at 20% dod. Better voltage performance seen for 2.8Ah cell compared to 2.6Ah during cycling. In conclusion, all the cells have performed well and will give best performance when operated at 15% dod, limiting charge voltage to 4.1V and maintaining temperature between 15 and 20 deg C. Fig.11 gives the comparison of end of

eclipse discharge voltage over number of cycles at different dods of 15% and 20%.

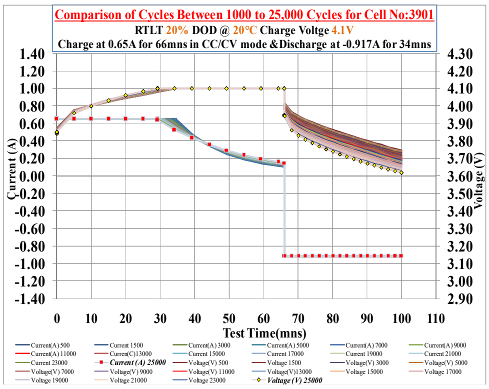


FIG.6: Charge/discharge characteristic of cell in one cycle from BOL to 25,000 cycles at 20 deg C

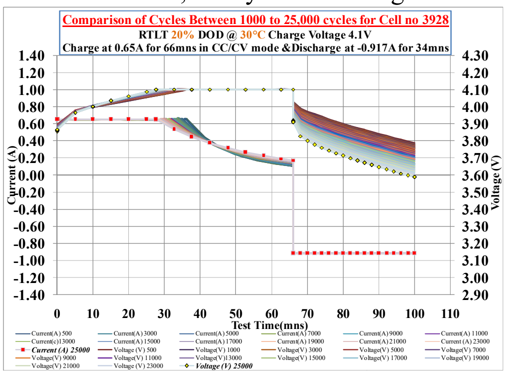


FIG.7: Charge/discharge characteristic of cell during one cycle from BOL to 25,000 cycles at 30 deg C

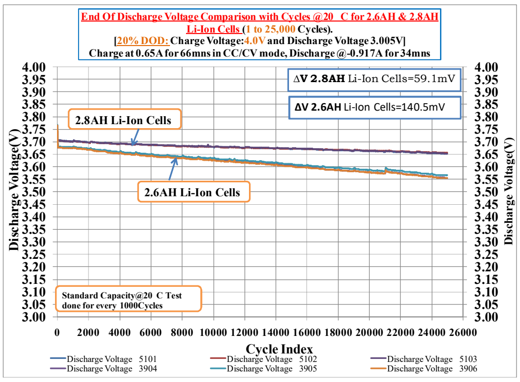


FIG.8: Comparison of end of eclipse discharge voltage variation over 25,000 cycles for 2.6Ah and 2.8Ah.

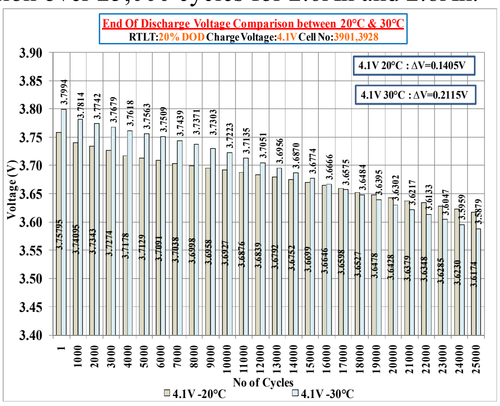


FIG. 9: Comparison of end of discharge voltage variation over cycles 20 and 30 deg C

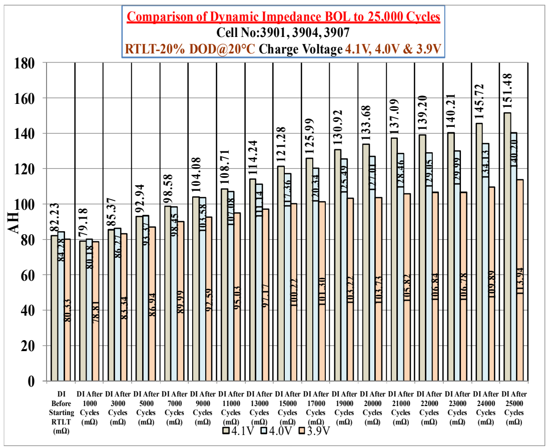


FIG.10: Impedance growth over 25,000 cycles at different charge voltages

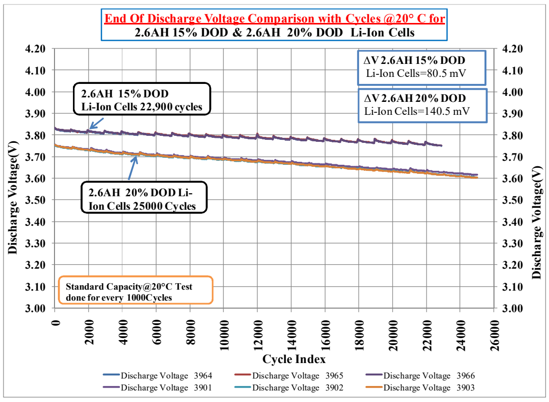


FIG.11: Comparison of end of discharge voltage variation over cycles for 15% and 20% dod

VI. CALENDAR LIFE TESTS

A separate study was taken up along with cycling tests to estimate the degradation of cells purely due to ageing but not cycling. Real time cycling tests will provide information on both cycling as well as ageing. This study will separate the ageing effect on cells and also provide insight on storage effects of cells before use on flight. A test matrix was planned and executed covering storage of cells at different states of charge and temperatures. Six monthly evaluations were done on these cells to determine capacity degradation and impedance growth over time. Fig. 12 and 13 show the capacity loss and impedance growth over time for 5 years. Fig. 14 shows the variation of complete discharge voltage characteristic over time.

In conclusion the cells stored at 3.8V showed lowest degradation at 20degC. Generally cells are stored at 0deg C at very low states of charge below 3.8V to minimise the degradation.

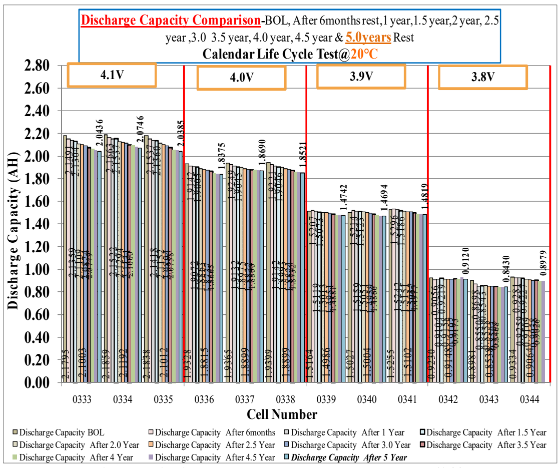


FIG.12: Capacity variation over 5 years storage at different states of charge

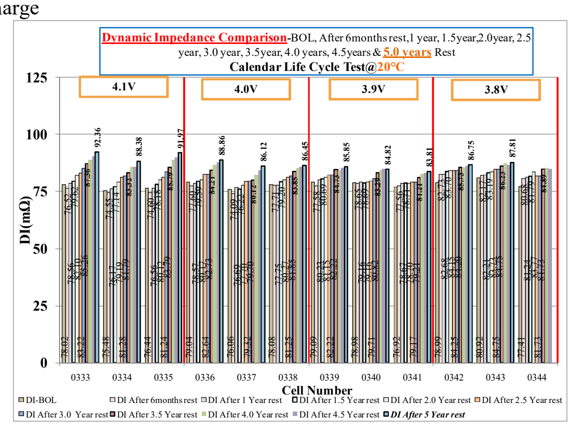


FIG.13 Growth of Impedance over 5 years of storage at different states of charge.

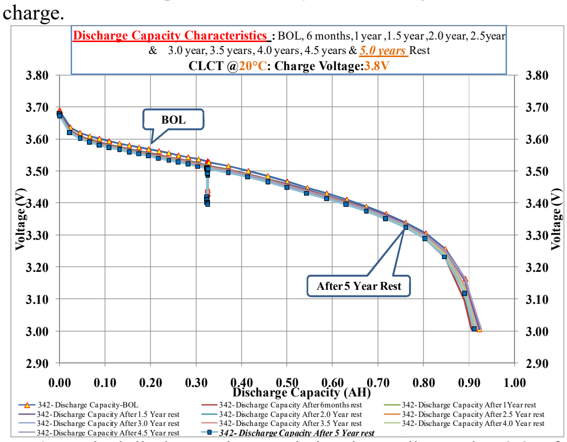


FIG. 14: Typical discharge characteristic when cell stored at 3.8V for 5 years.

VII. SCREENING AND MATCHING

Each cell that is used in our space batteries is further subjected to a screening test to ensure that we achieve a high reliability. COTS cells are manufactured sufficiently large in a single batch and that can cater to fabricate many batteries. Cell properties are very uniform within a batch and ideal for a COTS approach. Following initial characterisation, the cells are screened 100% to detect rogues and to grade and match for use in a battery. All cells are screened for standard capacity measurement, End of charge and end of discharge resistance measurements, self discharge and dynamic impedance measurements. Subsequent to screening of all cells, cells are subjected to matching to eliminate non uniformity in cells before forming into battery. Matching criterion is applied on capacity, impedance and self discharge. Stringent acceptance criteria are generally applied to both in screening and matching to make batteries more robust and space worthy.

VIII. BATTERY CONCEPT DESIGN

Traditionally for a spacecraft battery, nickel cadmium and nickel hydrogen cells were connected in a single string. In lithium ion battery, cells can be connected in series and parallel. There are two alternative topologies exist, s-p and p-s by connecting series parallel of strings. In both topologies, number s determines the battery voltage and p determines the battery capacity. In s-p topology, series cells are arranged in parallel strings as shown in Fig.15. In p-s topology cells are connected in parallel (as shown in Fig. 16) which forms one module and these modules in turn are connected in series [1]. The s-p topology is highly tolerant to cell failure.

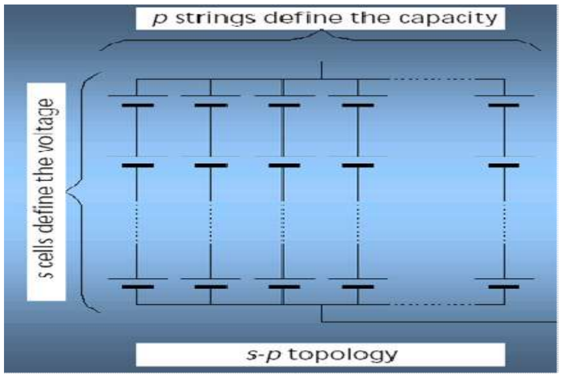


FIG. 15: Battery configuration with s-p topology

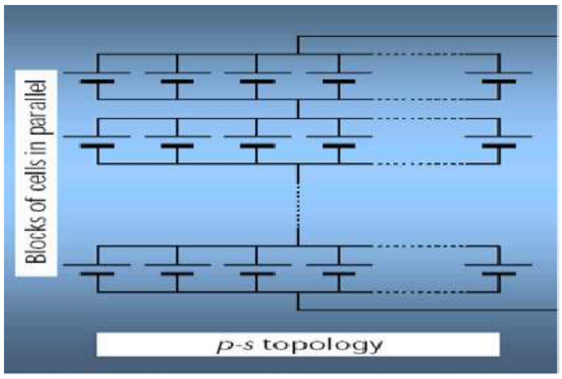


FIG.16: Battery configuration with p-s topology

- In the event of an open circuit failure of cell, a string of cells is lost. Importantly, for a small cell, the loss in

capacity is relatively small compared to larger cell capacity of the battery where the effect is unacceptable.

- In the event of closed circuit failure, during charge other cells in that string become overcharged. Since these cells contain overcharge protection device (cell disconnect mechanism) causing the cell to fail in open due to excessive overcharge eventually leads to open circuit failure and results in loss of one string as before.

High battery reliability is achieved because the battery can be easily sized to accommodate several cells failures with only a small loss in capacity. Independent studies were made on these types of cells to evaluate safety aspects related to over-charge and over-discharge [2].

Large space cells are produced in small batches using low-volume production techniques. Consequently, large cells exhibit appreciable capacity variation within batches. To ensure that the full capacity of each cell is used and that no cells are overcharged, charge-balancing electronics must be employed on large-cell batteries. Cell balancing and bypass electronics add considerable complexity, cost and mass to the overall battery system. In small cell approach, complex charge/discharge electronics are not required and control is at battery voltage level.

Modular stackable battery design has been adopted using the COTS cells which will offer advantages in terms of mass and volume. The battery module in vertical configuration has been designed where the cells are bonded to the structure horizontally. Here the modules are stacked one beside the other meeting structural and thermal requirements. Fig.17 shows how modules can be inter-connected to boost the capacity.

Utilising the s-p topology with small cells allows a huge degree in flexibility in battery design. Merely by altering the s-p array dimensions, the capacity and voltage range can be modified without the need for fundamental re-design or cell qualification.

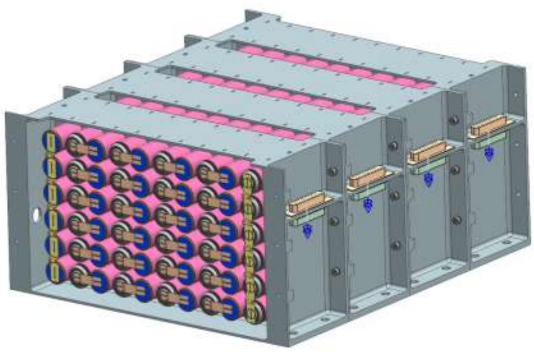


FIG.17: Battery made in stackable configuration

Space programmes often choose to procure flight spare units to alleviate schedule risk in the event of handling errors during Assembly, Integration and Test. Modular batteries can offer a low cost spare solution, as a full suite of modules are not usually required.

IX. CONCLUSION

Batteries have traditionally been an item that can demand a significant portion of programmatic budget. Use of batteries made out of low cost, COTS cells offer great savings as great as 80% compared to space grade batteries taking into account the cost of facility setup and running the life tests spanned over many batteries. Based on the successful evaluation of cells, qualification test matrix at cell level and at battery level, established screening and economical matching methodologies adopted will certainly make batteries with COTS cells very attractive for space applications.

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Performance Analysis of COTS Components used in PISAT

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Abstract— PISAT is 3-axis stabilized magnetic control Student Satellite from PES University, Bangalore. The main objective is to familiarize students with Space Technology and operations. PISAT is designed based on COTS components such as Micro controller, H-Switch, current limiter and DC/DC converters etc. PISAT was launched on 26th Sep 2016 by PSLV-C35. We found most of the components in PISAT worked well. However we observed upsets in some components.

This paper describes configuration of PISAT highlighting all COTS components and provide statistics of upsets and subsequent recovery. This is also to be highlighted that most of major components in PISAT has current limit circuitry hence mitigation techniques of current limit has helped that no components has failed. Finally this paper provide recommendations which types COTS components could be used for student Satellites. Also gives details of mitigation techniques used in PISAT which has avoided permanent failures.

Index Terms—PISAT, COTS Components, failure mitigation techniques

I. INTRODUCTION

PISAT is a three axis stabilized imaging satellite. PISAT is a Nano satellite weighing about 5 Kg. The major subsystems are Payload-an imaging camera – GomSpace Nano Cam C1U [1], On Board Computer (OBC), Attitude Determination and Control System (ADCS), RF communication system with S Band frequency, thermal and structural systems and Electrical Power System (EPS). The ground software essential for mission operations has been developed for on ground orbit determination, telemetry reception and commanding. PES University has commissioned S-Band ground station which is the master control center for PISAT mission. The estimated operational life is approximately six months. The orbit is a Sun-Synchronous Polar orbit similar to the main satellite. This satellite was launched by PSLV C-35, a standard IRS class of orbits around 680 km. Fig 1 shows the CAD model of PISAT.

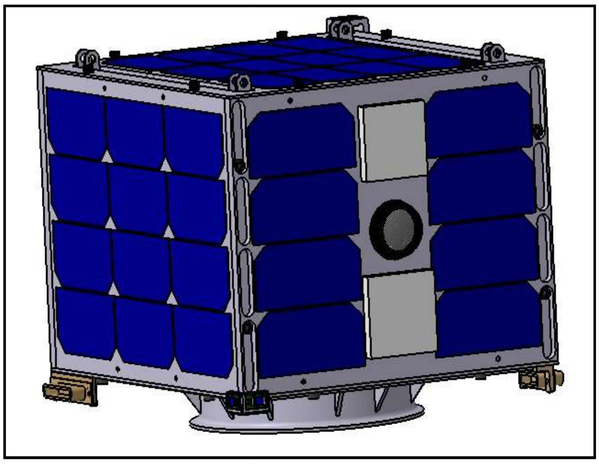

Fig 1: CAD Model of PISAT

The mission objective was to design and develop Nano-satellite for remote sensing applications. The payload was a 1U camera with <80 m/pixel resolution. Some of the secondary objectives were to familiarize and excite students in the area of space technology. This project served as an educational platform in dealing with advanced space technology and its experiments. The tertiary objective was to perform payload processing for imaging payload on ground.

II. PISAT SUBSYSTEMS INVOLVING COTS COMPONENTS

A. Payload

The payload used for the mission is a CMOS based Nano camera. It is a COTS component designed and developed by Gomspace. It has a 3MP 10 bit color CMOS sensor, with a resolution of 91.1m / pixel from 720 km altitude, with Field of View (FOV) – 9.22˚. The image acquired has a resolution of 2048 X 1536 pixels. It is interfaced with the on board computer through I2C

communication and has onboard compression capability of 6MB to 200KB. The payload used is shown in Fig 2.

Fig 2: Gomspace Nano Cam C1U used in PISAT

B. On Board Computer (OBC)

On Board Computer consisted of a high performance 32 bit AVR32 RISC micro-controller (AT32UC3A0512), with a clock speed 12 MHz. It is a COTS component designed and developed by Atmel. It has 64 kB static RAM and 512 kB Storage (Flash Memory). I2C protocol is used to interface with payload with a data rate of 400kbps. OBC is connected to Inertial Measurement Unit (IMU) using SPI protocol with a data rate of 600kbps. This controller supports 10 bit Analog to Digital conversion. These pins are used to interface with temperature sensors, Four Pi Sun Sensor (FPSS). Along with a micro-controller we have Actel Anti fuse FPGA for Telemetry, Tele command verification. Voltage and power safety logic (developed in-house) is executed using this FPGA. A 4 MB EEPROM is interfaced using I2C protocol for Payload data Storage. A Modular approach was followed for developing supporting software for devices interfaced to OBC. Fig 3 shows the OBC card used in PISAT.

Fig 3: OBC card used in PISAT.

C. Electrical Power System (EPS)

Electrical Power System (EPS) card consists of a battery tied bus. Four Li-ion cells are connected in 2S-2P configuration with a nominal voltage pf 7.4 V. Each cell has a capacity of 5200 mAh. The power generated by solar cells is 11 W and power consumption is 5 W. We have body mounted solar cells; a total of 52 solar cells (13 strings with 4 cells in series). For power distribution SMD type DC-DC Buck-Boost converters (LTC3112) are used to provide the regulated power for various subsystems of the spacecraft. The enable / disable function of the DC-DC converters are used to meet the under voltage protection of the battery. Built-in soft start circuitry is enabled to reduce the startup current to avoid loading of solar panels. Two numbers of 8.7V, 5W low leakage current Zener diodes are connected in parallel to provide overvoltage protection for the battery. Safety features such as current limiter (TPS2030) circuit is provided for OBC card to protect the microcontroller. Snap mechanism is realized using a MOSFET switch (IRF7751). The PCB of the EPS card had a special copper cladded thermal layer to provide thermal efficiency and safety to the system [2].. Fig. 4 shows the block diagram of electrical power system of PISAT. Fig. 5 depicts the EPS card used in PISAT

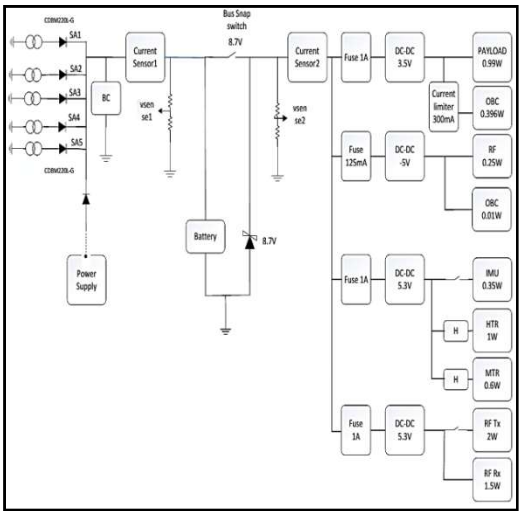

Fig 4: Block Diagram of Electrical Power System of PISAT

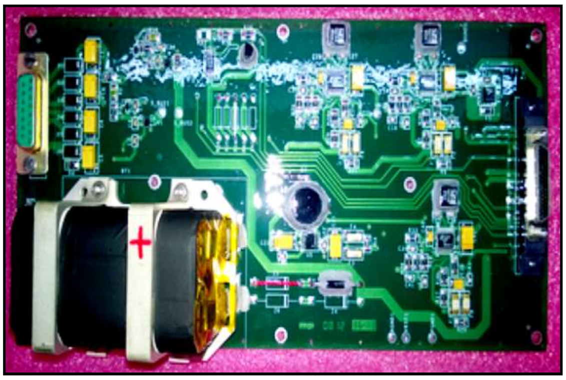

Fig 5: EPS Card Used in PISAT

D. Attitude Determination and Control Systems (ADCS)

PISAT is a three axis stabilized satellite with active magnetic control. The sensors used are Four Pi Sun Sensors (FPSS) for position estimation and Inertial Measurement Unit (IMU) for body rate, magnetic field determination [5]. The ADCS system gives the satellite a pointing accuracy of +/- 5˚. The IMU used is a COTS component designed and fabricated by Analog Devices whereas the FPSS was developed in-house at PES University. PISAT is designed to operate in four modes; Suspended mode, Detumbling Mode, Three Axis Mode and safe mode. The actuators used are magnetic torquers. SGP4 model is used for orbit determination and propagation. Fig 6 illustrates the IMU [1] used in PISAT.

Fig 6: IMU Used in PISAT

E. RF Communication Systems

The onboard TT&C (RF) system for PISAT consists of a single non coherent S-band FM receiver, S-band BPSK transmitter and an antenna system to provide omni coverage.

FSK/FM modulation scheme is used to transmit the formatted telecommand data, at 100 bps rate, on S-band uplink carrier (2030 MHz). The onboard receiver receives the S-band signal transmitted from the PES Satellite Control Facility. The received S-band signal is down converted to 70 MHz and FM demodulated to get FSK signal which is fed to OBC for further processing. The telemetry and payload data is formatted at 10 kbps and ½ convolution coded. The coded data at 20 kbps is transmitted by BPSK modulating the locally generated S-band carrier (2240 MHz). An omni antenna system designed with micro strip patches to provide up and down links in orthogonal circular polarizations [3][4]. The configuration of the onboard RF system is shown in Fig7

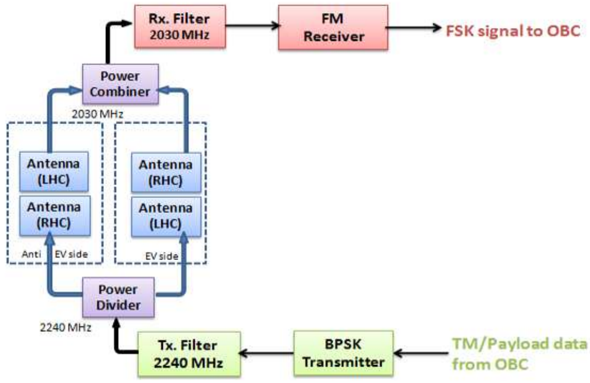

Fig 7: Block Diagram of PISAT RF Transceiver System

III. ANALYSIS OF COTS COMPONENTS

A. Gomspace Nanocam C1U (Payload)

The NanoCam C1U camera used is a robust and modular system. It is an off-the-shelf component made off: lens, lens table, image acquisition, processing board, and software [2]. NanoCam C1U is designed and developed to be implemented in a standard 1U CubeSat. The performance of the camera was satisfactory. During testing we observed fungal growth on the lens on the camera. This impeded the clarity of the image. Analysis showed that the humidity is to be controlled to reduce the fungal growth. Proper measures improved the performance of the camera. Fig. 8 show the camera performance after the clearance of fungus.

Fig 8: Image after fungal treatment

B. Microcontroller

Atmel AVR 32 Microcontroller (AT32UC3A0512) formed a core part of the on board computer of PISAT. It is a 32 bit RISC architecture based microcontroller. The on board computer is connected to payload, IMU and EEPROM through I2C and SPI protocols supported by this microcontroller. During ground testing the controller performed as per the requirement. In space conditions the controller was affected by radiation effects. The upsets in the controller forced periodic system reset. This had a

critical effect on the mission. Due to periodic resets, the ADCS parameters could not be updated. As a result there was considerable attitude loss which affected the imagery. Furthermore, the latch up also affected the payload data storage. The I2C line experienced periodic upsets which resulted in corrupted data to be stored in EEPROM. However no hardware failure was observed.

C. Inertial Measurement Unit (IMU)

During IMU testing and simulation using Test system glitches were seen in data transfer due to noise spikes. Through analysis it was found that long SPI lines caused timing delays. Proper measures were taken and this condition was avoided for on board functioning. The performance was satisfactory with no timing delays and manufacture mentioned precision was achieved.

D. DC-DC Buck Boost Convertors

SMD Type DC-DC convertors LTC3112 and MAX764MJ were used for positive and negative voltages respectively. These were employed to distribute the power generated to all the subsystems. The enable / disable function of the DC-DC converters provided ample protection to the battery. These converters come with a built-in soft start circuitry which reduce the startup current and avoid loading effects. During qualification model EPS card fabrication we found that these convertors are thermally sensitive. Proper utilization of heat pads improved the performance drastically thereby meeting the design requirements.

E. MOSFET Switch and Passive Components

MOSFET Switch (IRF7751) was used in the snap mechanism of PISAT. The performance of the switch was satisfactory with proper functioning at all conditions.

FSK Band pass filter is a critical element in Telecommand chain. In PISAT Qualification Model it was observed that commands were not through below -5˚C. Analysis showed that the capacitors used in Band pass filter circuit were of type X7R dielectric. The capacitance variation of these type of capacitors over the temperature range of -55 to +125 is +/- 15 %. For a temp range of -20 to +55 the variation in capacitor is 12.5 %.

So the centre frequency used to shift by 12.5% resulting in non-execution of commands.

IV. MITIGATION TECHNIQUES

To protect critical components various mitigation techniques were employed in every subsystem. Some of them are listed below:

A. Microcontroller Latch up techniques

Radiation effects are predominant on COTS components. Different errors may be caused; soft errors, hard errors and latch up. Soft errors generally cause endless loops in software. These can be handled by employing Non Mask able Interrupt (NMI) reset issued through Watch Dog Timer programmed in a radiation tolerant FPGA.

Hard error can be handled by employing provision of system reset through a radiation tolerant FPGA.

Latch up condition is very critical and can cause fatal damages to the IC if current is not limited. To handle this, in PISAT the microcontroller is powered on through Current limiter IC which protects the microcontroller during Latch up condition. Fig 9 illustrates the block diagram of power on scheme employed in OBC of PISAT.

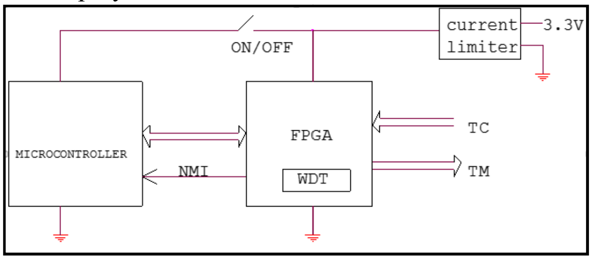

Fig 9: Power on Scheme of PISAT OBC

B. Deep discharge protection for Battery

Battery is a very critical component for any satellite system. Special care is to be taken to ensure maximum safety to this component. For battery short circuit protection, fuses are used before connecting to DC/DC converters. The configuration is shown in Fig 10. Also to protect battery from deep discharge DC-DC converters are disabled automatically by run control signal.

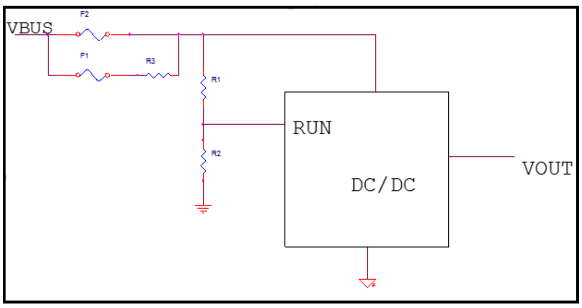

Fig 10: Fuse configuration for battery protection.

C. Thermal layers for DC-DC convertors

D.

The DC-DC converters used were tiny SMD COTS devices with heat pad at the bottom as heat sinks. As we faced issues, we took extra care in layout design so that thermal optimization was provided for these convertors. The

material of the PCB was selected to conduct heat away from the device. The thermal layer was connected to structure through mounting holes. While soldering we employed reflow soldering technique to establish contact between heat pad and PCB.

E. Capacitor selection for Band Pass Filter used in telecommand chain

During testing a shift in the cutoff frequency was observed. After analysis the capacitor was changed from X7R dielectric type to NPO type capacitors. These capacitors have high efficiency and thermal tolerance of (30 ppm/˚ C).

F. Imaging payload fungal growth mitigation

During testing of Camera in Day light fungal growth was observed. This growth was exponential and affected imaging. To solve this issue the Lens assembly was detached and sensor was cleaned with Isopropyl Alcohol (IPA). This reduced the growth and clear images were observed.

V. RECOMMENDED COTS COMPONENTS

From our experience with PISAT these are the critical guidelines to be followed to select COTS component in low cost satellite missions.

1. For critical systems proven COTS components have to be chosen.
2. Augmented circuitry software provision to be employed in OBC to overcome radiation related problems.
3. To mitigate thermal problems proper fabrication techniques to be followed. The components selected should meet the space conditions and work efficiently in the temperature range of -40˚C to +85˚C.
4. The ICs should preferably have ceramic packaging for better material and thermal stability.
5. The designers should select components with minimum of 50 % derating for higher stability of the design.
6. Current limiters and Zener protection to be provided to all critical components to avoid hazardous effects of radiation latch up.
7. Materials used in harness should have low percent of evaporation.
8. Along with temperature, ESD protection, humidity control also to be provided to avoid fungal growth in optical systems.
9. Proper thermal analysis to be performed at different space craft modes.

Radiation certified micro controller will increase the lifetime of the mission and enhances the success rate of the

VI. CONCLUSION

The COTS components used in PISAT have principally worked satisfactorily. The mitigation techniques described in this paper have worked efficiently and have increased the life of the spacecraft. These techniques are recommended to be employed in future low cost missions. If the recommendations for selection of COTS components given in this paper are followed, better results can be achieved.

ACKNOWLEDGMENT

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Flash memory technology for space application – An approach and implementation plan

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Abstract—Flash memory technology has been considered for space application. This paper provides an approach and implementation plan for flash memory based mass data storage system for space application. It also provides outcome of the experiments that have been carried out in recent past to characterize the behavior of flash memory in space environment and the design aspects which need to be addressed when dealing with flash memory for space environment, as identified by domain experts.

Key words—Bit error rate, Flash memories, Error correction codes, Satellites

I. INTRODUCTION

Initially, a simple sequential tape recorder was used as storage technology for mass data storage in space systems. Henceforth, Memory technology for space application is evolving as in commercial application. The evolution is driven by the requirements coming from the complex space mission and the emerging memory technology for commercial application. For more than a decade, DRAM technology devices are in use for mass storage in space systems [1].

Flash memory technology is being used for mass data storage in the consumer electronics products[2]. Recent past, Flash memory technology is being considered for space application for their non volatile, high storage density, low power, and high data throughput[1]. Towards this, experiments have been conducted to study the impact of particle radiation on performance of flash memory devices. Also, the challenges in adopting the flash memory technology for space applications have been studies by domain experts

This paper aims to provide an overview of the flash memory technology, conclusion of the experiments conducted on flash memory technology in recent time to study the impact of particle radiation, design parameters of flash memory which need to be critically looked into, for space application, as identified by domain experts. It also provides, the approach for induction of the flash memory based mass data storage system to space program.

II. FLASH MEMORY TECHNOLOGY

Flash memories store data as charge trapped on a floating gate between the control gate and the channel of a CMOS transistor. The basic structure of a flash-memory cell uses a dual sandwiched gate structure, interposing a floating gate between the body of the device and the control gate. It is similar to the structure of an EEPROM. Compared to EEPROM, Flash memory technology uses a much thinner oxide between the floating gate and channel region. The thin oxide allows charge to be transferred to and from the floating gate by either of two mechanisms namely Flower-Nordheim(F-N) tunneling from the source or body, or hot-electron injection from the channel region [3].

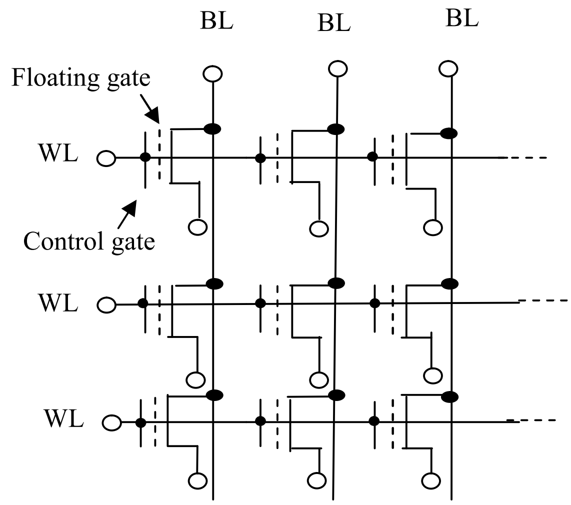

Figure 1. NOR flash memory cell architecture

NOR and NAND are the two basic structures that are used for the development of flash-memory. The NOR structure, shown in Figure 1, provides direct access to individual cells, but increases cell area because of the need for contacts at each drain and source connection[4].

The NAND structure, shown in Figure 2, organized in 16-bit stacks, is more compact because it does not provide contacts to individual source and drain regions. But, cells in the NAND structure require reading and writing through the other cells in the stack. This results in inherently slower cell access [4].

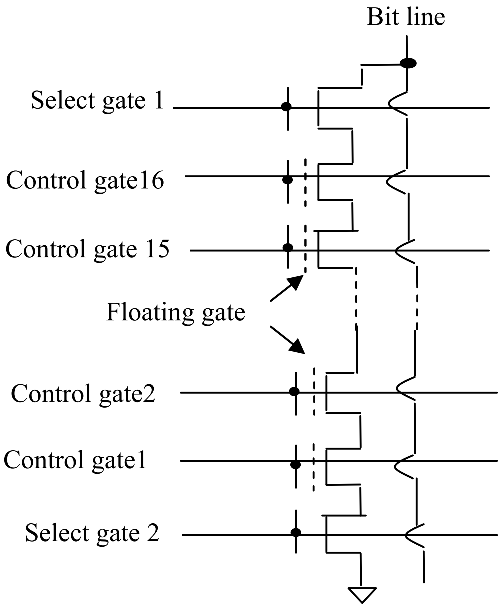

Figure 2. NAND flash memory cell architecture

A charge-pump circuit is also required in order to provide the high internal voltages that are needed for erase and write operations of the flash memory. Reading can be done relatively rapidly for either cell architecture. However, erasing and writing are very slow operations compared to conventional memories. To overcome this limitation, flash memories are subdivided into blocks and erasing and writing operations are done at the block level [4]. NAND flash memory is preferred for storage systems due to the very high memory capacity per device.

To evaluate the flash memories, it is essential to identify the operating modes of the device for a particular application. Read, program and erase are the basic modes of Flash memory.

New design techniques such as multilevel storage have been developed to increase storage density in flash memory. Thus, each gate can store one or more bits of information depending on whether it is a single-level cell (SLC) or a multi-level cell (MLC).

Further, the complexity of the device increases with reduction in the cell size. Because of its complexity, flash memories cannot be considered as simple memory device. So, it is quite interesting to determine how they respond in a radiation environments.

III. RADIATION EFFECTS

In the past, experiments were conducted on flash memory to understand the impact of Total ionizing dose (TID) and Single event effects (SEE). Also, its performance was verified with respect to bit error rate, during the experiments.

Many of the heavy-ion tests were done with the device in a static mode during the irradiation period. This simulates a very low duty cycle read-only mode and eliminates the possibility that the upset in the decoding or write logic might interfere with cell upset during active-reads. Reading the memory contents after the irradiation test, provides a direct way to determine whether portions of the memory were changed during irradiation. Some tests were also done in Erase Write Read(EWR) mode. Tests were also done with devices unpowered to determine whether heavy ions could introduce cell upsets or operational error in unpowered devices [3].

Way back, a radiation test was conducted on flash memory from Intel and Samsung devices and its results were reported [4]. Conclusion of the experiment reported, is as follows. Tests of multi-level flash memories have shown that they typically fail at relatively low levels, below 20 krad(Si), when biased during irradiation. The advanced devices tested in the experiment demonstrated lower failure levels relative to earlier generation devices. These devices undergo far less degradation when they are irradiated in an unbiased mode, and there are many applications where they can be used effectively in a mainly unpowered, read-only mode. However, they are far more vulnerable to failure in erase and write modes, which is probably caused by changes in the internal charge pump (erase and write functions requires very high internal voltages). With relatively tight tolerances, charge-pump failures were identified as the cause of failure at low total dose levels in older device type [4], where external erase/write voltages could be used instead of the internal charge pump. However, the newer devices do not provide this option. Single event upset in the newer devices appears to be similar to the older parts with some exceptions. Functional failures caused by cell upset in the very complex control and state registers used in flash memory architecture continue to occur. Catastrophic failures are still occurring for irradiations in EWR mode

Another experiment was conducted on another set of flash memory from Intel and Samsung and its results were reported [3]. Conclusion of the experiment reported, is as follows. Tests of these two flash memory technologies have shown that the single event upset effects are dominated by the complex architecture of these devices rather than upset in the storage array. The many operating conditions and functional upset conditions that occur, make it difficult to interpret-event upsets in flash memory. Recovery becomes more difficult because of the number of the functional errors that occur due to irradiation. Error correction would have to be implemented at the block level in order to correct for all of errors, along with power cycling to recover from modes that caused functional errors, but did not produce

memory errors. The irradiation test indicates that cell upsets never occurred in unpowered devices, even for effective LET values up to 120 MeV-cm2/mg at a 60 degree angle [3].

IV. DESIGN CRITERIA

Design of a solid state data recorder for space applications should address many constraints imposed by space environment. Hence, proper counter measures are needed to improve the dependability of the whole system. Designing flash memory based systems for space application requires exploring number of design dimensions to enhance reliability [5]. In recent time, use of flash memory in space systems is reported [1].

General observation is that unhardened commercial technology has variable radiation response, and requires testing for characterization. Also, Flash memories have bit error rate performance better than standard volatile memories, because of nonvolatile feature [6].

To start with, it is essential to assess the radiation tolerance requirements for a memory device, which is to be used in a data storage system of a spacecraft, and it depends on the location of the device, design of the spacecraft, orbit of the spacecraft and mission life[7]. Also, it is essential to know modes of operation of memory devices and their frequencies in a mission life while designing the data storage system. Depending on the memory being selected, certain design techniques have to be adopted for reliable operation of a data storage system for space application.

To enhance the reliable operation of flash memory in space environment, certain design techniques have been indicated for space application by domain experts. Major design techniques are listed below.

First, up-screening is mandatory for the selected flash memory devices [1]. Since latch up is still an issue which can result in permanent failure for certain devices, there is a need to provide memory isolation feature when the situation demands and to increase memory failure tolerance.

Further, size of the blocks, number of pages for each block, data retention time and endurance are the other parameters of the flash which need to be considered while designing a system [8]. The manufacturer of the device will state these parameters in the data sheet.

Fault tolerance mechanisms shall be systematically applied to increase reliability and endurance of these devices[1]. In particular, redundancy must be built into the system to ensure data integrity during its operating lifetime.

Further, results of the radiation tests carried out on the selected devices needs to be studied to understand SEE error rates and patterns. In a case of absence of radiation test results, devices need to be fully characterized independently to understand its behavior to irradiation and to incorporate appropriate error correction codes (ECC).

As per manufacturer and independent studies, flash memories have random failures. Hence, the common ECCs techniques of SDRAM such as simple Hamming codes cannot be directly applied to flash devices. Bose-Chaudhuri-Hocquenghem (BCH), low density parity check (LDPC), and so on may be a suitable choice [1]. Reed-Solomon codes were also indicated in the literatures [5]. Choosing the most suitable ECC for a specific mission is always a trade-off among design parameters.

Also, it has been experimentally verified that Single event functional interrupts(SEFI) and single event latchup (SEL) errors can be removed by reset or power cycling (i.e., switching off and on the memory) without any loss of data [1]. Hence, it is essential to provide local reset and power on/off features.

V. APPROACH

The approach for induction of the flash memory based mass storage system to space program can be as depicted in the figure 3. The design and development of the flash memory based mass storage system start with the literature survey regarding the experiments that have been carried out in recent past to understand the behavior of flash memory in space environment. After the literature survey, suitable flash memory device will be identified for the application considering its electrical, thermal, packaging, assembly process and radiation tolerance specifications. The device from the established vendor will be considered while selecting the devices. As part of acceptance criteria, the selected device will be subjected to up-screening tests. Subsequently, specifications, quality aspects and up-screening test results of the selected device will be subjected to review process.

The next step in the activities is the design process. The design activities can start with the DRAM based mass storage system as the baseline configuration. The development of memory control logic for FLASH memory is the critical element of the design. The control logic circuit can be realized in a Field Programmable Gate Array (FPGA) device. The flash memory control logic and associated circuits need to be designed for space application considering the criteria indicated by the domain experts. The memory control logic needs to be built with mitigation techniques to overcome constrains imposed by space radiation. At the end of the design, the analysis will be carried out as part of the design activities. It includes functional, timing, power and thermal analysis

of the system. The design analysis results will be subjected to review by peer committee.

After the review process, design verification model will be developed and tested to verify the implementation of the design. After successful completion of the design

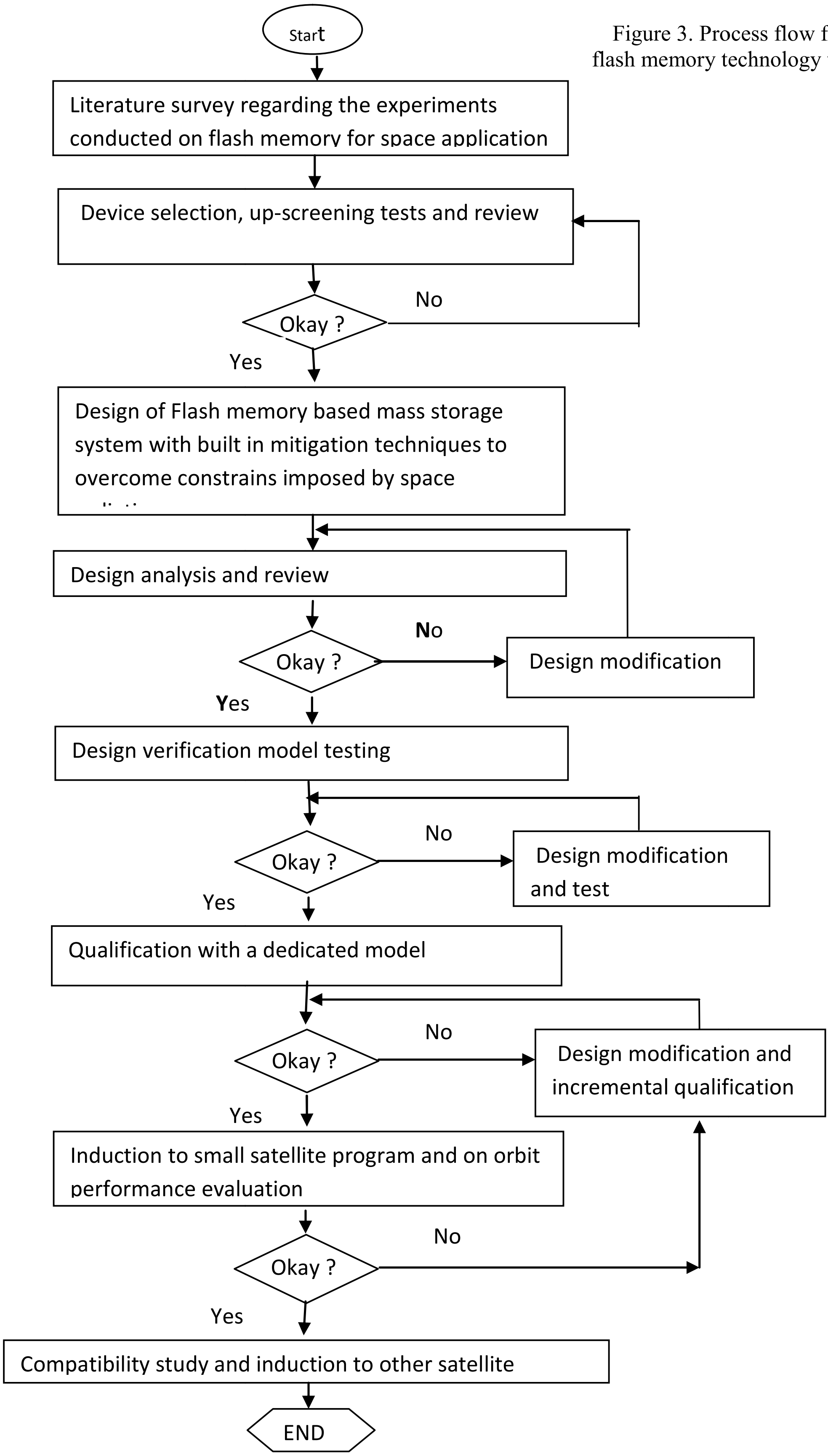

Figure 3. Process flow for induction of flash memory technology to space program

verification model tests, qualification model will be developed for design margin demonstration with respect to electrical, thermal and mechanical design specifications [7]. The qualification model will be subjected to series of electrical and environmental tests. The test levels will be higher than the expected for the system during storage, transportation, launch and on orbit. The qualification test levels include the margin over the expected level for the hardware. Flight hardware fabrication process will start after successful completion of the qualification

The flight model will be realized with those flash memory devices which have undergone up-screening tests. Later, the flight model will be subjected to series of acceptance tests at unit level prior to integrated test at spacecraft.

To begin with, flash memory can be attempted in small satellite program. On orbit performance of the flash memory based mass storage system needs to be monitored after launch. In addition to its on orbit performance, the adequacy of the mitigation techniques adopted in the design, needs to be assessed at regular interval. Based on its performance, necessary corrective measures need to be incorporated in the next version of the flight hardware. After successful induction of the flash based mass storage system to small satellite program, it can be attempted in other program too.

VI. IMPLEMENTATION PLAN

Implementation of flash based data storage starts with DRAM based mass storage system as the baseline configuration. The typical block diagram of the data storage system is shown in figure 4.

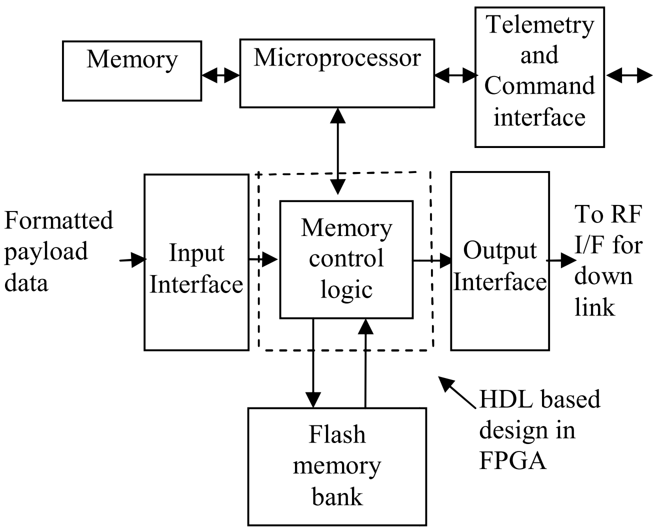

Figure 4. Functional block diagram of data storage system

It is a processor based system and consists of 'N' number of memory banks. The flash memory control logic will be designed with built in mitigation techniques to take care of soft error and hard failures due to radiation. The HDL (Hardware description language) based design will be realized in a FPGA device with built in Triple Module Rredundancy (TMR).

The data received from the payload in pre-specified format will be recorded in the system. The recorded data will be transmitted down to earth through RF system. The system gets the supply from the onboard power system. Further, it has an interface with onboard computer for commanding and monitoring the health parameters of data storage system[7].

Basic operating modes of flash memory includes block wise erase, page program and page read[8]. Based on the input received from the processor, these operations are carried out by memory control logic.

In the nominal mode, before writing the data into flash memory, coding is done on the received data from the input. Decoding is done on the data read from the memory. Coding scheme will be selected such that it will be able to address both random and burst error. FIFO will be incorporated at the input interface to handle different input and output data rate. In erase mode, contents of the specified block will be erased. There will be an option to disable coding in the logic. Redundancy will be provided for flash memory devices. Further, self test mode will be incorporated in the design. Objective of self test mode is to identify the fault developed at later stage. Faulty devices will be isolated from further activities. Isolation feature needs to address isolation of the faulty memory from other memory and power supply.

After successful implementation of the design, system will be subjected to series of tests and review as indicated in the figure 3.

VII. CONCLUSION

Flash technology has been considered for replacing the well-established DRAMs for their high storage density, low power, low cost, and high data throughput.

This paper provides details about outcome of the experiments conducted on flash memory technology in the past to study the impact of particle radiation, design parameters of flash memory which need to be considered for space application. The typical approach and implementation plan for induction of the flash memory based mass storage system to space program is also provided in this paper.

Flash memory intended for space application is available from established vendor. However, it becomes necessary to study the results of the radiation tests carried out on the selected devices to understand SEE error rates and patterns. It helps in incorporating appropriate design techniques to overcome the limitations. Same approach needs to be adopted when flash device of smaller size is adopted for the first time.

To conclude, flash memory appears to be the future semiconductor storage technology for mass storage in space systems provided suitable design techniques are

adopted in the design. To begin with, flash memory can be attempted in small satellite program.

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Small Satellites and COTS Philosophy : An Integrated Assessment

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Abstract : Satellite based space services have become an integral part of our lives. In recent times, the progress in micro-electronics, VLSI, miniaturization, consumer electronics etc., have given rise and scope to realize Small Satellites to give performances comparable to many of the earlier bigger satellites. Additionally, the growth of Internet and Googalization of society has created the need for data / information to be available in near real time. This has given impetus to small satellite constellations and trends toward mass manufacturing aspects to reduce cost and cycle times. This approach has given scope to COTS philosophy (Commercial off-the-shelf) to lower costs and simpler missions in large numbers. It has also led to Student Satellites in Academia due to affordability which has boosted R & D as seen by the success of Cubesat class of satellites. Essentially, COTS has given scope to democratization of space services based on small satellites driven by venture capital / silicon valley concepts as seen by the success of Planet Labs. The graceful degradation of space service is now possible in a small satellite constellation configuration based on COTS compared to the total failure situation of the earlier large single spacecraft based on Hi-Rel components.

In this paper, our objective is to present the integrated perspective of the recent trends in Small Satellites Systems, COTS philosophy and R & QA. Satellite R & QA needs to be suitably organized along different tracks based on missions / application.
– Hi-Rel based on redundancy, space qualified and Rad-Hardened & space qualified components for High-Cost / Long life mission programmes e.g., GEO-Communication Satellites
- Adaptive R& QA based on mix of components with enhanced role for COTS for Low Cost / Constellations / Shorter Mission Life programmes especially for Small Satellites in LEO orbits.
Key words : COTS, Small Satellites, Cubesats, R & QA, Constellation

I. INTRODUCTION

Spacecraft designers need to consider the satellite from System Engineering point of view. A major factor that contributes to the expense associated with satellites is the launch cost of putting it into orbit along with the insurance costs. Satellites are also affected by damage or down times. Sometimes, a launch may not be successful and results in a multi-million loss to the space agency. Satellites and space systems have traditionally used expensive radiation tolerant, radiation hardened or at-least military qualified parts for computational and other subsystems to ensure reliability in the harsh environment of space[1,2].

Thus, due to the high cost, limited number of manufacturers and extremely specialized testing, radiation hardened ICs are limited in scope. This has encouraged the designers of space systems to adopt commercial components wherever possible for space applications in recent times. This is clearly evident from NASA's "Faster-Better-Cheaper" approach to space programmes[3].

The enormous progress in micro-electronics, VLSI, miniaturization etc., have enabled Small Satellites to give performances comparable to earlier bigger satellites. During the last decade, the importance of Small Satellites has increased significantly as seen by ONEWEB, SKYBOX (now renamed as Terra Bella) etc., Small Satellites is now a global multi-billion dollar business. The success of the recent Planetlabs shows the potential of Cubesats for even operational services. Constellations based on small satellites and trends toward manufacturing aspects to reduce the cycle times based on COTS, shorter life spans / simpler missions became acceptable for lower costs.

The R & QA aspects have also evolved in parallel based on the cost and mission life considerations, graceful degradation based on COTS philosophy / constellations. It is a major paradigm shift from the earlier big satellite approach for complex multi-purpose missions with long life spans that actually put a high demand on R & QA aspects such Hi-Rel components, rad-hard components, redundancy in systems / complex configurations etc., and need for big launch vehicles.

Section 2 traces the historic case study of C2-BMU and SRE-MMU on the Integrated framework of Reliability / Redundancy / Components / Mission Life. Section 3 explains how COTS has enanbled low cost access to space. Sections 4 and 5 show the evolution of COTS in Cubesats and Microsats. Section 6 shows the evolving trends in R & QA practices. Section 7 gives the conclusion.

II CARTOSAT-2 AND SRE : CASE STUDY OF COMPONENTS AND R & QA IN BMU – MMU

	Cartosat-2	SRE
Mission Life	Greater than 5 years	Initial plan was less than 3 months. Finally mission objectives were achieved in less than 2 weeks with the deboost operation.
Components	Space Qualified devices – Class-S / QML-V / RH	A mix of Space qualified / Rad Tolerant and Mil-Grade / commercial grade components
FPGA devices	Radiation Hardened	Radiation Tolerant
Redundancy	Dual System	Single System
Powering	Always powered during the mission	Spacecraft logics always powered while re-entry logics powered only before deboost operations. Reliability enhanced by cold start provision.
Radiation / components	TID taken into account for more than 5 years. Hence, Space qualified, RH components used	TID taken into account for less than 3 months. Hence, Rad Tol devices / Mil Grade / upscreened industry components used suitably for S/C and re-entry logics

Table 1 C2-BMU & SRE-MMU

The case study of Cartosat-2 Spacecraft BMU and SRE Mission Management Unit is presented to highlight the integrated framework of R & QA / Redundancy / COTS / Mission Life on the On-Board Computer System of a Spacecraft (close to Small Satellite class for the dual launch of PSLV Jan 2007). The mission life of Cartosat-2 was expected to be more than 5 years where as the mission life of SRE was expected to be less than 3 months. Cartosat-2 is an advanced remote sensing satellite with panchromatic camera as payload which is capable of providing scene specific imageries at high spatial resolution. It required Hi-Rel Components and Redundancy based approach (main and redundant systems for the On-Board Computer System known as BMU) to achieve reliability. The SRE project had the objective to develop a recoverable capsule, launch it on board PSLV to a Low Earth Orbit, conduct micro-gravity experiments, deorbit and recover it in Indian waters. As it was a short duration mission, a single On-board Computer system known as Mission Management Unit (MMU) was used along with components based on application requirements. The powering scheme was also suitably configured for reliability as Rentry logics were powered only during the final deboost phase. The data corresponding to various TM parameters of SRE mission are stored and downloaded during short visibilities over Saskatoon, Lucknow and SHAR. The storage was done in EEPROMs. The selection of components for the Spacecraft Logics / Re-Entry Logics is a case study based on mission / application and R & QA requirements.

III EVOLUTION OF COTS INTO AVIONICS / SMALL SATELLITES FOR LOW COST ACCESS TO SPACE

One of the biggest drivers of traditional spacecraft cost is the requirement to use high-reliability space-qualified components. However, there is presently an increasing trend to develop and fly low- cost spacecraft with rapid development schedules. This trend makes the use of traditional space-qualified components less appropriate, due to long lead and procurement times associated with many of these components. While the parts themselves may be very similar (or even identical) to their lower-cost commercial equivalents, the additional cost of parts programs, testing, analysis, reliability engineering, and acceptance data packages increase the cost. There is a growing gap between the performance of commercial electronic components and that of their Rad-Tol and Rad hard counterparts. Although the use of COTS components is limited, it is nevertheless increasing, particularly when they provide system-level performance that their Hi-Rel/Rad-Tol counterparts cannot achieve (e.g processors), and/or where there is a substantial quantity effect (e.g. memory components for mass memory units) Today, due to enhanced quality in components, the EEE Parts Engineer needs to understand the part application rather than just selecting parts from an approved parts list [4,5,6].

“Small-Sats” (micro-, nano etc.,) are part of the solution to the enormous expense of traditional aerospace. As launch costs are a significant portion of a satellite deployment cost, simply making satellites smaller is a first step in breaking the inflationary cost cycle. Commercial components can withstand radiation dose up

to 5 krad by using multi-layer insulation or other shielding techniques. Radiation dose of 5krad is not a serious problem for LEO satellites at an altitude of 500-700 km. This has fuelled the growth of COTS especially in Small Satellites / Constellations and Factory Model for its realization as seen by the recent launch of over 80+ Cubesats of PLANETLABS by PSLV-C37 .

Driven by the personal computer and personal communications markets, commercial-off-the-shelf (COTS) microelectronic systems have advanced considerably in the last few years. It is now feasible to realize capable small satellites to provide cost-effective and rapid-response space missions which are boosting Small Satellites. The biggest growth in commercial satellites is with the low-cost constellations which use a lot of commercial products and achieve radiation mitigation and reliability through non-conventional means. An integrated approach has evolved for Small Satellites / COTS and R &QA.

IV CUBESATS

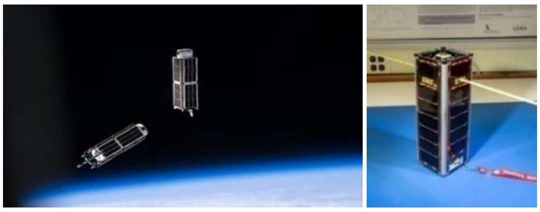

Figure 1: A set of NanoRacks' CubeSats as photographed aboard the International Space Station. Photo courtesy of NASA.

A CubeSat is a miniaturized satellite for space research that is made up of multiples of 10×10×11.35 cm cubic units (1U) and often use COTS components for their electronics and structure. In 1999, California Polytechnic State University and Stanford University developed the CubeSat specifications to promote and develop the skills necessary for design, manufacture, and testing of Nano satellites. They were intended for LEO to perform scientific research functions and explore new space technologies. Academia accounted for majority of CubeSat in the early days and in recent times, CubeSats were being realized in company / start-up mode. The CubeSat reduced the cost of deployment and ensured suitability for launch in multiples, using the excess capacity of larger launch vehicles or via ISS. Hence, it gave opportunity for trade off between COTS Vs. Mission Life with adequate care in electronics device selection w.r.t tolerance to radiation. For Low Earth Orbits(LEO) small life missions, radiation can largely be ignored & standard consumer grade electronics may be used as the chance of a single event upset (SEU) is very low. However, for sustained LEO operations lasting months or a few years, additional precautions need to be taken to mitigate radiation effects. CubeSats are very small – nominally four to five kg for a 3U or "triple" – and limited in volume, and can be scaled up to even 6U. This could be a tremendous value position in terms of more capability, performance, and utility [7, 8].

UK's first nano-satellite: **SNAP-1 (** 3U cubesat, 5kg) designed and built by Surrey Space Centre (SSC) and Surrey Satellite Technology Ltd (SSTL) staff demonstrated that a sophisticated nano-satellite can be constructed rapidly, and at very low cost, using an extension of the modular-COTS-based design philosophy. SNAP-1 was successfully lofted into orbit on June 28th 2000 from the Plesetsk cosmodrome on-board a Russian Cosmos launch vehicle. SNAP-1 became the first nano-satellite to demonstrate full attitude and orbit control via its miniature momentum-wheel-based attitude control system and its butane-propellant-based propulsion system. A major achievement in this COTS approach is in the simplification of testing as modules are integrated with standard connectors. SNAP-1 uses the 32 bit ARM RISC processor & standard CAN interface for data transfer. Programming is done in C language. It uses body mounted panels to simplify the power system. The less than £1M mission cost is due to COTS approach[8,22].

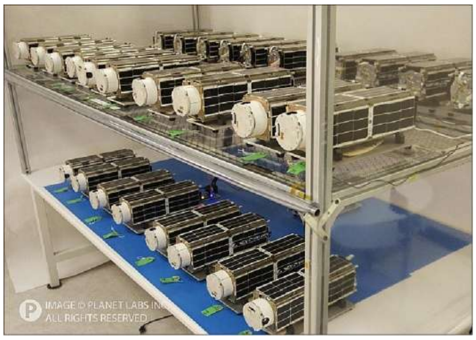

Figure 2 Doves (nano-satellites) before being sent to the launch site (image credit: Planet Labs).

Planet Labs, Inc. is an American Earth imaging private company based in San Francisco, CA. The company designs and manufactures CubeSat miniature satellites called Doves (3U, 5Kg) that are then delivered into orbit as passengers on other missions. Each Dove Earth observation satellite continuously scans Earth, sending data once it passes over a ground station. Together, Doves form a satellite constellation that provides a complete image of Earth at 3-5 m optical resolution and open data access. Small size and a relatively low cost enable the company to quickly prototype and test new designs. The images gathered by Doves provide up-to-date information relevant to climate monitoring, crop yield prediction, urban planning, and disaster response. The nanosats of Planet Labs provide much of the

performance of a conventional satellite for a fraction of the cost based on COTS philosophy. There are other cost-saving measures. Satellites are usually built in elaborate clean rooms, but Planet Labs assembles its nanosats in “clean-enough” rooms in its downtown offices[9,10].

The **STRaND programme** builds upon the successful SNAP-I nanosatellite mission, launched in 2000. It improves on the CubeSats as it flies a modern commercial off-the-shelf (COTS) Android Smartphone as a payload, along with a suite of advanced attitude and orbit technologies developed by the University of Surrey and CubeSense from the University of Stellenbosch in South Africa. STRaND-I is also different as anyone will be eligible to fly their "app" in space, for free.

STRaND-1 started out as a feasibility study and mission requirement exercise in the Mission Concepts team at SSTL in the February of 2010. The aim of the study was to answer the question: ‘what could be done do to harness the miniaturisation revolution of consumer electronics of the last 10 years (i.e. since SNAP-1)?’.

The innovative STRaND-1 CubeSate was built and tested in just 3 months. It demonstrated the feasibility of using low cost smartphone electronics to control a spacecraft. STRaND-1 is operated by two computers: one is classic CubeSat computer and second is a Google Nexus One smartphone with an Android operating system. The smartphone was intended to provide cameras, accelerometers and high-performance computer processors - almost everything except solar panels and propulsion. During the first phase of the mission STRaND-1 was intended to use a number of experimental apps to collect data, while a new high-speed Linux-based CubeSat computer developed by SSC takes care of the satellite. During phase two the STRaND team intended to switch the satellite's in-orbit operations to the Smartphone, thereby testing the capabilities of a number of standard smartphone components in a space environment.[11,12]

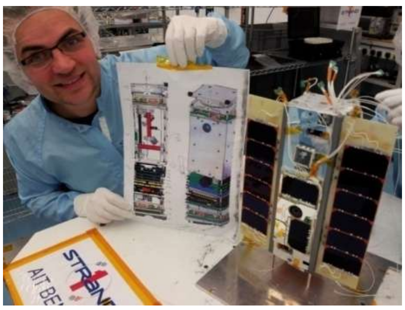

Figure 3 STRaND-1 is Smartphone-Cubesat (3U)

V MICROSATS

The traditional, large spacecraft capture data at the high resolution but because of their enormous capital cost (and, hence, limited numbers), they produce data too infrequently to enable multiple monitoring or change detection applications. Today, Cube-sats can be launched in large numbers due to their lower costs but can’t produce data with high enough resolution to monitor economic-scale change (cars in parking lots, ships in ports, supply chain monitoring etc.,. Hence, a system must both capture data of high enough quality (resolution) to monitor economic activity and also be cost-effective enough to deploy in large numbers for revist (timeliness).

Traditional Satellite imaging companies like DigitalGlobe have long been launching expensive spacecraft with powerful cameras into high orbits. However, the expensive images can only be updated based on the revisit frequency i.e., only when the slowly orbiting satellite hovers above the spot again.

Microsats (satellites with masses on the order of 100+kg) are finding increasing utility as scaled-down providers of services and capabilities traditionally associated with much larger satellites. The traditional satellite design paradigm has been modified to develop low-cost, responsive microsats. The operational life and functional reliability / availability of space service is now seen w.r.t a Small Satellite constellation / COTS as compared to the earlier single large spacecraft based on Hi-rel components and complex design & configurations with redundancy at different levels.

Since most businesses are interested in economic activities, the most valuable data is high resolution data (1m) and temporal scales (daily revists). Existing Earth Observation (EO) systems based on Hi-Rel components have not been able to meet the need of many business applications as they lack the critical combination of timeliness and high resolution imaging [13,14].

The **Skybox vision (Google-Terrabella)** aims to leverage timely satellite data to provide insight into daily global activity. Such data has enormous value in industries such as agriculture, asset monitoring, security, supply chain management and many more. Berkenstock and his three Skybox co-founders visualized a radically low cost imaging satellite. The Skybox team aimed to find the golden mean between CubeSats, which were too small to collect high resolution images, and the prohibitively expensive NASA-grade imaging satellites. So they configured a Microsat and found higher-grade components and clever workarounds wherever they could.

Traditional imaging satellites work like a line scanner, capturing images row by row. Complex onboard systems then assemble those thousands of rows into images and send them back to Earth. The critical leap with Skybox is that it has developed an inexpensive Micro satellite that

flies at a lower orbit. Skybox aims to take pictures with greater frequency in constellations mode. Regularly revising Google Maps with fresh imagery could lead to “a whole bunch of new applications. Skybox has creatively combined technologies from a half-dozen consumer products to alter the business of satellite imagery.

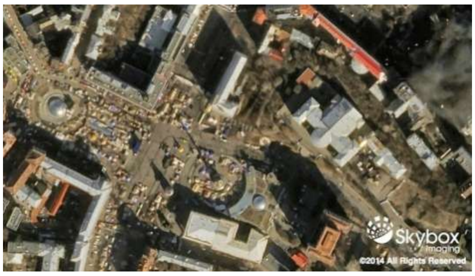

Fig 4. Imagery of Kiev - Skybox

The Skybox satellite uses

- a two-dimensional video sensor created for night-vision goggles
- electronics borrowed from high-end digital cameras to capture video.
- software, adapted from Magnetic Resonance Imaging (MRI) and ultrasound machines, which reads the data from the sensors and compresses it in real-time before it is sent similar to DirectTV.

The video data is parsed and reassembled into useful high-resolution images on the ground, allowing Skybox to build much simpler (and therefore smaller and cheaper) satellites. SkySat-1 is one of the highest performance micro-satellite ever built. It has delivered terabytes of spectacular sub-meter imagery and video - data of incredible business value - at a cost more than an order of magnitude less than comparable existing systems. The success of SkySat-1 is an achievement in combining tightly integrated system architecture, modularity, leverage of the incredible performance of modern commercial-off-the-shelf (COTS) components in space and the best engineering practices in the industry [15,16,17].

A. A Low-Cost, Responsive MicrosatBus MMB – 100 Utilizing by SpacDev

SpaceDev (OTCBB: SPDV) developed a new high performance microsatellite product program named the SpaceDev Modular Microsat Bus. The SpaceDev MMB-100 Microsat is a highly capable modular 100 kg (220 pound) microsatellite based on industry standard "Plug-n-Play" interfaces. In addition to standard Ethernet and USB interfaces, the SpaceDev MMB-100 uses a real-time Linux operating system, and uses CORBA-based object oriented interfaces for subsystems as well as commanding from the ground via the Internet. The basic SpaceDev MMB-100 Bus is expected to price at less than $10 million, excluding the payload and payload integration[49].

The SpaceDev MMB-100 spacecraft platform is a single-string 100-kg class microsat that is suitable for experiments, flight demonstrations, and highly-responsive missions. It is designed specifically for 1-2 year LEO missions. It has flexible launch options, including the ESPA ring and the SpaceX Falcon launch vehicle. The MMB-100 makes extensive use of commercial off-the-shelf (COTS) parts and software, which enables low cost and rapid development times. The MMB-100 is a significant departure from conventional spacecraft design practices, and will enable a new generation of small, low-cost satellites [18].

B. XSAT

Current small satellite missions generally do not have high computational power onboard due to limitations of power, space, volume or budget. XSat provides a cost-effective way of designing space computing architectures that enable reliability, despite the usage of COTS components.

XSat is a 120kg Polar and Sun-synchronous Low Earth Orbit (LEO) micro-satellite developed by CREST (Centre of Research for Satellite Technologies). CREST is a joint project team set up by Nanyang Technological University and the DSO National Laboratories of Singapore. The primary mission is to carry out image acquisition, storage and download of images from a multi-spectral camera payload, called IRIS. The Parallel Processing Unit (PPU) payload is a research payload used to demonstrate high performance computing in space. It contains 20 StrongARM processors (COTS) connected to perform parallel processing on the images captured by the IRIS camera. The PPU is connected to the Solid State Recorder (SSR) where the IRIS images are stored after acquisition. The SSR is also used to store the processed image for subsequent downlink to the ground reception station. [19,20].

VI R & QA FOR SMALL SATELLITES / COTS

The major features of R & QA in a traditional Spacecraft Programme are

- Usage of high-rel components
- Derating
- Redundancy
- Extensive Testing and Qualification
- Significant role for simulation studies

Motivations for using COTS components is essentially for reducing system life costs. Improved launch access to <u>space</u> is helping to drive the <u>small</u> satellite market and is behind a new focus on using small systems. Now that it’s

possible to readily place small satellites on launch systems being sent up to the International Space Station or to low-Earth orbit (LEO) at a fraction of the cost compared to in the past – for hundreds of thousands of dollars now, rather than millions – and on a fairly regular basis and finding alternate ways to use space & create new applications / capabilities.

Underwood [21] described the effects of radiation on COTS components in LEO orbits :
"Twenty years of experience have shown that low-cost, rapidly built spacecraft based upon COTS technologies are very practical. Total-dose effects show up in COTS devices at 5 krad (Si) and begin to be a threat to the mission at 10-12krad (Si).

A case study is presented to present the in-orbit results of COTS components w.r.t radiation and reliability in Small Satellites. On 10th August 1992, the S80/T and KITSAT-I micro satellites were launched alongside the TOPEX/ Poseidon ocean monitoring satellite, into a relatively high 1305 x 1325 km, **66.1”** inclination orbit. This orbit causes the satellites to spend a significant proportion of their time exposed to the trapped protons of the inner Van Allen belt, providing an opportunity to examine the in-orbit performance of COTS data handling devices (e.g. memories and processors) under relatively high radiation-flux conditions. These satellites both utilise Surrey’s “UoSAT” standard 50 kg micro-satellite bus, which has data-handling systems comprising an Intel 8OC186 processor-based primary on-board computer (OBC- **186),** and an associated solid-state data recorder (which we call a RAMDISK) implemented using commercial, non-hardened, high-density 128K-bit and 1 M-bit static RAMS. Such COTS devices are particularly attractive for small satellites which typically have very severe power, mass and volume constraints, and which are often subjected to stringent cost control and fast “design-to-orbit’’ schedules.

Observations of single-event effects (SEES) and total-dose degradation are presented for the data-handling system of the S80/T and KITSAT-I micro-satellites, which have been operating for six years in a 1,320 km altitude, **66”** inclination orbit, and which are comprised almost entirely of (COTS) components. The radiation environment inside both spacecraft is inferred from measurements made by the radiation monitoring payload carried on-board KITSAT-1. Ground-based radiation testing of samples of the COTS devices (including flight spares) using proton and heavy-ion beams, has allowed comparisons to be made between the observed performance of the devices under this radiation environment, and predictions made using standard models. The conclusion is that, whilst the accumulated radiation damage is likely to cause the spacecraft to fail in the near future, the use of COTS devices coupled with a not-too conservative design, has enabled the satellite to carry out its intended mission rapidly and at very low cost. Several years of practical experience have shown that low-cost spacecraft based upon COTS technologies are a realistic proposition for low-Earth orbit. The S8WT and KITSAT-I missions have shown that satellites can survive radiation environment, and perform for several years[21]..

Frequently, very long delivery times or other restrictive practices such as, excessive minimum purchase requirements place Hi-Rel components out of reach for the small manufacturer. With today’s emphasis on moving towards a more frequent “smaller, faster, cheaper” approach to space access, COTS has emerged as a major option. Due to market pressures, fewer volume manufacturers will continue to support space. Moreover, the failure rates for integrated circuits have been falling significantly. As the number of Hi-Rel component suppliers diminishes, the organizations running space standardization and approval systems will have to adopt a mix of COTS and Hi-Rel components based on mission / application considerations.

Satellite R & QA needs to be suitably organized along different tracks based on missions / application / programmes. A Two-Track policy can be considered
– Hi-Rel based on redundancy, space qualified and Rad-Hardened & space qualified components for High-Cost / Long life mission programmes e.g., GEO-Communication Satellites
- Adaptive R& QA based on mix of components with enhanced role for COTS for Low Cost / Constellations / Shorter Mission Life programmes especially for Small Satellites in LEO orbits.

VII CONCLUSION

The spacecraft industry is witnessing revolutionary trends in system realization due to user demands, obsolescence of technology, rapid strides in miniaturization efforts and global competitiveness especially in the domain of Small Satellites. Consequently technology inversion (Development Vs User demands), complexity inversion (space systems Vs ground systems), small / micro-mini satellite efforts, coupled with the need to produce systems, **faster, cheaper and better** have resulted in a relook for small satellites. It’s really more of an acceptance of risk and finding ways to maneuver around and mitigate that risk to be more successful and to realize all the cost and schedule savings that can come from it.
The quality in component manufacturing processes has been steadily increasing over the years. The design to obsolescence life cycle is having ever decreasing time spans. To make use of new devices for a viable period before obsolescence it is necessary to make an early evaluation of the component and be ready to have a

replacement in line before this product becomes unavailable. This situation can only be fully exploited within a programme of frequent mission opportunities with rapid turn around times. The rapid increase in component functionality means that system performance can potentially increase at a similar rate, usually accompanied by price reductions.

A new engineering philosophy has evolved addressing the many different issues that are relevant to "COTS" usage. This philosophy relies on sound engineering practice while ensuring that the specified quality of a component is maintained for the mission requirements in place of the Hi-Rel components used in traditional large spacecraft. Hence, component selection, design configurations and applications provide a viable alternative to conventional qualification methods to achieve expected results. COTS and CONSTELLATIONs have influenced the Factory Model for Small Satellites as it is now seen from a manufacturing perspective to further lower COSTs. The recent launch ofover 80+ Cubesats of PLANETLABS by PSLV-C37 shows the remarkable impact and contribution of COTS towards Small Satellites.

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Overview of COTS Component Selection, Qualification, Subsystem Engineering, Redundancy Techniques and Testing for Nanosatellites

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Abstract-Recent advances in VLSI electronic components has accelerated the use of commercial of the Shelf (COTS) Components in small satellite programmes, significantly contributing towards a 'faster, cheaper and arguably better' approach to space missions. Such applications however, in combination with the fundamental inconsistencies of COTS heritage require some differing techniques to those of the established space engineering regimes. In this Article COTS component selection, qualification, subsystem engineering, redundancy techniques, testing aspects and case studies for Nanosatellites have been discussed.

Keywords: COTS, satellite, selection, reliability, redundancy, fault tolerant

I. INTRODUCTION

Space, with long mission time and higher mission costs has relied extensively on Mil standard components for realization of space satellites. The historic reasons for dismissing COTS devices in place of Mil/Space grade parts in the design of satellites are lack of hermeticity, inadequate manufacturing traceability and a reduction in environmental specifications including radiation. A quick look at space history would indicate that COTS parts were used in sounding rockets. Furthermore, the rapid development cycle of modern microelectronics devices and their packaging profiles for the commercial and domestic markets constitute a radical departure from the assurance base offered by the now dwindling Mil Standard component lines. But off late COTS components are being considered and extensively used in the design of Nanosatellites and this is the motivation to write this paper.

II. WHAT IS COTS:

"COTS" implies any grade which is not space qualified and not radiation hardened. Below are the grades

- Commercial: 0°C to +70°C
- Industrial: -40°C to +85°C
- Extended Industrial: -40°C to + 100°C
- Automotive grade: -40°C to + 125°C
- Mil/Space grade: -55°C to + 125°C
- 99% of COTS are Plastic Encapsulated Microcircuits (PEMs).

The most obvious parts difference w.r.t Mil grade parts are in terms of packaging, operating & storage temperature, electrical & physical characterization, and screening. COTS parts must be evaluated and qualified before being used in space projects.

a. ADVANTAGES OF COTS:

They are cheaper due to large volume production, general purpose being more flexible for different applications, shortens design-to-production cycles, larger user base generally uncovers design defects early, provides current technology solutions. Emerging technology tends to be backward compatible with legacy products and avoids binding solution to single hardware/software.

b. DISADVANTAGES OF COTS:

They are not suitable for all applications; highly deterministic performances may require special operating system; environmental constraints like temperature, radiation exposure and corrosive exposure; packaging like size, weight and shape and further may not meet reliability requirements of mission critical systems without qualification or upscreening or redundancy. COTS binds user market trends- critical components may become unavailable and impossible to reproduce.

c. Reasons to go for COTS:

The changes in the supply of Mil and Hi-Rel devices, scale down in manufacture of Mil components; less lead times for procurement; small minimum order of quantity frequent need of "Smaller, Faster, Cheaper" approach for space, low cost and need for frequent, less complex missions with faster response times lead to a dramatic user culture change.

d. Current status of COTS:

COTS components offer massive increase in coverage, features and performance; COTS have routinely used in every satellite (Viz., MYRIADE and GAIA) as part of main bus system. There is indication of improving quality when components are manufactured by highly automated processes and in vast quantities. The quality in component manufacturing processes has been steadily increasing over the years.

2.5 Quality Indicators of COTS:

Designers along with QA should visit the distributors and check out their handling, storage, packaging and pre-delivery general processes. Always look at the delivered state of goods from the distributor; individual components inspection; components should be in sealed bags and it is preferable they remain in these until required for use. Set up suitable in-house regimes to provide secure storage.

III. COTS COMPONENT SELECTION:

COTS selection done in close collaboration between the design team and the product assurance team. Designers shall choose as a priority the "most mature components from major suppliers" usually the most reliable and the longest life cycle. For radiation hardened (Rad hard) device requirement designers shall opt for minimum levels of shielding (3-5 yrs LEO). Designers can purchase rad hard devices or qualify only the inherently vulnerable devices such as A/D converter, memories and FPGAs. Designers are advised to choose components that are conservative w.r.t. power dissipation and voltage stress; Handling and mounting techniques are important for new component styles; Mechanical issues such as launch survivability of the component and its method of mounting can be evaluated fairly easily with a vibration proof test using a representative sub assembly housing a test board populated with all new components requiring evaluation. Derating COTS devices with derating factors more than MIL-975M or refer to literature since there is no standard available for derating of COTS parts. Select COTS devices from successful missions. Its an indication that other items in the same batch being to the same standard (space heritage-COTS).

a. Notional EEE Parts Selection:

A few details on the matrix shown in figure 1.

When to test:

– "Optional"
  • Implies that you might get away without this, but there's residual risk.

– "Suggested"
  • Implies that it is good idea to do this, and likely some risk if you don't.

– "Recommended"
  • Implies that this really should be done or you'll definitely have some risk.

– Where just the item is listed (like "full upscreening for COTS")

This should be done to meet the criticality and environment/lifetime concerns.

Criticality				
	High	Level 1 or 2 suggested. COTS upscreening/ testing recommended. Fault tolerant designs for COTS.	Level 1 or 2, rad hard suggested. Full upscreening for COTS. Fault tolerant designs for COTS.	Level 1 or 2, rad hard recommended. Full upscreening for COTS. Fault tolerant designs for COTS.
	Medium	COTS upscreening/ testing recommended. Fault-tolerance suggested	COTS upscreening/ testing recommended. Fault-tolerance recommended	Level 1 or 2, rad hard suggested. Full upscreening for COTS. Fault tolerant designs for COTS.
	Low	COTS upscreening/ testing optional. Do no harm (to others)	COTS upscreening/ testing recommended. Fault-tolerance suggested. Do no harm (to others)	Rad hard suggested. COTS upscreening/ testing recommended. Fault tolerance recommended
		Low	Medium	High
		Environment/Lifetime		

Fig.1: Notional EEE parts selection matrix

The higher the level of risk acceptance by a mission, the higher the consideration for performing alternate assembly level testing versus traditional part level. All fault tolerance must be validated. Good mission planning by the project identifies where on the matrix a EEE part lies.

IV. COTS PROCUREMENT:

Designers shall obtain single lot of components with single date code of encapsulation and preferably single foundry lot. The knowledge, the quality and the control of the procurement chain is important to keep an efficient traceability and to avoid counterfeit parts (Up to 20 % of IC lots from non official distributors are counterfeit). Usually a strategic stock is done to face short life cycle of COTS. When manufacturer are aware of a bug in a HiRel component, users are generally notified. This is not always the case with COTS this can have serious impacts, financially and/or from a planning perspective. Short life cycle of COTS w.r.t. a 5-8 year satellite life cycle,

designers can go for strategic stock and reuse capability. Long term storage COTS are more subject to (strategic stock).

a. COTS Qualification:

The qualification tests depend on the "Quality Assurance" level of the project. On one hand, COTS must be evaluated and qualified before being used in space projects: "use as is" approach is extremely inadvisable
On the other hand, tests to apply have to be adapted, and possibly reduced, with regard to the selected component and mission requirements to find the best trade-off between cost and quality.
Tests involved in the lot qualification step / "lot acceptance tests" (LAT)
Type A - Tests that are fairly conventional in all types of embedded applications, e.g.:

- Electrical characterization at three temperatures

- Construction analysis – "Destructive Physical Analysis" (DPA)
- Life-test : long-term reliability test
- Screening test/Burn-in: to pass over the first part of the 'bath curve' (to avoid infant mortality)
- Thermal cycling tests (due to differential dilatation coeff between silicon and plastic packages)
- ON/OFF power cycling tests for some missions: Earth observation payloads can require 100,000 power cycles for power optimisation and, at this time, there is very little feedback on the behaviour of plastic packaged components with regard to this way of operating

- Type B - Tests linked to some problems common to both HiRel and COTS, but to which COTS are more subject to, e.g.:
  - ✓ Damp heat tests (e.g. HAST "Highly Accelerated Stress Tests") specific to plastic packages
  - ✓ if required, some risk analysis are done to define mitigation actions, e.g.:
    - –risk of 'whiskers'
    - –risk of 'purple plague'

- Type C - Tests specific to the space domain, related to the environment or mission requirements, e.g.:
  - o TID (Total Ionisation Dose)
  - o SEL (Single Event Latchup)
  - o SEU (Single Event Upset)

4.2 Use-by date of Qualified Lot of Parts:

- LAT = authorisation to solder a lot of ICs for 7 years from the date-code

- Relifing tests = authorisation to solder such lot for 3 more years
- The lot cannot be used after this period of 7 + 3 years for space developments

Strategic storage should be accompanied by monitoring of aging of the stock, and regenerating it if required

V. MOUNTING QUALIFICATION:

The mounting of EEE parts on a PCB of each type of package has to be qualified, the associated know-how for a given company being described in its "Process identification document"(PID). PID includes facilities and tools, staff certification method, products and packages, mounting configuration, materials, soldering process, etc.

VI. SEU/SET SENSITIVITY OF COTS ICS:

The use of COTS could require to mitigate SEU/SET e.g. protection code for memories (EDAC) and Fault Tolerant (FT) architectures for micro-processors, mitigation mechanisms and architectures have to be validated e.g. FI (fault-injection).

So, w.r.t Rad Tol ICs, the use of COTS requires an additional function (SEU / SET mitigation i.e., "Software hardening" + "System hardening"), thus an extra 'validation work', it means extra cost / planning overheads. Validation of FT architectures could become a laborious work so designers have to pay attention to keep at a realistic and efficient level.

VII. COMPONENT INSPECTION:

Every component should be inspected with a view to determining exactly what has been delivered and to confirm its suitability. Ensure that the product is undamaged and always look for differences that may indicate changes in specification, variations from the constructors batch or maybe differences in materials.

Simple components such as passives or discrete semiconductor devices may provide valuable pre assembly screening information with a test of one or two parameters (look for deviations from an average value).

More sophisticated components are easier to screen when part of an assembly tested as a sub system.Non hermetic components shall undergo a long duration bake out with a slowly increasing temperature profile to minimise the effects of moisture ingress and should be implemented prior to conformal coating or other encapsulation. Items from same batch produce little spread in characteristics.

VIII. CONSTRUCTION AND ASSEMBLY:

Skills level of personnel, construction processes, build quality standards are critical for subsystem realization. Keeping all subsystems construction under one roof and within control of a small number of persons is a good practice. Any anomalies in small platforms are easier to detect and build quality can be readily checked.

IX. CASE STUDIES ON COTS PARTS:

In case study 1 (shown in Figure 2) MYRIADE micro-satellite family, developed by CNES, the French Space Agency, and first launched in 2004. Its two embedded computers were mostly developed using COTS

components for integrated circuits (except for the Telecommand and Telemetry interfaces
which used Hi-Rel/Rad-Tol ones), which enabled unrivalled relative performance regarding volume/mass for this family of satellites.

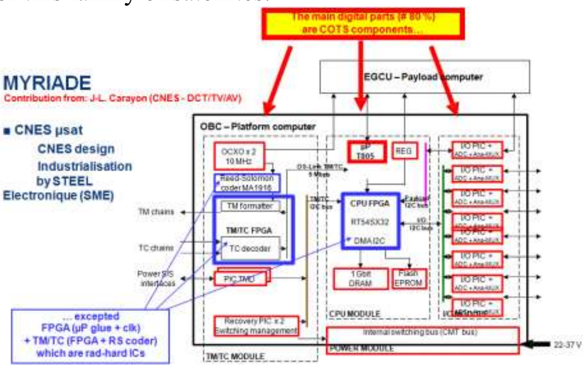

Fig.2: Case study 1 about usage of COTS

In case study 2 (shown in Figure 3) GAIA, the Billion Star Surveyor from ESA (European Space Agency), uses a processor board from MAXWELL Technologies based on the commercial PowerPC750FX from IBM; its power consumption is 20 W (typical) at maximum frequency. For GAIA, the frequency of the core of the PowerPCs has been reduced in order to reduce power consumption (which does not significantly slow down data processing in this case because the bottleneck for that project occurs mainly at the memory bandwidth level).

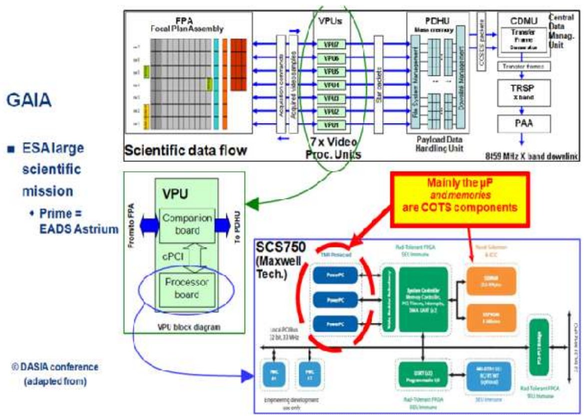

Fig.3: Case study 2 about usage of COTS

X. ENGINEERING PHILOSOPHY FOR COTS BASED SPACE SYSTEMS:

Good engineering practice includes component handling, board level design, build quality, sub assembly compatibility, system structure, interconnection techniques, safe software and modes of operation, selective use of redundant or semi-redundant design, criteria, appropriate level of quality control and best price/reliability ratio for applications not requiring the highest level of product assurance and reliability facilitates designers to achieve reliability and quality assurance in their product realization.

10. DESIGN REGIMES FOR COTS BASED SUBSYSTEMS:
At the design stage a prime consideration should be to best match the reliability requirement as dictated by sub-system importance with the product assurance confidence level in a selected component set. Such confidence perhaps coming from previous flight heritage coupled with ground based testing. Clearly a high reliability requirement should be matched to similar level of product assurance confidence. This same line of reasoning would allow the least essential sub systems to host a trial on the components with little or no flight heritage.

Component specifications are important, quality of design is function of power and mass constraints, location of subassemblies within the satellite is important (Thermal modeling and accumulated flight data can identify benign locations for items unable to withstand large thermal excursions). Thermal blankets and thermal surfaces can improve the environment of external subassemblies.

XI. HOW TO ACHIEVE RELIABILITY IN COTS BASED SYSTEMS:

Reliability of a COTS based the system is guaranteed by adopting various fault tolerant (FT) strategies. FT is a good choice for the short mission period and low-earth orbit spacecraft.
10.2 USING FAULT TOLERANCES:
Making a system more "reliable/available" can occur at many levels
– Operational
 • Ex., no operation in the South Atlantic Anomaly (proton hazard)
– System
 • Ex., redundant boxes/busses or swarms of nanosats
– Circuit/software
 • Ex., error detection and correction (EDAC) scrubbing of memory devices by an external device or processor
– Device (part)
 • Ex., triple-modular redundancy (TMR) of internal logic within the device
– Transistor
 • Ex., use of annular transistors for TID improvement
– Material
 • Ex., addition of an epi substrate to reduce SEE charge collection (or other substrate engineering)

Good engineers can invent infinite solutions, but the solution used must be adequately validated.
10.3 System Redundancies: There are various types of redundancy. A redundant sub system can be:

- Identical (if real estate is more)
- Dual (if real estate is more)
- Triple (if real estate is more)
- Cold (if real estate is more)
- Hot
- Warm (Guest takes over Host tasks before 1 sec of break-off)
- Semi redundancy (many separate and different sub assemblies all work together to form the bus systems). The complete failure of one or more subsystems will in most cases still allow total functionality but perhaps with reduced speed or accuracy or power.
- All sub systems that can survive a power down should be protected with an essential automatic power shut off facility(SEL protection).

XII. TESTING PHILOSOPHY OF COTS BASED SYSTEMS:

Component level Qualification based on mission requirements of the project. Validation of the fault tolerant features incorporated (HW and SW). Environmental test & Evaluation of subsystems followed by environmental test & evaluation of spacecraft.

a) Testing (in-house regimes):

Module level ambient functional testing. Precise records of results are retained for comparison with previous module builds and for follow up tests (quiescent current values). Thermal vacuum test (bring out subtle component failures or changes in characteristics).
Repeat detailed subsystem level testing following any environmental sessions. Subsystem temperature cycling or a burn in at elevated temperature (enhances the chances of detecting early failures). Additional thermal cycling of a fully assembled spacecraft is from -20°C to +60°C will further increase the chances of detecting early failures. More serious problems show up in thermal vacuum. Additional accelerated burn in test of three weeks continuously at +70°C. Additionally the satellite should be operated at ambient temperature for as long as can be accommodated within the confines of a rapid response mission.

b) Testing (at a Test house):

EMC testing,for spurious emissions in compliance with the specifications as requested by the launch service provider or payload provider.

- Magnetic testing, additionally to in house testing in order to validate magnetometer calibrations and to quantify magnetic anomalies.
- Vibration testing, Common test specifications with combined severity of all features catering to qualification levels to all the launch service providers to very late launch opportunities
- Thermal vacuum testing has been optimised to a 1 week period covering 3 complete cycles to further show up any early component failures and to determine thermal balance. A Surrey microsatellite is tested with an input temperature range of -30°C to +70°C. This gives a profile distribution across the satellite with the external exposed areas such as solar panels and external instrumentation reaching peaks of –20°C to +50°C. The well thermally isolated areas such as the battery sub system achieving much smaller excursions

XIII. CONCLUSIONS:

This paper focused by providing insights into COTS parts, their qualification, fault tolerant techniques for increased reliability. Further engineering philosophy, design regimes, various environmental test at subsystem and spacecraft level has been discussed. Systematic approach to Reviews, Quality Control and testing methods and documentation practiced for space systems results in excellence in Quality.

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Qualification of ultra-light plastic lens & body CMOS camera module for remote sensing space programs

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Abstract: In order to make use of the technology advantages, COTS Camera Module is being used in various space programme e.g. Rover and Lander of Chandrayaan-2, Event monitoring camera of Carto 2S, launch vehicle and cabin monitoring for Human Space programme. This 2 Megapixel single chip CMOS colour camera with 2.2µm pixel size device is selected due to its unique features of being extremelylightweight (~356mg), highly miniaturized package (8mm × 8mm × 5.55mm) and lowpowerconsumption Being COTS component and having no space heritage, the Camera Modulehas undergonean exhaustive Screening, Qualification, characterization exercise on samples under harsh space environments at SRG/SAC.

Under the Qualification plan, Hot and Cold storage, Temperature cycling, Biased Humidity, Operational Thermo-vacuum, Radiation (SEL/TID), Material analysis, Mechanical (Sine/Random/Shock), Outgassing and Life tests were successfully carried out. In addition, endurance to -197˚C, was carried out to simulate storage conditions during Lunar night. As the body and lens are made from plastic compound material, its susceptibility to Ultraviolet (UV) radiation was also carried out and results were found to be satisfactory.Due to its typical packaging and plastic body, Camera mounting process was also successfully done. Qualification test plan as per the expected environmental conditions in the space was successfully carried out and the Camera module was used for the first time in the Event Monitoring Camera (EVM) for Cartosat-2Swhich is already flownand excellent images have been received.

This paper describes the performance of the COTS camera module during tests performed under various environmental conditions during screening and qualification along with electrical & optical performance of these devices over the entire environmental tests

I. INTRODUCTION:

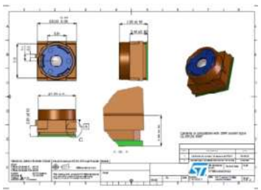
This 2 Megapixel colour camera module is a single chip CMOS imaging device with 2.2µm pixel size. It is manufactured using 0.18 µm CMOS Imaging process. This is extremely light weight ofonly 356mg & highly miniaturized package dimensions 8×8×5.55mm^3 with low power consumption. Due to its unique features it is planned to use in current and future Chandrayaan-2 Rover, Lander and Orbiter, Event monitoring in Carto series, Launch vehicle monitoring and cabin monitoring for Human space program of Indian Space Research Organization.This COTS camera module has no space heritage, therefore in house spacequalification test plan was generated and tests were performed accordingly on sample camera module.

This paper describes performance of the COTS camera moduleduring screening and qualification test performed under various environmental conditions.Exhaustive activities were carried out for evaluating the suitability of this camera module to survive the harsh space environments. This includes Hot and Cold storage, Temperature cycling, Biased Humidity, Operational Thermo-vacuum, Radiation (SEL/TID), Mechanical (Sine/Random/Shock), Outgassingand Life tests were successfully carried out. In addition, endurance to -197˚C, was carried out to simulate storage conditions during Lunar night. As the body and lens are made from plastic compound material, material analysis, glass transition temperature and its susceptibility to Ultraviolet (UV) radiation was also carried out and results were found to be satisfactory.

Integrity of these devices was evaluated by performing Visual Inspection & Electro-Optical Tests. Following sections describe the test plan for evaluation along with electrical & optical performance of these devices over the entire environmental tests.

II. DEVICE DETAILS:

The device has 1600x1200 pixels array to providecolor images instandarddigital formats and JPEGcompressed form (Reference-h).



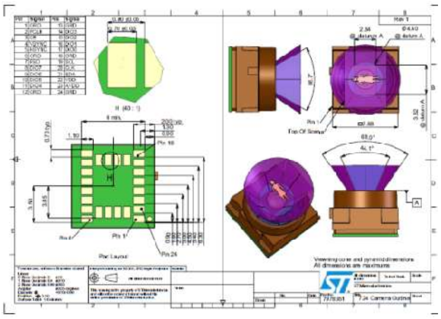


Figure-1: Camera Mechanical Drawing

It integrates a quad element plastic lenses, high-sensitivity pixel array, digital image processor and camera control functions. Camera mechanical drawing is given in figure-1 mechanical drawing is given in figure-1.

It has 9 resolution modes up to 1600 X 1200 pixels, number of pixels for each resolution mode is given in Table-1.

Resolution	No of pixels	Resolution	No of pixels
UXGA	1600X1200	CIF	352X288
SXGA	1280X1024	QVGA	320X240
SVGA	800X600	QCIF	176X144
VGA	640X480	QQVGA	160X120
		QQCIF	88X7

Table-1: No of pixels for different resolutions.

Four data output modes along with JPEG compressed and uncompressed outputs. The FOV is around 50°. The video data is output over an 8-bit parallel bus in JPEG (4:2:2 or 4:2:0), RGB, YCbCr or Bayer formats and the device is controlled via an I²C interface. The device is capable of streaming UXGA (1600 X 1200 pixels) data up to 30 fps in compressed mode and up to 15 fps in uncompressed mode.
It supports 1.8V or 2.8V digital interface and requires a 2.4 to 3.0V analog power supply. Typically, the device can operate as a 2.8V single supply camera or as a 1.8V interface /2.8V supply camera. The integrated PLL allows for low frequency system clock, and flexibility for successful EMC integration. An input clock is required in the range 6.5 MHz to 27 MHz.

The device also includes a wide range of image enhancement functions, designed to ensure high image quality, these include:

- Automatic exposure control
- Automatic white balance
- Lens shading compensation
- Defect correction algorithms
- Interpolation (Bayer to RGB conversion)
- Color space conversion
- Sharpening
- Gamma correction
- Flicker cancellation
- Noise reduction algorithm
- Intelligent image scaling
- Special effects

Figure-2 shows the internal block diagram of camera module. The device can operate it's sensor array in two modes controlled by register SensorMode within Mode setup.

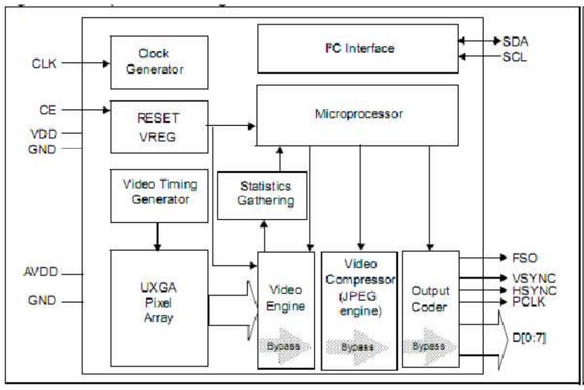


Fig:2 Block diagram of the camera

1) SensorMode_UXGA - the full array can be read out at 30 fps and the device canachieve:
– 30 fps JPEGs up to UXGA
– 30 fps YCbCr or RGB up to SVGA
– 15 fps YCbCr or RGB over SVGA
2) SensorMode_SVGA_analogue binning - this is a reduced power mode which uses the full array and a technique of analogue binning output SVGA at up to 30 fps.

III. SCREENING & QUALIFICATION PLAN:

Qualification plan was executed on 21 randomly selected devices. Prior to radiation and life tests, devices were subjected to 168 hrs burn-in tests.In addition, endurance to -197˚C, was carried out to simulate storage conditions during Lunar night. As the body and lens are made from plastic compound material, its susceptibility to Ultraviolet (UV) radiation test was also carried out.

Camera mounting process and lunar night survivability tests for camera assembly were also carried out successfully.

Overall screening and qualification plan and environmental tests performed in each group are given in below Figure-4&5 respectively.During each environmental tests, integrity of devices was evaluated by performing Visual Inspection& Electro-Optical tests.

Test setups used for Characterization and burn-in were validated for consistency and repeatability before start of

the Screening and Qualification activities.Typical set-up is given in Figure-3.

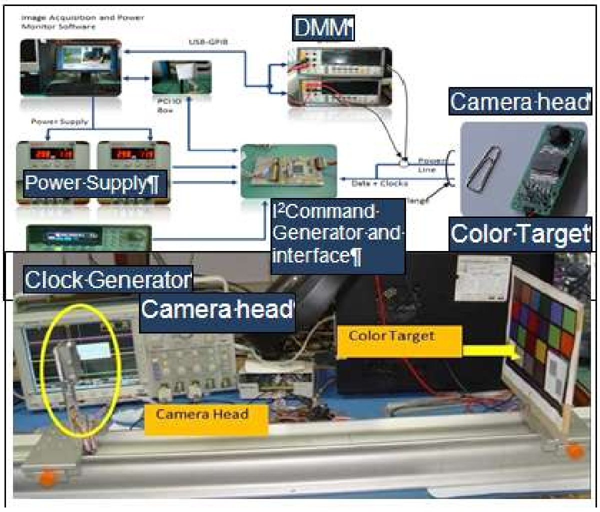


Fig:3 Typical test set-up

Screening of Camera Module VS6724 (100%)
- Initial E-O Measurements
- Stabilization Bake (75°C, 24 hours)
- Temperature Cycling (-55°C to +60°C), 20 Cycles (10 min. each) transition rate 1 °C/min
- Burn-in (55°C, 168 hours)
- E-O Measurements
- External Visual inspection (10X) at every stage

Figure4 Screening test plan

Overall Qualification Plan

G-I G-II G-III G-IV G-V P-I

G-I Group-I: Thermal test: Two devices
- Initial Electro-Optical Measurements
- Storage test (-55°C, +75 °C ,168 hours), one module was extra subjected to -197°C/240hrs.
- Temperature Cycling (-55°C to +75°C), 50+50 Cycles (10 min. each), transition rate 1 °C/min
- Th-vac operational Cycling (-25°C to +55°C), 5(1hr)+1(6hrs) Cycles,transition rate 1 °C/min
- Humidity Test (40°C/95%RH, 96/168 hours,Biased)
- Electro-Optical Measurements
- External Visual inspection (10X) at every stage

G-II Group-II: Life test: 8 devices
- 2000 hrs (@55°C – 4 devices & @60 °C-4 devices) Measurements at every 500hrs.

G-III Group-III: Radiation test -7 devices TID/SEL/UV
- TID 10Krad - 3 devices /SEL -2 devices
- UV-1 device+one lens assembly

G-IV Group-IV: Mechanical Test-1 device
- Sine Vibration – 25g /
- Random Vibration-18.1 Grms
- Mechanical Shock -700g ,0.5ms,5 blow

G-V Group-V: 3 Devices
Outgassing /Micro-sectioning/Material testing
- Outgassing - +125°C/24hrs/pressure 10E-5 torr

P-I Process Qualification 3 devices → Cold Temperature (-197°C) component survivability test One camera assembly → Camera mounting Process qualification and survivability during lunar night

Figure-5 Qualification plan flowchart

IV. PERFORMANCE DURING QUALIFICATION AND SCREENING TESTS:

Screening: Screening test was performed as per plan given in Figure-4. Power and its image quality was compared with the standard images using MTF. Drift in power and MTF was observed to be±5mA and 3% respectively.

Qualification: Tests performed in variousgroups are given in figure-5. Performance summary is given below.

Thermal Group:As camera moduleismade of plastic body & has plastics lens, various thermal tests e.g. hot and cold storage, thermal cycling, Humidity operational test,thermovac operational tests and in additionendurance test to -197˚C/244hrs, was carried out to simulate storage conditions during Lunar night (Reference-j).

Cryo temperature storage test.

Typical set-up and lens observation is given in below figure-6.

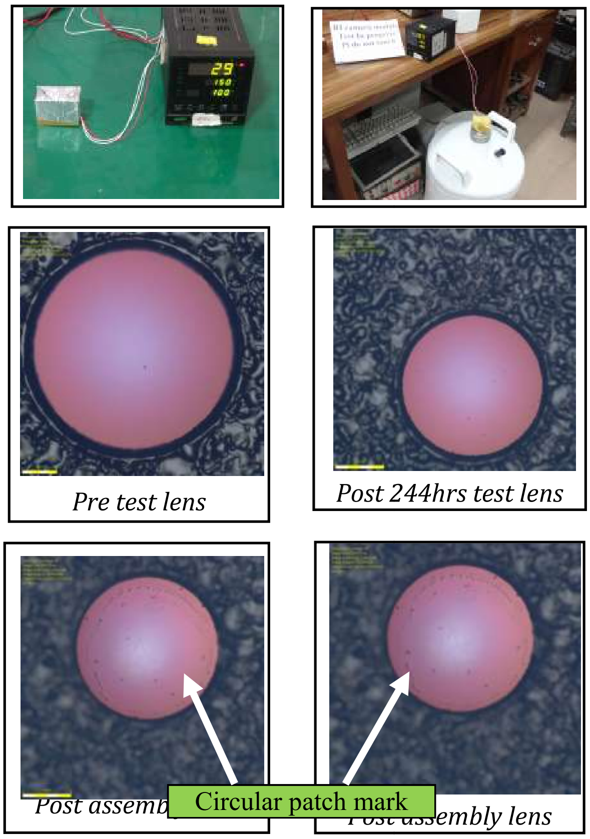


Figure-6Cryo test setup & lens observation.

No degradation was observed during post storage visual inspection. However, after camera mounting on the assembly some permanent impression circular patch was observed on the lens. After cleaning also, it remained as it is. After various tests viz. hot storage, thermal cycling, thermo-vacuum operational test and humidity it remained as it is and no further degradation was noticed. This impression on the lens did not affect the image quality of the camera module.

Humidity test:

Humidity operational test was carried out on two devices(Reference-i). Power consumption of both devices remained consistent.Pre to post visual inspection shows no degradation. Pre & post computed MTF at 113.6 lp/mm MTF at N/2 (56.8lp/mm) were found to be within 3%.

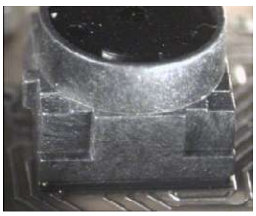
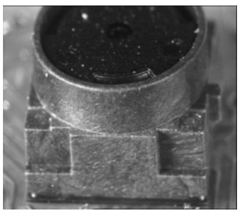
Pre Humidity Test	Post Humidity Test
	

Fig-7 Pre & post humidity camera plastic body

Thermovac test:Two devices were subjected under thermovaccum testing. Slant target was used for MTF computation. Computed absolute MTF values of both assemblies are observed to be different due external parameters like background, illumination condition, nature of target and selection of region of interest etc. However relative change in the MTF from 5°C to 30°C was only 4%, which is acceptable for both devices.Spectral Response of Band Pass Filter of camera module was measured after thermos-vacuum test and given in Fig-8.

Change in current values at 55˚C & -25˚C are roughly ±5mA from the nominal values and are well within the maximum limit135mA.

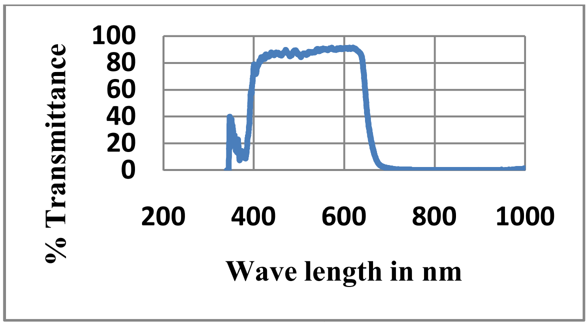


Fig-8: Spectral Response of Band Pass Filter of camera module

Life Test Group:

Eight device assemblies, were subjected to life testfor 2000Hrs (Reference-a). Four @55°C & remaining four @60°C. Imaging was carried out & recorded Every 500 hrs, in laboratory ambient conditions. Power consumption during life test was monitored and recorded. Average Current drawn by assemblies were 70mA with variation within ±5mA.

Radiation Group Test:

Total Ionization Dose(TID): Three RI camera modules were subjected to 10 KradTID-Gamma doseusing the SCLChandigarh radiation facility (Reference-a).Device current was monitored during exposure typical observation is given in fig-9. Pre and post transmission measurements of one lens (Fig-10) matches within measurements accuracy. Post exposure

images taken by camera modules were acceptable. One assembly was exposed up to 300Krad in steps. Imaging after exposure was also found to be satisfactory.

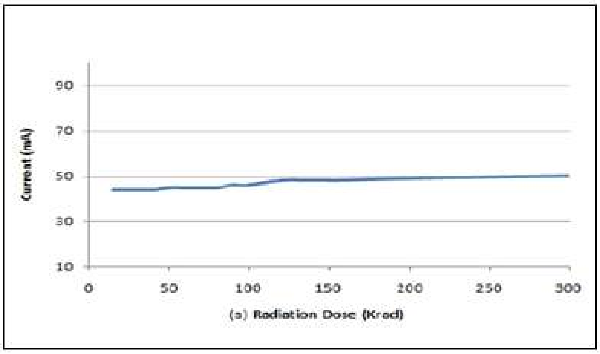


Fig.:9 Typical current variations w.r.t. total dose.

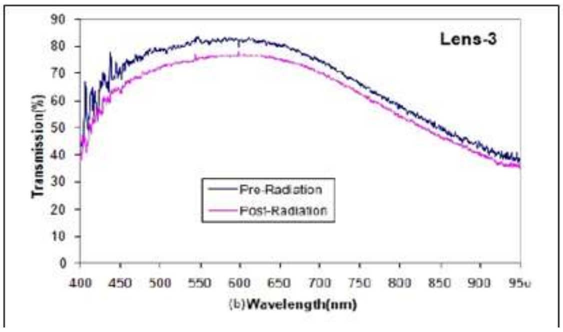


Fig.:10 Camera lens transmission test data for pre and post TID.

Single Event Latch(SEL) Test : Heavy ion test on the camera module is performed to evaluate its functionalityw.r.to. single event latch-up (SEL) and single event upsets(SEU) using the 15 MV Tandem Pelletron Accelerator (Reference-c). In this test the Silver (Ag) ions with energy of around 140MeV wereradiated with an LET of around 50 MeV-cm2/mg on the camera's CMOS sensor areawhich was exposed after lens assembly was removed. Two samples of the camera modules were subjected to this testand no failure was observed.

Ultra Violet (UV) Radiation Test: Camera module is packaged in plastic compound material and also having a plastic quadlens assembly. To assess the performance of plastic lens due to UV radiation in vacuum, a separate test was carried out (Reference-d). Custom made test setup was developed as shown in the figure-11. UV dose was measured and monitored by using spectrometer given in Table-2. From thermal group one assembly & demounted lens were used for 120hrs UV irradiation test. During the test, temperature rise due to visible and IR radiation wasmonitored and it has not crossed 70ºC.Camera lens and body were sufficiently exposed to UVA, while in case of UVB & UVC accelerated dose was applied. Post UV exposure visual inspection was carried out and was satisfactory, with few line traces seen on the lens (Ref Fig- 12), which did not affect the image quality of the camera as shown in figure.

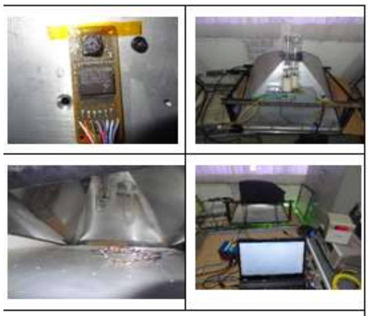


Fig.11 Custom made UV exposure set up

Expected exposure as per ASTM E-490			Achieved exposure during testing for 120 hrs	
UV type	Spectral range (in nm)	Radiation (in mW/cm2)	Peak exposure intensity during testing. (in mW/cm2)	Peak wavelength (in nm)
UVA	315-400	11	8.59 9.28	313 365
UVB	280-315	2.4	8.19	297
UVC	200-280	0.07	10.24	254
EUV & VUV	Up to 200	0.01	VUV test to be performed in vacuum. Impact of this will be separately addressed.	

Table: 2 UV radiation exposure details

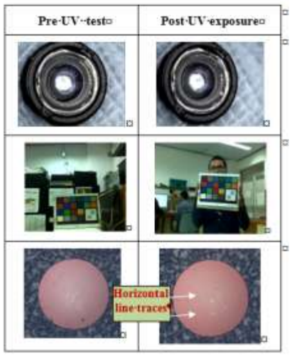


Fig.-12 Pre and Post UV exposure lens and camera image

Mechanical Group Test:

Sine, random vibration and shock tests were performed sequentially on a radiation tested assembly as per the level given in Fig-5.

No degradation was observed. As active vibration test, Images were captured during low level 0.5g sine test and found to be satisfactory. After complete vibration test,

post electrical measurements of Power & Image performance were also found to be satisfactory.

V. OUTGASSING, CONSTRUCTIONAL & MATERIAL ANALYSIS:

Outgassing test:

There are four plastic lenses & RGB Bayer color filter array in Camera module. The housing of these optics is also made of plastic. Presence of any other material like glue or adhesive is not known. Outgassing from these material at higher temperature and in vacuum environment may cause transmission loss of the optics. Therefore outgassing test was carried out as per ASTM E595. Test condition: 125ºC/24hrs at pressure 1×10-5torr. Results were satisfactory. Specifications:

TML≤ 1%, Measured value: TML= 0.17% CVCM≤0.1%, Measured value: CVCM=0.001%

Micro-sectioning:

One non-functional device was subjected to micro-sectioning to assess its assembly.Images of the same are given below. It gave a view of the total die-surface. It also gave confidence that removal of housing to expose the semiconductor to SEL testing will not be mandatory, as by line-of-sight at least 80% die surface is available to an incident beam of ions during the SEL test.

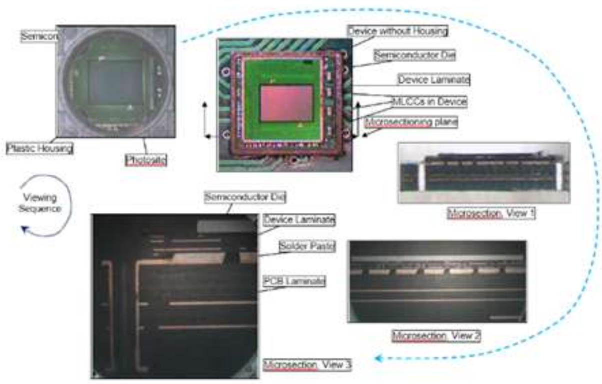


Fig.-13 Micro-sectioning to assess exposure to semiconductor for SEL test.

4.2.5.3 Material Analysis: Camera module was subjected for material analysis. By DSC & FTIR Analysis (Reference-k) camera module compound materials were identified as given below. Lens material is High Impact Polystyrene (HIPS) whose glass transition temperature T_g=118.1°C. while other two compound materialshaveT_g is >200°C.

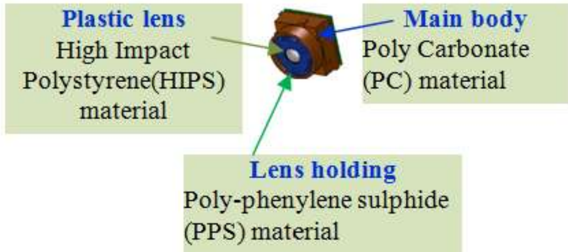


Fig.-14 Device material details

VI. CONCLUSION:

Devices have successfully gone through all tests during qualification. Qualification of process for mounting the Camera module on to PCBs; modules were assembled and have successfully passed all qualification tests.In addition, camera assembly successfully underwent Cryo endurance testing, to simulate storage in lunar night conditions.Based on their state of the art features and good performance duringqualification exercise, devices are used in ongoing mission of ISRO and also planned for future missions.

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Indigenous Development of MMIC Based Phase Shifter

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***Abstract*—Advanced technologies in Space systems are always a prerequisite to a successful space industry. In Indian Remote Sensing satellite program, there has always been a demand of higher data transfer rate in the available bandwidth. Sophisticated remote sensing and imaging techniques generate ever increasing scientific and payload data for ground transmission. Reliable transfer of enormous amount of data in the visibility period, requires high speed communication system. The Advanced packaging techniques for electronic components and miniaturization using indigenous technology, backed by industry support will be a step towards implementation of higher data rate systems for satellite applications. The paper describes the realization of Microwave Monolithic Integrated Circuit (MMIC) based phase shifter at X-Band for 8 PSK modulator. The phase shifter circuit uses low barrier Schottky diodes, realized at Gallium Arsenide Enabling Technology (GAETEC), Hyderabad. The implementation is based on a modified configuration, further optimized for better performance. A comparative study of topologies and switching element has been undertaken to justify the adopted configuration. The paper highlights MMIC design process, simulation stages, and, GAETEC foundry capabilities. The development aims at making the MMIC available off-the-self for future satellite applications.**

I. INTRODUCTION

There are various techniques to implement constant or variable phase shifter. Loaded line, reflection type, high pass-low pass type and switched line topologies are some of those configurations. The frequency of operation along with targeted application plays a vital role in deciding the phase shifter design. At higher frequencies (C, X, Ku), discrete components cannot be used to implement the design due to their series resonant frequencies. A hybrid approach by combining loaded line and switched line topologies to obtain 45^0 phase shift at X-Band has been implemented. Since the application is high data rate payload data transmission, very high speed switching is required. MIC implementation at X-Band suffers from undesired capacitance and delays which affects high speed circuit integrity. To overcome packaging uncertainties, Microwave Monolithic Integrated Circuit (MMIC) based phase shifter has been developed.

The phase shifter is capable of high speed switching at data rates up to 1Gbps. The switching element, Schottky diode, fabricated at GAETEC, is a custom designed device for X-Band data transmission applications. The design simulation for phase shifter has been carried out in Advanced Design System (ADS) using GAETEC foundry libraries. Wafer based diode

rahulk	Parameter	Specifications
1.	Frequency Range	8-8.4 GHz
2.	Phase Imbalance	5
3.	Amplitude Imbalance	1 dB
4.	Insertion Loss	Less than 5 dB
5.	Switching Frequency	200 MHz
6.	Return Loss	Better than -15dB

TABLE-I
TARGET SPECIFICATIONS FOR 45^0 PHASE SHIFTER

model has been obtained from GAETEC foundry and integrated to generate MMIC layout in ADS. The diode has been integrated with MIC circuit design fabricated in-house at ISRO Satellite Centre and tested for S-parameters at GAETEC.

II. SYSTEM CONFIGURATION AND SPECIFICATIONS

As the phase shifter application is in high data rate transmission, its specifications were derived from the performance matrix of 8-PSK modulator. Phase shifter is a standalone unit of 8 PSK modulator, where the phase shift is controlled by C bit of data. The phase shifter module is followed by QPSK [1] modulator, also planned to be in MMIC form, that accepts I and Q bits. The modulated signal in each path is combined to give 8-PSK output. Figure 1. Shows the configuration for phase shifter and figure 3 illustrates the application of phase shifter in 8-PSK modulator. The phase shifter configuration arrived at, also takes into consideration the available components at the Centre and available technology in the national industry. The specifications derived are given in Table I

II. PHASE SHIFTER DESIGN

There are four topologies studied for X-Band application of phase shifter. A brief comparison is outlined below:

Topology Selection

1. The switched line design uses two switches to route the signal through one of two paths. The difference in electrical length between the two paths provides the necessary phase shift.

2. The reflection type phase shifter is very similar in performance to switched line design. The additional length is introduced by the round trip to short circuit and back, compared to the shorter trip to the switch and back, thus providing the required differential phase shift. However, more dissipation/losses are expected in reflection type phase shifters
3. The loaded line designs rely on the phase shift introduced by one or more susceptive elements placed in shunt across the transmission line. This method has a disadvantage that it cannot be impedance matched easily. However, it can be circumvented by placing two susceptive shunt elements along the transmission line at a particular distance from each other but to some extent performance is compromised.

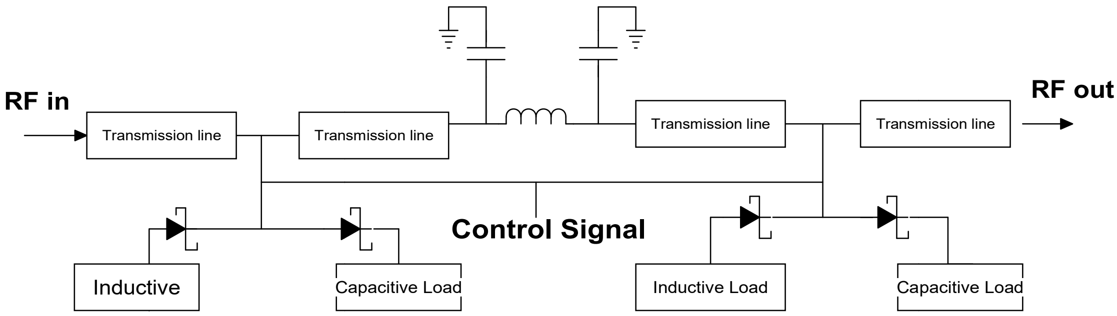

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Fig. 1. 450 Phase shifter schematic

4. Another phase shifter topology is where two switches route the RF signal through a high pass filter section in one phase state and through a low pass filter in the other phase state. The high pass filter introduces phase advance to the signal and the low pass filter provides phase delay and the switching between these two states. However, the high pass-low pass combination requires discrete values for realization and hence, is suitable only for lower frequency ranges.

Based on the comparative study, a modified configuration of switched line phas e shifter and loaded line phase shifter has been derived. A Switched line phase shifter which is simplest to design and to match impedance using schottky diodes, is made to switch between inductive and capacitive loads. The implemented schematic is shown in figure 1. In the switched line design, two switches are used to route the signal through one of two paths. The difference in electrical length between the two paths provides the necessary phase shift. If the two physical line lengths are l_1 and l_2, the phase shift is given by:

$$\Delta\varphi = \beta \times (l_1 - l_2)$$

Where, $\Delta\varphi$ = Phase shift required
β= Propagation constant of the transmission lines

The electrical length difference ensuring 45^0 phase shift is a 50Ω line @ X Band. The signal switches between the two pre- determined lengths (reference arm and delay arm) calculated with the information of wavelength and desired phase shift value.

$$\Delta\varphi = (2\pi/\lambda) \text{ x } \Delta L$$

ΔL= Reference and delay arm length difference
λ=Guide Wavelength

As shown in Figure 1, the control signal bit switches to either inductive or capacitive load depending on control bit value and presents the load to the RF signal for the desired phase shift. Depending on the load selected, the signal phase is shifted thus giving a differential 45^0 phase. The two symmetric arms, separated by a $\lambda/4$ equivalent of inductor and capacitor, improve the system return loss.

Switching element selection

The primary function of a switch here is to load the RF signal (inductively/capacitively) for a differential phase. Hence, the switching element selection becomes the stepping stone for the development. The commonly used switches are pin diodes, schottky diodes and MESFETS. These have been compared below and appropriate selection has been made for the design.

1. In pin diodes, the depletion region is separated by a greater distance than the normal p-n junction hence reducing the capacitance. At microwave frequencies the capacitance of the junction needs to be rather low. The delay time for this type of diode is high limiting the switching frequency to less than 50MHz. Hence Pin diode is not desirable for the purpose here to switch at 200Mbps.
2. Schottky barrier diode is formed by the junction between a metal and a semiconductor. The size and shape of the contact can also be controlled. The schottky diodes can be driven by the complementary outputs (0.4V) with current requirement of about 10mA per diode whereas in PIN diodes to reduce the turnoff delay, a large

reverse voltage is required across the diode that needs a much more complex driver to maintain high speeds. Current flow in the schottky barrier diode involves the movement of electrons in both the n-type material and the metal. These carriers are majority type in both materials, which redistribute very rapidly in response to changes in current. Hence the switching speed of schottky diode is very high compared to pin diodes.

3. MESFETS are transistors made from three contacts on a semiconductor. The gate forms the schottky barrier while the source and drain contacts are ohmic. The junction between regions of different doping is abrupt in MESFET making the carrier transit time small. MESFETS are typically made on gallium arsenide where the carrier mobility is high; thereby further reducing the carrier transit time. This helps in attaining high switching speed in MESFETS. But the voltage swing required in this transistor to switch is difficult to obtain from data without any signal distortion.

Considering the drawback and advantages of these semiconductor devices, low barrier schottky diodes are selected for switching in the 45^0 phase shifter.

III. MMIC IMPLEMENTATION

With prior experience of GAETEC, Hyderabad to deliver space qualified products and with recent up-gradation of MMIC fabrication processes, the foundry is an ideal place for realization of MMICs. The 0.7µm MMIC process of GAETEC is a space qualified fabrication process. The foundry provides ADS library support to carry out design simulations which are translated to fabrication after modifying as per GAETEC design rules [4].

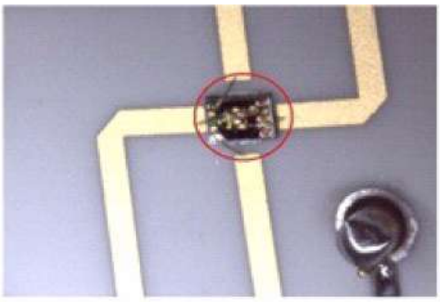

Fig. 2. Schottky Quad fabricated at GAETEC and assembled on in-house alumina substrate

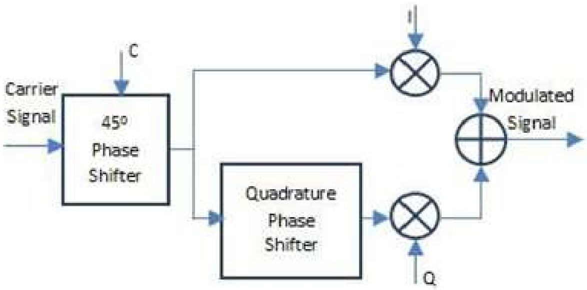

Fig. 3. Proposed 8 PSK scheme

Phase shifter MMIC layout and schematic simulations were carried out in ADS using GAETEC foundry libraries. These libraries include the models of capacitors, inductors, transmission lines, transistor and schottky diode, approximating the on-wafer performance of the devices.

According to Figure 1, the control signal C, switches the diodes for one of the appropriate paths. The differential phase of the two paths is fixed at 45^0. The design values for capacitors and inductors have been calculated based on discrete component. Figure 4 shows the 45^0 MMIC layout realized in ADS. As, there is no 50Ω impedance match in MMICs, inductive and capacitive effects of transmission lines have been incorporated in the selected values of passive components using iterative simulation techniques. λ/4 line properties were obtained using the equivalent inductor- capacitor combination.

MMIC schematic and layout generation process is rigorous and highly iterative. Various MMIC design simulation and layout phases observed during usage of GAETEC foundry libraries are listed below.

a) Schematic generation based on topology and design values.
b) Schematic simulation to obtain desired performance. (tuning and optimization)
c) Layout generation as per the schematic components. (At times schematic values used cannot be synthesized in layout due to foundry fabrication constraints. So nearby values are taken)
d) Momentum simulation for the layout.
e) Momentum result analysis to take note of value deviation
f) Optimizing schematic values based on layout components. Trying for best performance by revisiting schematic and layout till the most optimum fit is obtained
g) Importing momentum (layout) results for co- simulation (layout with active and passive component models)
h) Result analysis. If deviation observed revisiting schematic followed by momentum and co-simulation.

The design steps for MMIC layout are shown in the flowchart Figure 5

MMIC implementation comes with an inherent advantage: Discreet components such as inductors and capacitors are grown on wafer directly. Component selection is a vital design step for phase tuning and better performance. Discrete components of leaded/surface mount type cannot be used directly on PCB due to series resonant frequency of inductors and diodes at X-Band.

However, MMIC realization has certain challenges of its own. *Firstly*, the layout generation is a step-by-step and

iterative process. Each layout modification follows a schematic analysis before the change is incorporated into the design. RF Momentum analysis of the layout is imported for a co- simulation to include the active device behavior. Any deviation during co-simulation calls for a fresh analysis from the initial stage. *Secondly*, each fabrication/foundry has its own set of rules [4] and guidelines [4] which limit the finer values required of passive devices. Device orientation with respect to foundry axis is another consideration/limitation to design freedom *Thirdly,* wafer level characterization is another challenge as appropriate MMIC probing stations need to be installed to analyze the performance of intended device. In the present scenario, a test probe from Cascade Microtech has been procured for probing activities, which will be carried out at GAETEC probing station. *Lastly,* though MMIC realization overhauls MIC implementation with respect to repeatability and superior performance, it comes at a hefty cost. Hence, a limited number of iterations are permitted after a proper and optimized design analysis in simulation has been carried out.

The enlisted guidelines for MMIC development are observations during the developmental stage. These may vary with respect to foundry, DRC guidelines and vendor directives. However, a general structure of MMIC phases has been presented to take up design process at GAETEC

IV. RESULTS

The MMIC based 45^0 phase shifter will be used in 8PSK [3][5] modulator. The stringent requirement of 10^{-8} bit error performance at 8 GHz RF carrier and 160 × 3 Mbps data stream, requires high speed switching and low parasitic capacitance in the transmission path, a requirement which is met with MMIC implementation. .Figure 7 shows the 45^0 phase shifter simulated output in ADS. Table II shows the comparison of simulated and measured results for 45^0 phase shifter.

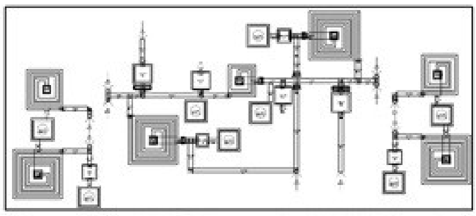

Fig. 4. MMIC layout generated in ADS using GAETEC libraries

TABLEI
Comparison Of Simulated And Observed Data For 45^0 Phase Shifter

Parameter	Simulated	Measured Result
Insertion Loss(dB)	1	2.
Input Return Loss(dB)	1	12.
Output Return Loss(dB)	1	13.1
Phase Shift(degrees)	4	45.

Schottky diode fabricated at GAETEC, Hyderabad has shown satisfactory results. Figure 6 shows the waveform obtained during on-wafer diode characterization.

Figure 2 shows the quad assembly on indigenous MIC. The assembly was tested as BPSK modulator to verify the diode switching function. Phase imbalance of 20 and amplitude imbalance of 2 dB was obtained for the BPSK assembly. The diode works at a bias voltage of 1 V with a current of 10 mA in nominal operating condition.

CONCLUSION AND FUTURE WORK

The package details for MMIC have been worked out in consultation with GAETEC, Hyderabad. A suitable housing for the MMIC has been identified and layout has been optimized as per the package dimensions. Radiation effects and temperature limits of both operation and storage have been found satisfactory as per the QA guidelines.

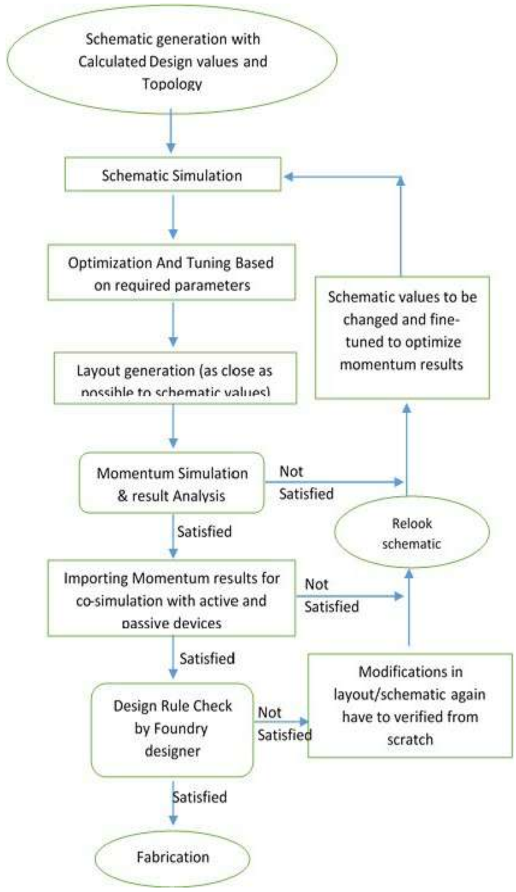

Fig. 5. MMIC Design Flow at GAETEC

Request for quotation is under preparation, scrutinizing the requirements, deliverables, number of iterations to be supported, delivery schedules and budget.MMIC realization will be, indeed, a major development in the high frequency application for satellites. It will be a boost to fast track space missions and an opportunity for industry to participate in the development of Indian space infrastructure.

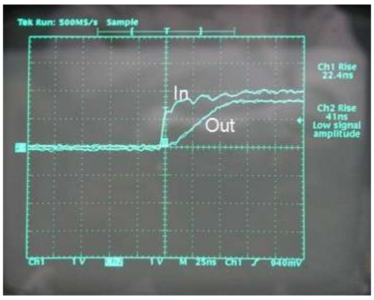

Fig. 6. On wafer waveform for Schottky diode Characterization

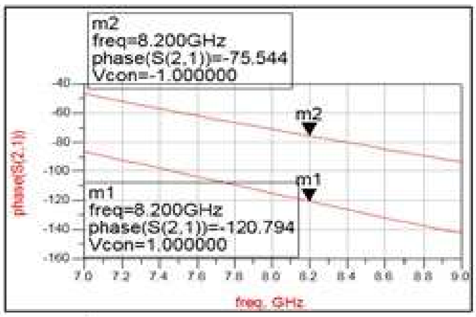

FIG. 7. ADS SIMULATED OUTPUT FOR 450 PHASE SHIFTER

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The author would like to acknowledge Shri. Parimal Kumar and Lt. Shri. R.M.Mishra for their valuable advice and guidance to realize the system successfully.

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C

FABRICATION AND TESTING PROCESSES & METHODOLOGY

Ruggedized Design and Fabrication of Crystal Oscillators for Launch Vehicle Application

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Abstract — **High reliable clock oscillators are vital parts in most of the avionic packages for launch vehicle applications. Imported oscillators are in regular use. Avionic entity has taken up the indigenization of clock oscillators by making use of the expertise available in VSSC and manufacturing facilities available in Indian Industries. Selected frequencies were identified for qualifying the process and testing. Performance evaluation carried out on proto version/QM version was found to be meeting the specification requirements. However, FM model before inducting into the launch vehicle was subjected to field trial in packages configured in stack level. Performance deviation was observed during stack level vibration test. Design of the oscillator was re-looked. Fabrication process, assembly level steps etc were critically examined. Finally the problem was identified and it was understood that the process needs to be ruggedized. This paper addresses the issues faced, its analysis, solutions, validation, qualification and finally induction in Launch Vehicle Applications.**

I. INTRODUCTION

Clock oscillators ranging from 10 MHz to 500 MHz are in use in the critical avionics packages for launch vehicle applications. Imported SPXOs (Simple Square wave crystal oscillators)are used in packages which are to undergo various tests like screening and qualification. The indigenization cell of Avionics Entity of Vikram Sarabhai Space Centre, Thiruvananthapuram has taken up the SPXO indigenization activity through Indian industry. It has become necessary to supplement the design with adequate design margin and realization owing to performance deviation observed during field trials.

II. RUGGEDISATION REQUIREMENTS

SPXOs are generally fabricated using crystal with shaping circuitry. Springs are employed for mounting the crystal in the base material. The devices are fabricated using a standard process capable of withstanding the screening and qualification tests at the component and package levels.

During the qualification tests in stacked configuration, performance deviation has been noticed. This was analyzed in detail. The probable causes are due to insufficient mounting area of crystal leads to substrate and inadequate mounting method.

III. TEST RESULTS

An indigenously developed 12 MHz square wave crystal oscillator has been used in the fabrication of one package and the cards were mounted in a stacked mode and subjected to PSLV/GSLV qualification level of sine and random vibration along thrust axis. The functional performance was monitored using checkout port data. Clock frequency was monitored with bit rate clock using frequency counter having 1 Hz resolution and 12 MHz oscillator output was monitored continuously with digital storage oscilloscope.

The package level performance was normal during the pre-sine vibration, sine vibration and post sine vibration. Erroneous performance is noticed in random mode vibration. Following are the observations:

a. The output of crystal oscillator becomes notched during a particular range of frequency.
b. Erroneous checkout port data

The package showed normal performance in stack mode during pre and post random vibration.

IV. CRYSTAL MOUNTING TECHNIQUES

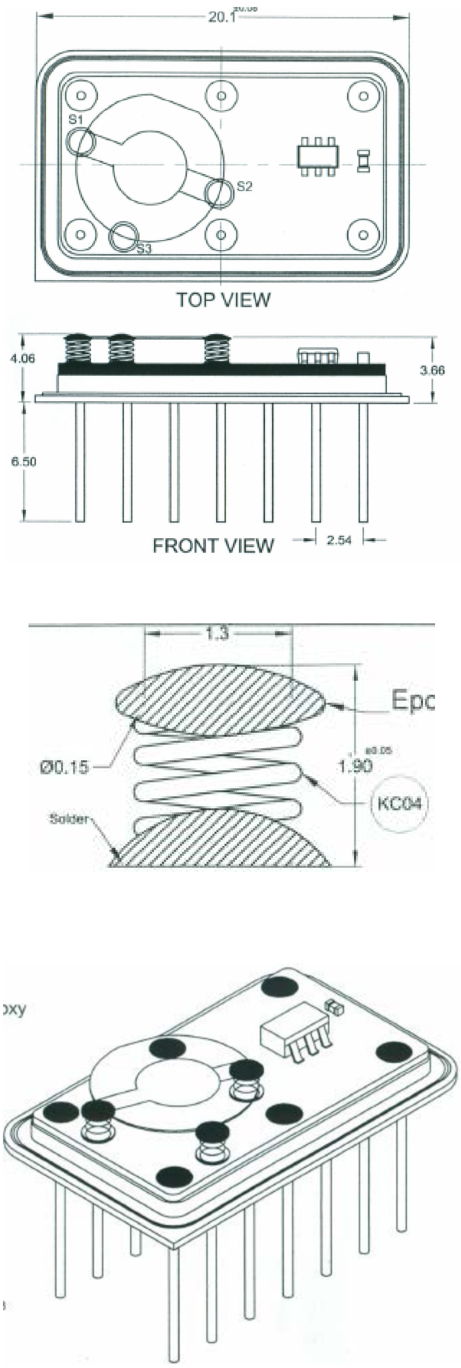
The crystal oscillator fabrication was relooked based on the performance deviations observed during the random vibration while it showed normal performance otherwise. Two types of mounting method were adopted for fabrication.

V. SPRING BASED CRYSTAL MOUNTING

The crystal was mounted on the base using springs at four corners and associated electronics were

assembled in the base. The whole assembly was bonded to the header using standard techniques. The Fig. 1 shows the mounting assembly.

The crystal oscillator with spring based mounting was subjected to component level vibration and withstood all the requirements. The oscillator showed notched output during random vibration in stack mode in a small range of frequency.



VI. DUMB-BELL MOUNTED CRYSTAL

Even though the crystal mounting with spring could withstand all the component level tests which is specified as $20g_{rms}$, its capability to withstand higher modes of vibration in packages configured in stack level was to be assessed. The mounting mechanism is modified with the dumb-bell technique and new devices were fabricated. The fig. 2 shows the dumb-bell based mounting mechanism.

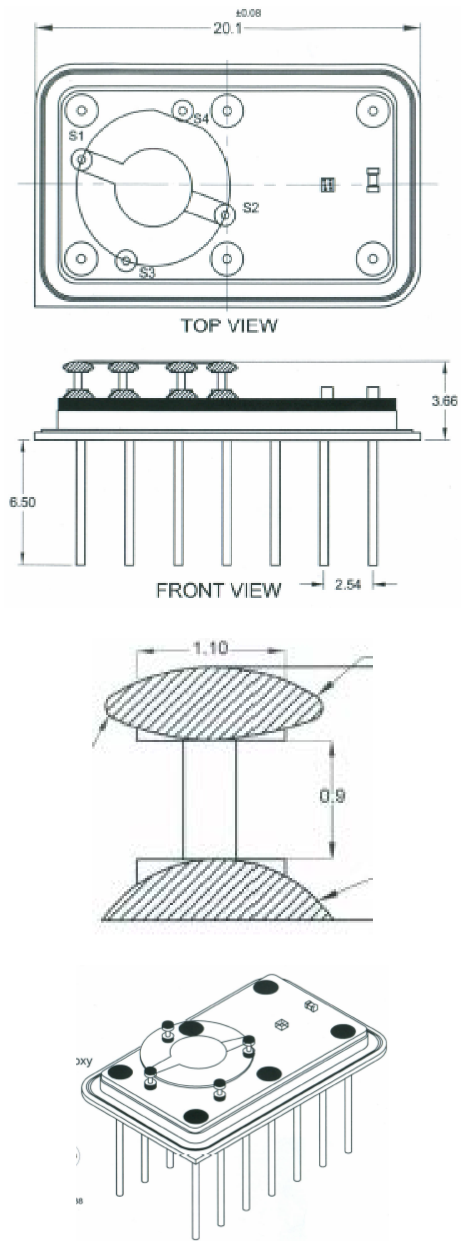


Fig. 2: Dumb-bel based crystal mounting

The dumb-bell mounted crystal oscillator was subjected to all the required PSLV/GSLV qualification level sine and random vibration test in stack mode. The oscillator showed satisfactory performance and found that the problem was solved. To gain confidence, more samples were subjected to all the qualification tests.

VII. RUGGEDISATION OF DESIGN AND FABRICATION OF CRYSTAL OSCILLATOR CIRCUIT.

Issue 1:

In the oscillator circuit, where the design has been carried out to make the oscillation stable, 3rd overtone tank circuit has been made use of. In the initial circuit set up using alumina substrate. Crystal leads have been soldered to the alumina substrate whose conductive track is made using silver palladium. Due to inadequate soldering and inadequate area of conductive pad over which crystal leads were soldered, the oscillators ceased at the frequency of interest. The negative resistance of the circuit was not satisfying the equation $Re < |-R|$, where R_e is the equivalent resistance of Crystal on parallel resonance.

Solution:

The pad area where Crystal is soldered in the substrate has been increased twice. Soldering has been improved by adding 2% silver alloy to the Pb-Sn solder (63%, 35%, 2%).

Issue 2:

Crystal is mounted inside the oscillator package using 4 mounting posts. The post is spring loaded to avoid unwanted oscillation due to high environmental vibration to which electronic packages are subjected to. In one situation, it was observed that higher modes of vibration of the order of 75 g_{rms} is encountered at the top of the module in stack configuration, when the electronic package with crystal oscillator is subjected to vibration in thrust axis at 13.5grms. In this situation, when the frequency of vibration is between 140 t o 300Hz, the oscillator ceases its operation and then restoring when frequency of vibration exceeded the above range. On analysis, it was found that spring is resonating at frequency between 140 to 300Hz in opposite phases of that of crystal and nullifying the oscillation (anti-resonance).

Solution:

After analysis, it was seen that a rigid support materials for Crystal whose natural resonance frequency as low as below 100Hz can solve the problem. Accordingly, support posts in the form of dumbbells are suggested for supporting the crystal using 3 mounting posts. Crystals with dumbbell based support posts assembled in samples was subjected to vibration in package level to ensure adequacy of oscillation in higher levels of vibration in all three axes. The results were found to be satisfactory.

VIII. ANALYSIS

The device showed the erroneous results only for the spring based fabricated crystal oscillators. This peculiar performance was evaluated in detail.

The resonance survey was conducted and observed peaking of vibration is noted for certain frequency range. The test was repeated by notching the frequency band. The problem still persists.

Further analysis revealed that the crystal oscillator vibration was nullified/modified by the external vibration coupled through the springs. For the lower level of vibration, the coupled level is not sufficient enough to neutralize the crystal vibration and hence the oscillator output is normal. Due to the amplification level associated with the stack, provision is to be provided to arrest the vibration level to the designed level or the mounting mechanism is to be changed. The second option is found to be the most suitable one, since it will be free from external coupling of the vibration to the crystal when the package is subjected for severe vibration levels.

IX. VIBRATION TEST RESULTS:

The performance of device at two different vibration levels is compared.

DUT:

Serial Number:

Project File Name:		ZZ Axis Random13.5grms DQT.prj
Profile Name	:	13.5 GRMS
Test Type	:	Random
Run Folder	:	.\RunDefault Feb 27, 2013 12-41-41

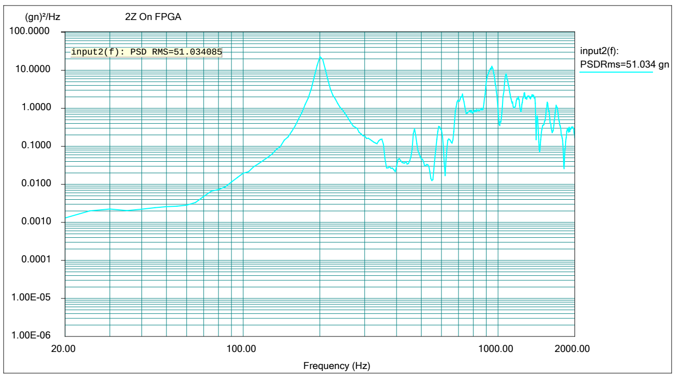


Fig. 3: ZZ Axis Random13.5 g_{rms}

DUT:
Serial Number: 4th Sample (Dumb-bell type)
Project File Name: ZZ Axis Random 13.5g_{rms}.prj
Profile Name: Random 13.5g_{rms}
Test Type : Random
Run Folder:.\Run Default Sep 29, 2014 15-04-59

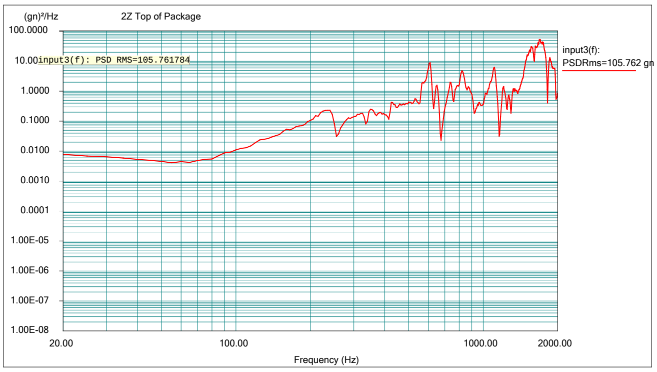


Fig. 4: ZZ Axis Random 13.5 g_{rms}

X. CONCLUSION

Careful design of the electrical circuit and ruggedness of mechanical assemblies for crystal mount through the mechanism discussed in the paper can ensure the oscillator performance in all environmental conditions expected for launch vehicle application.

This has been established through the mounting procedure described in the paper and validated the mechanism employed in the design of 12 MHz and 32 MHz crystal oscillators through stringent screening, qualification and package level testing.

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3GHz SAW BPF becomes a possibility with Qualification of 250nm Process Capability

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Space Applications Centre, Ahmedabad

***Abstract*— Surface Acoustic Wave (SAW) band pass filters consist of thin film inter-digitated metal transducers fabricated on the polished surface of a piezoelectric substrate. Till recently, the processing capability of such metal features, at Space Applications Centre (SAC), was limited to 1-micron feature size (electrode width and gap). This feature size restricts the frequency of operation of corresponding SAW filters to the sub-GHz range.**

Development of 250 nm process capability for SAW devices and its subsequent qualification represents a quantum technological advancement in terms of the realization of high frequency SAW devices. This paper presents the details of the said qualification activity together with the philosophy adopted for testing the process capabilities and recommendations for successful implementation in realization of flight hardware.

***Index Terms*—Surface Acoustic Wave BPF, Lift off process, 250 nm IDTs pattern**

I. Introduction

Surface Acoustic Wave (SAW) filters are realized by the fabrication of thin film inter-digitated metal transducers on the polished surface of a suitable piezoelectric substrate such as ST-X Quartz, Lithium Niobate and Lithium Tantalate. These are passive devices that offer precision filtering in the frequency range of 10 MHz to 3 GHz. As shown in Figure 1, the critical feature size of a SAW device, W, scales inversely with respect to frequency. For example, the feature size of a 2.5 GHz SAW filter, fabricated on 42deg Y-X Lithium Tantalate, scales down to 0.4 micron.

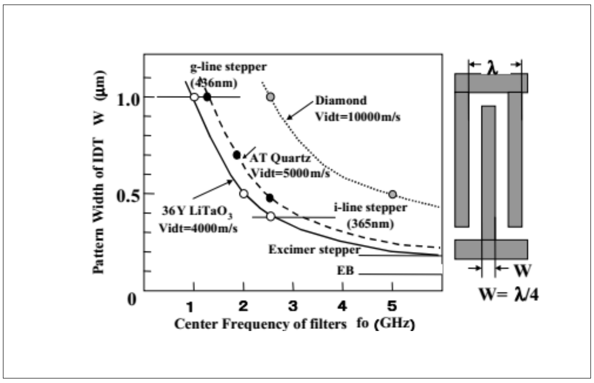


Fig. 1. Scaling of SAW feature size with respect to frequency

Defining IDT like metal lines having dimensions below 1um using wet chemical etching gives a very poor dimensional control and yield. The solution to this problem is offered by the additive patterning process–lift-off. Hence, to achieve the required dimensions, lift-off process was used. The coating, e-beam lithography and development parameters were optimized to achieve the required resist thickness as well as undercut profile on a single layer PMMA950K e-beam resist. The undercut profile helps in ensuring discontinuities at the pattern edges after metal deposition for the solvent to attack resist and facilitate proper lift-off. Subsequently, the e-beam evaporation of required thickness of NiCr–Al was carried out ensuring orthogonal deposition on the wafer so as to avoid step coverage of resist profiles. The developed lift-off process was successfully used for fabricating SAW BPFs on quartz wafer with good edge definition without any symptoms of tearing or peeling of metal at pattern edges

Fabrication process is depicted in figures-2.

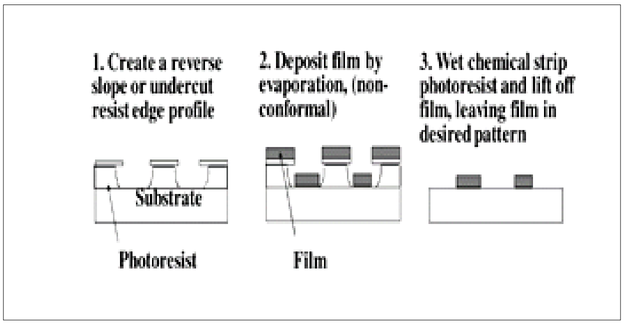
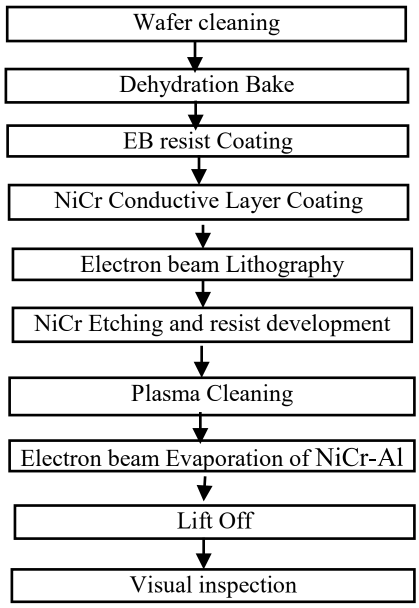


Fig. 2. The Process Simplified

The flow chart given below identifies the stages of Pattern Definition process



II. PROBLEM AREA IDENTIFICATION

a. Pattern definition of targeted dimensions
b. Patterning integrity (No Shorts/ Opens)
c. Pattern adhesion (Under Qual. Conditions)
d. Wire bonding compatibility

III. QUALIFICATION TESTING

Considering the requirement of all environmental stresses during mission life and to evaluate targeted design requirements, qualification test plan and qualification test sample were prepared. For test sample a combination of pattern was designed to assess realization of line width/gap, pattern integrity, pattern adhesion & that of repeatability and uniformity of the pattern over the substrate area;

To evaluate the resolution and uniformity in overall area of substrate IDT patterns were designed with different line width and spacing which consists of line widths from 0.25 microns to 3 microns;

To evaluate the pattern integrity like short in IDT fingers, probing point were designed to identify the shorts through electrical continuity testing because in SAW filter IDT consist number of fingers and only one short is sufficient for failure of the device;

To evaluate the pattern adhesion with substrate, since SAW pattern thickness & line widths being very small, subjective adhesion test with scotch tape or quantitative adhesion test with stud pull tester cannot be done on the SAW pattern. Hence in lieu of this 1 mil gold wire bond pull test were carried out on termination/appropriate conductor line widths at identified locations. Designed test sample shown in figure 3, below.

Initial visual inspection of all the samples for defects like cut, short, chipping, surface mark, scratches & metal lift off etc. & electrical tests for shorting in opposite IDT coming from opposite bus bar were carried out. Dimensional measurement for line width and gap also well within the tolerance (below ± 12%).

Qualification test samples were exposed to all applicable environmental stresses to assess the quality and reliability of samples, after each and every environmental test and visual inspection for all the defects and monitoring test were also recorded and no deviation was observed like pattern peeling /lifting, scratches, surface mark, crack, discoloration etc. *Hence, Problem Area 1 & 2 addressed successfully.*

For adhesion testing, adhesion test was conducted on initial samples (Group-1) as well as after environmental test (Group-2) and values are also recorded and it was observed that the adhesion strength/bonding strength of 1 mil wire bond meeting the MIL requirement of 3 gmf, it was also observed that all the wire break from bond heel area which shows that the perfect pattern adhesion with substrate. The graph in Figure-4 & Figure-5 for adhesion test shows that pattern adhesion with substrate and red line in the graphs shows the required adhesion strength.

The graph shows that the adhesion strength of pattern with NiCr-Al metallization and substrate are acceptable before environmental stresses and it was also observed that after environmental stresses no degradation was observed. *Hence, Problem Area 3 & 4 were also addressed successfully*.

Qualification test plan followed for the lift off process for 250nm pattern definition is given in below table –1

TABLE I. QUALIFICATION TEST PLAN

SAW Substrates	
Visual Inspection & Dimension Measurement	
Electrical Continuity	
Group -1	**Group -2**
Adhesion Test	High Temperature Storage Test
Post Adhesion Test Visual Inspection	Post High Temperature Storage Test Visual Inspection & Electrical Continuity
High Temperature Storage Test	Thermo- Vacuum Test
Post High Temperature Storage Test Visual Inspection & Electrical Continuity	Post Thermo- Vacuum Test visual Inspection
Temperature Cycling Test	Electrical Continuity Test
Post Temperature Cycling Test Visual Inspection & Electrical Continuity	Adhesion Test
Metallization Thickness measurement	Post Adhesion Test Visual Inspection

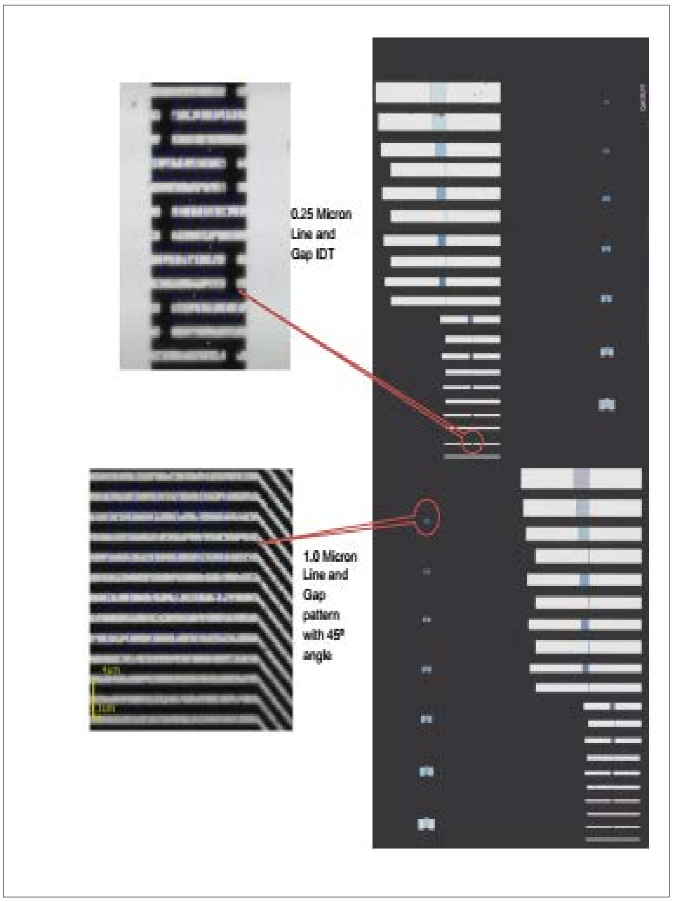


Fig. 3. Design of Test Sample

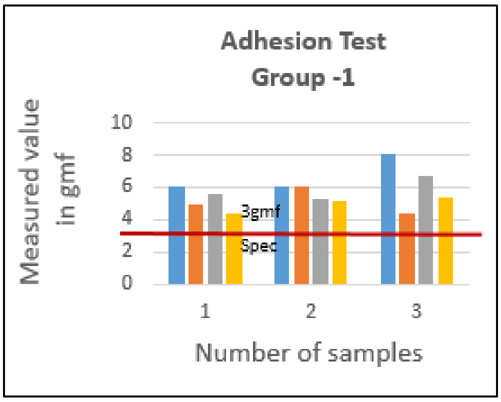


Fig. 4. Adhesion test

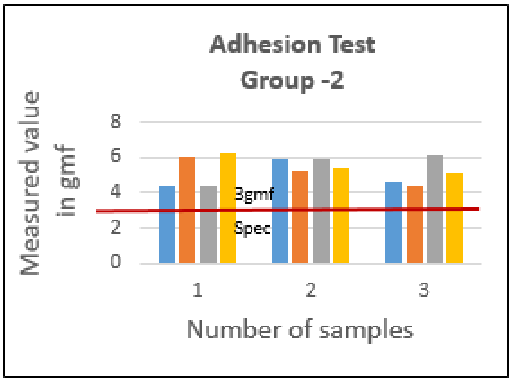


Fig. 5. Adhesion test

IV. CONCLUSION

Hence, realization of SAW devices for Critical Dimension (CD) -0.25 micron (IDTs pattern) with NiCr-Al metallization, using Lift off process on quartz SAW Substrate, was thus found meeting the Process Qualification requirements and the pathway is cleared for use of this process to develop SAW BPF devices of GHz range.

The main features of the qualified process and obtained result is mentioned in Table-II

TABLE II. MAIN FEATURES OF DEVELOPED PROCESS

Parameters	Specifications
Wafer Material	ST-X Quartz
Wafer Size / Thickness	3”, 4” diameter / 0.5mm – 2mm
Resist	Single layer PMMA950K
Pattern	Equal Line / Space (IDT) patterns, CD down to 0.25µm
Lithography	E-Beam Lithography
Critical Dimension (CD) Control	±12%
Evaporation	E-Beam Evaporation System
Metallization Thickness Control	±5%
metallization Thickness Uniformity	±2% across the wafer
Pattern Transfer	Lift-Off

V. FUTURE SCOPE

The lithography process is to be augmented to include LiNbO3 and LiTaO3 wafers and subsequently their qualifications are to be taken up. SAC is also working on a process to achieve sub-100nm critical dimensions for IDT like structures to be used for SAW as well as other applications using e-beam lithography and RIE.

ACKNOWLEDGEMENT

Acknowledgements are due for all the seniors, our team leaders and the review experts for their constant guidance. The authors are extremely grateful to director SAC for his continuous encouragement to achieve higher objectives and the activity under this paper is one such successful attempt

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New Packaging Configuration of CCGA1752 leading to Challenges in its Assembly Process Reliability Assessment

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***Abstract*—The Virtex-5 FPGA from Xilinx is increasingly being used for its capability to meet the advanced processing requirements of emerging payload applications. The challenge in assembly of the latest 1752-pin Ceramic Column Grid Array (CCGA) package version of this Xilinx Virtex-5 FPGA is that the column assembly as well as decoupling capacitors on the package uses the same solder composition as that which is employed for assembly of the device on multilayer boards. This poses the risk of solder joint re-melt of columns from package and also that of capacitor on the package in case stringent control is not exercised. Optimizing the assembly process and assessing its reliability before it can be used for space payload applications is the need of the hour and also the real challenge.**

This paper describes about the challenges faced in assembly of this 1752-pin CCGA package, reliability assessment of the optimized assembly process and its comparison with the assembly of previous Virtex-4 1140-pin CCGApackage and the confidence generated thereof.

***IndexTerms*—CCGA, Pb80/Sn20, Six sigma column, CN1752, CF1140,**

I. Introduction

Virtex-4 FPGAwith 1140-pinCCGA package from Xilinx have been used to develop and optimize the assembly process at Space Applications Centre (SAC, ISRO). These packages were having solder columns attached to ceramic substrate using Column Last Attach Solder Process (CLASP) from IBM. The CLASP process uses palladium (Pd) doped 63Sn/37Pb solder to attach the high melting point 90Pb/l0Sn solder column on the substrate side. The Pd doped 63Sn/37Pb fillet has a slightly higher second reflow temperature (256°C) due intermetallics formed between Pd& Sn in first reflow [8]. This allows the columns to be attached to the PCB using 63Sn/37Pb solder paste without disturbing the substrate side column joint.

Xilinx no more employs the services of column attachment from IBM as the assembly line has been shut-down [3]. Hence, this work is now being done by Six Sigma with new column configuration 80Pb/20Sn with Cu-spiral reinforcement. The process of column attachment at Six Sigma uses standard 63Sn/37Pb (without any doping). This scenario raises a possibility of column to package joint re-melt during reflow assembly on the multilayer boards that may results in column kick-off [4].

This paper describes the reliability assessment of process optimization to overcome the concerns arising due to this new packaging style. Hot gas reflow process is used for selective soldering of these CCGA packages over multilayer boards.

II. Challenge Identification

A. CN1752 CCGA Package & Assembly Requirements

CN1752 CCGA package of Xilinx Virtex-5 FPGA device uses solder column which is constructed of 80Pb/20Sn solder wrapped in a copper ribbon. The wrapped column is then tinned with eutectic solder 37Pb/63Sn. The flip-chip assembly & decoupling capacitors soldering done using eutectic solder 63Sn/37Pb. The detailed construction of column &package is given in Fig.1 & 2 respectively.

In CF1140 package, the columns are made of Pb90/Sn10 and attached to package-side with Pd-doped Sn63Pb37 (IBM CLASP process) & capacitor and flip-chip are attached using Pb95/Sn5 which were having second reflow temperature of 256^0C& 312^0C respectively. However, in CN1752 package, the package-side column &capacitor and flip-chip are attached with eutectic Sn63/Pb37 which can melt at 183^0C in second reflow. A comparison between CF1140 & CN1752 CCGA package style is summarized in Table-1.

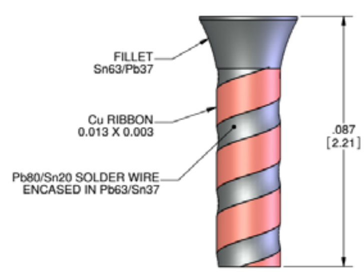

Fig. 1. Pb80Sn20 Cu spiral reinforced Column

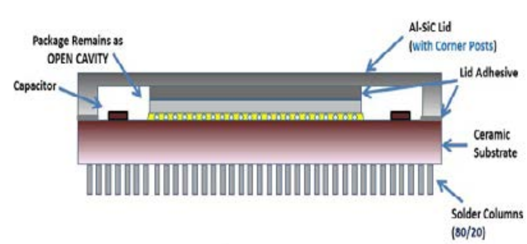

Fig. 2. CN1752 CCGA Package [3]

TABLE I. PACKAGE COMPARISON OF VIRTEX-4 (CF1140) & VIRTEX-5 (CN1752) FPGA

Sr. No.	Features	CF1140 CCGA	CN1752 CCGA
1	No. of I/O pins	1140	1752
2	Device Packaging	IBM	Kyocera
3	Package Columning	IBM Using Sn63Pb37 with Pd impurity (CLASP Technology)	Six Sigma Using Sn63Pb37
4	Solder columns	**90Pb10Sn** (Liq. temp.- 302^{0}C) (Sold. temp.- 275^{0}C)	**80Pb20Sn,** with copper ribbon reinforcement & tinned with 63Sn37Pb (Liq.temp.- 277^{0}C) (Sold.temp.- 183^{0}C)
5	Solder for Flip Chip Bumps (Silicon Die attachment)	High Lead Solder **(95PbSn5)** (Liq. temp.- 312^{0}C) (Sold. temp.- 308^{0}C)	Eutectic **(Sn63Pb37)** (183^{0}C)
6	Solder for Capacitor Attachment	High Lead Solder **(95PbSn5)** (Liq. temp.- 312^{0}C) (Sold. temp.- 308^{0}C)	Eutectic **(Sn63Pb37)** (183^{0}C)
7	Mechanical Packaging Lid	SiC (Electrically Non Conductive)	Ni plated Al-SiC (Electrically Conductive)
8	Package weight	~23 grams	~49 grams

Thus, the issues faced with CN1752 CCGA packaging are as follows,

- Lower solidus of column to package attach solder-alloy
- Lower solidus temperature of Column
- Lower solidus of Flip-chip bumps
- Lower solidus of Chip capacitors on package
- Higher Package weight & thermal mass

These issues raise the possibility of column to package joint re-melt during reflow assembly on the multilayer boards and may result in column kick-off due to package weight. Also, re-melting may disturb the flip-chip bumps & capacitor joints which may degrade the reliability of the devices.

Trial runs in the mass reflow systems showed a fair amount of thermal equilibrium across the entire PCB assembly during reflow, which made the above problem easily solvable.However, in prototyping/low volume production with mixed technology components, selective reflow is preferred, and thus, a need arises to optimize the reflow profile to achieve the thermal equilibrium and the quality solder joints without affecting the package reliability.

Trial runs with soldering profile as well as preheating of PCBs with different temperature & duration were carried out. The aim was to minimize the temperature gradient of PCB-side column solder joint & package-side solder joint to avoid column kick-off during reflow as well as achievement of required solder reflow profile at solder joint between column and PCB.

B. PCB material& Layout Requirements

To minimize temperature gradient between package top and bottom during selective reflow process, preheating of PCB is required to be done at higher temperature and duration. Polyimide PCBs are preferred option over FR4 PCB because of margin available due to its high glass transition temperature (Tg). For assembly process optimization, both Via-in-pad design & Dog-bone design is used in PCB layout design. Non-solder mask defined (NSMD) pad design are used as it avoids generation of high stresses on solder joint area [1]. The board size is 10"x 8" and board finish is Hot Air Solder Levelling (HASL). The board thickness is 2.4mm and PCB properties are given in table 2.

TABLE II. PCB LAMINATE PROPERTIES

Sr. No.	Property	Polyimide	High Tg FR4
1	Glass Transition temperature Tg (^{0}C)	>250	180
2	CTE (ppm/^{0}C) X-Y Z	 55 16-17	 45 14-17
3	Water absorption (%)	0.19	0.15

C. Soldering Process Requirements

A peak temperature value at the device top surface was targeted (220°C) less than of maximum permissible reflow temperature suggested by the manufacturer. Experiments were carried out to achieve thermal equilibrium between the device top and solder site within a safe thermal gradient of 5 °C and to avoid thermal constraint of PCB and package. Bottom Infrared Heaters are slower as compared to hot gas at nozzle. To overcome this issue, required mechanism was generated by tweaking reflow system to achieve required ramp rates. Soak phase is of the utmost importance as flux activation occurs during this phase. A fast ramp causes flux explosion, creating discrete solder balls on the solder site, while a very slow ramp creates (<1 °C/s) undesired paste oxidation. At temperature ramp stage, temperature rate achievement is very critical for this package, since it has optimal reflow ramp rate was kept between 3°C/s to 4°C/s. A cool down phase ramp rate from −3 °C/s to −4 °C/s is used. Type V solder paste and liquid Rosin Mildly Activated (RMA) flux are used for the assembly preparation [2].

III. QUALITY ASSESSMENT TESTING

Quality evaluation of solder joints was carried out using three different methods viz.,

- Radiography inspection
- Visual Inspection monitoring of outer row solder-joints
- Electrical Inter-Connection Resistance (ICR)monitoring of daisy chains

The prominent failure mode in CCGA package assembly is solder joint crack due to stresses exerted by CTE mismatch between PCB (14–17 ppm) & CCGA device (6–8 ppm). This

failure mode is stimulated by Accelerated Thermal cycling test (ATC) (-55°C to +105°C, 15-minute dwell at each extreme & 3°C per minute ramp rate) as per profile given in Fig.-3.

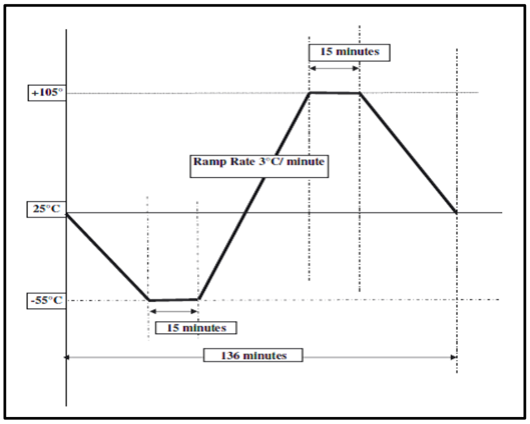

Fig. 3. Thermal Cycle profile for quality evaluation

Fig. 4. Thermal cycling test in Single-zone chamber

A total of 500 cycles testing has been carried out in steps of 100 cycles. Visual inspection, radiography & ICR measurements of daisy chain were done after every 100 cycles to note the degradation in the solder joint quality, if any. Observations & test results for CN1752 assemblies along with comparison with CF1140 assemblies are summarized in Table-4.

IV. Discussion on Test Results

1) The freeze lines observed in initial visual inspection in Package-side column solder joint of CN1752 package denotes that the solder joint got slightly melted during reflow soldering to PCB. In CF1140 package, due to Palladium doping, the re-melting does not occur and so the joints are smooth.
2) CN1752 package is using column material as 80Pb/20Sn, with copper spiral reinforcement. The copper spiral is acting as reinforcement and avoiding the column bending in temperature cycling. This has avoided any degradation in PCB side solder jointtill 500 thermal cycles.
3) Chip-capacitor joints are intact after reflow and remain unaffected after 500 thermal cycles.
4) Radiography inspection reveals no voiding, bridging, solder balls and metallic contamination in both CF1140 & CN1752.
5) Initial electrical measurement of daisy chain showed no open circuit and electrical resistance change after 500 thermal cycles was measured within 1%.

V. Conclusions

The observations & test results of reliability assessment exercise for process optimization proves that whatever assembly challenges that arose due to change in package style to CN1752 CCGA have been overcome, and at the same time, the other packaging elements like column-joint to package and chip-capacitor joint to package are intact and have successfully withstood the process optimization. This process will now be regularly employed in soldering of Virtex-5 CN1752 CCGA devices in ongoing & future space programmes of SAC-ISRO.

VI. Future Scope

The CN1752 package assemblies will be tested for temperature cycling up to failure and required database will be generated to calculate the fatigue life of the solder joints.

These assemblies are also required to be subjected to vibration & mechanical shock loads to check its survivability under actual launch vehicle flight stresses.

Since these are mechanical packages without functionality, the effect of reflow process on flip-chip bumps could not be evaluated. These could only be evaluated on actual functional devices.

ACKNOWLEDGEMENT

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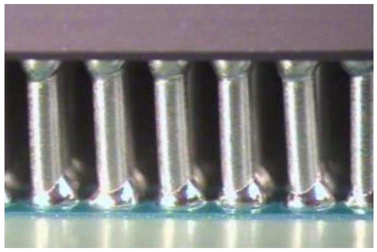
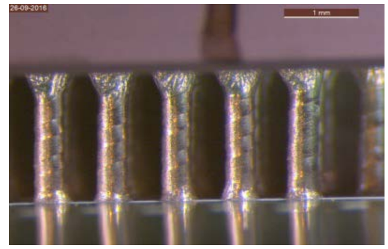
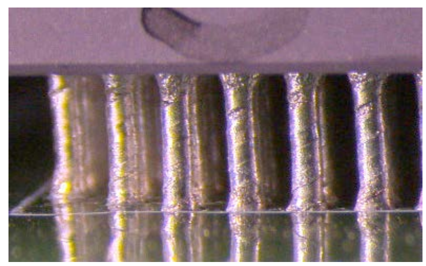
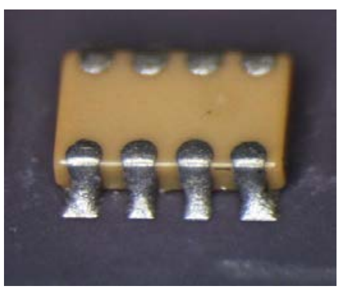
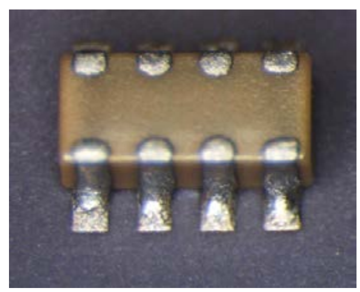
	CF1140 package Assembly	CN1752 package Assembly
Visual Inspection of outer row column solder joints		
Initial	Both package side & PCB side solder joints are smooth and properly wetted. 	PCB side solder joints are smooth & wetted but package-side has freeze lines 
After 500 thermal cycles	Corner Columns deformed as “S”-shape structure 	No corner column deformation observed 
Visual Inspection of Capacitors solder joints		
After 500 thermal cycles	Capacitor solder joints are inspected after 500 cycles and appeared with grainy finish. No cracking or fracture in solder joint 	Capacitor solder joints are inspected after 500 cycles and appeared with grainy finish. No cracking or fracture in solder joint. 
Radiography Inspection		
Initial & after 500 cycles	No voiding, bridging, solder balls and metallic contamination	No voiding, bridging, solder balls and metallic contamination
Electrical Resistance of Daisy chains		
Initial & after 500 cycles	No Deviations	No Deviations

TABLE I. COMPARATIVE RESULTS FOR STANDARD CF1140 PACKAGE ASSEMBLY AND NEW CN1752 PACKAGE ASSEMBLY

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Improvements in Capacitor Attachment Process for Resistor-Capacitor Networks

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ABSTRACT

Resistor Capacitor Networks (RCNWs) are developed and Qualified for usage in various space programs due to their advantages with respect to performance, reliability, size and weight over discrete components used on PCB. The RCNWs are subjected to stringent screening tests as per MIL-PRF-83401 on 100% basis. Successfully screened samples are being used in flight hardware. Electrical failures are seen in RC Networks in card level testing. Failure Analysis revealed that failure of RC Networks are due to resistive short mode failure of one of the ceramic chip capacitor CDR-31 as a result of excessive spreading of Conductive epoxy beneath the capacitor. Simulation tests were carried out to confirm the failure is due to above mentioned reason. Chip Capacitor attachment process is revisited and process improvements are made based on failure analysis feedback. Samples are realized with new process and evaluated the effectiveness of new process on samples. This paper discusses about the failure analysis, simulation experiments conducted, failure assessment, adoption of new process for sample realization, conduct of process qualification and the process qualification test results.

Keywords: RC Networks, Process, Chip Capacitors

I. INTRODUCTION:

Single-in Line (SIL) Networks are extensively used in all spacecrafts of ISRO. SIL Networks qualified for space programs of ISRO are of two types: Resistor Networks (RNWs) and Resistor-Capacitor Networks (RCNWs). The resistors are screen printed on ceramic substrate and leads are attached using solder dip method. In RC Networks discrete Chip capacitors are attached in addition to the Thick film resistors. Discrete Chip capacitors are attached to Thick Film Metallization by manual dispensing of Conductive Epoxy below the ceramic chip capacitors termination and Non-conductive Epoxy in the centre (below the body of capacitor) for mechanical strength as shown in Fig.1. Then capacitor is placed and pressed gently & subject to scheduled curing. Post curing, Conductive epoxy build up is given from 3 sides and made sure that build up is up to 20% of die height.

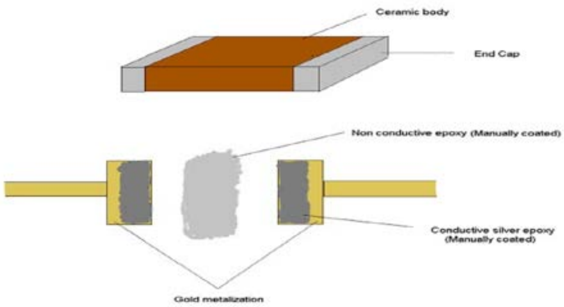


Fig1 Placement of chip capacitor, C onductive & Non-Conductive epoxies

Resistors/Capacitors are then protected with epoxy powder encapsulation. Photograph of an encapsulated RCNW are shown in Fig: 2

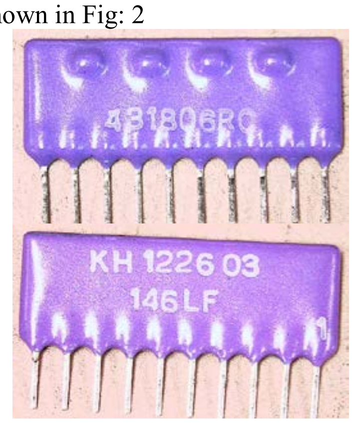


Fig2 RCNW with monogram on one side & Sl. No. oncomponent side

The above processes/operators are qualified prior to use in realization of Networks. Electrical failures are observed in RCNWs (146LF) during card level testing of Control System packages. This paper discusses on the analysis conducted to understand the root cause of the failures observed and identification/implementation of corrective actions.

II. QUALIFICATION APPROACH:

Newly designed RCNWs are subjected to qualification as per the requirements of MIL-PRF-83401[1] & PMPD /

SPES / HMC/GEN/008 [2]. The following is the qualification approach:

a) Qualification of New Processes (if any)
b) Pre-Qualification Tests
c) Screening
d) Product Qualification

All processes used to realize RC Networks are qualified and on successful completion of pre qualification tests, Batch of RC Networks is fabricated. Screened Networks from the first production lot are subjected to Qualification tests comprising of Environmental tests, Mechanical tests, High and low temperature operation & High and low temperature storage, Life test and 25 de g Power rating tests.

Six types of RC Networks are designed, developed and qualified to use in all spacecraft programs of ISRO Satellite Centre.
On successful completion of qualification, FM RC Networks are realized on a qualified line and are subjected to screening tests as per the requirements of MIL-R-83401[1] prior to FM use. Approximately 200nos of RCNWs (consisting of 6 types) are being used in each spacecraft.

III. FAILURE ANALYSIS:

Electrical deviations were observed in three numbers of Line Filter RCNWs (146LF) during card level testing. These RC Networks were realized on qualified line/successfully screened and were cleared for Flight use.

Each 146 LF consists of 4 sections (fig. 4) and Channel corresponding to one of the sections was not working. The failed RCNW was removed from the card and was subjected to failure analysis as per MIL-STD-883[4] method 5003 as per the following sequence.

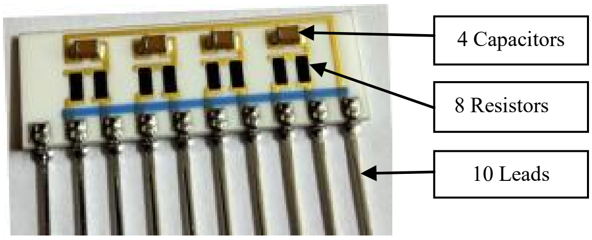


Fig3 Internal view of RCNW Line Filter (146LF)

a. EXTERNAL VISUAL EXAMINATION

Visual inspection was carried out and no visual anomalies were observed such as crack on the body, lead corrosion etc.

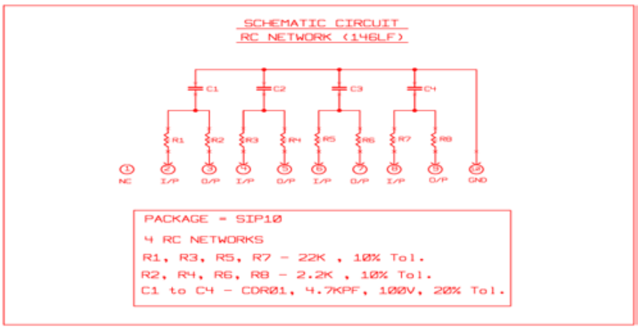


Fig4 Circuit Schematic of RCNW Line Filter (146LF)

b. ELECTRICAL MEASUREMENT:

Reported failure in the RC network was confirmed by electrical measurement. Values of the thick film resistors found to be within specified limit. But ceramic chip capacitor (CDR-01/31, 4.7kpF, 10% 100V) in one of the sections was found to be electrically degraded. Capacitance (C) and dissipation factor (DF) of failed chip capacitor (C3) are within the specified limit, only insulation resistance (IR) is beyond the specified limit. The results of electrical characterization of ceramic chip capacitors of all four sections in the failed Network are given in Table 1 & 2.

Table1: Capacitor Measurement

Tested Capacitors	Measured Parameters					
	Capacitance in kpF @1kHz		DF @ 1kHz		IR in Ω @ 100V for 30s	
	Measured	Specified	Measured	Specified	Measured	Specified
C1	4.46	4.7 ±10 %	0.055	<0.06	6.82×10^{11}	$>10^{11}$
C2	4.51		0.050		6.27×10^{11}	
C3	4.57		0.052		Over current (22.34kΩ)	
C4	4.53		0.057		7.38 x1010Ω (slightly degraded)	

Table 2: Measurement of Output Settling Time

Tested Capacitors	Output Settling Time (Specified Limit 400 to 600μs)
	Test Condition: I/P V=5V @ 0.5kHz, Pulse Width=1ms
C1	540 μs
C2	540 μs
C3	Improper waveform
C4	540μs

c. RADIOGRAPHIC INSPECTION

The failed RCNW was then subjected to Radiographic inspection and it did not reveal any visual anomalies within the device.

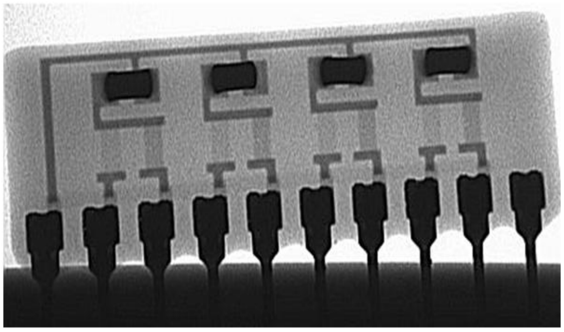


Fig 3: X-ray Inspection of the RC network did not reveal any visual anomalies, internal to the device.

d. DE-CAPPING & INTERNAL VISUAL EXAMINATION

The failed RCNW was then de-capped (through chemical etching process) and Visual inspection was carried out. Visual inspection on the rear side of the removed capacitors revealed excessive spreading of conductive epoxy below failed capacitor (which showed degraded insulation resistance) which in turn reduced the gap between two terminals of capacitor. Electrical Measurements (C, DF and IR) were conducted on all the four capacitors after removal from the substrate and all capacitors including the failed capacitors met the required specification. The results of electrical characterization of ceramic chip capacitors after De-capping are given in Table 3.

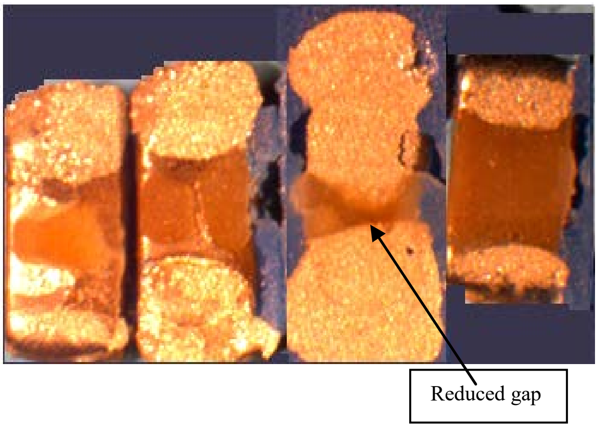


Table 3: Post de-capping measurement on individual Chip Capacitors

Tested Capacitors	Measured Parameters					
	Capacitance in kpF @1kHz		DF @ 1kHz		IR in Ω @ 100V for 30s	
	Measured	Specified	Measured	Specified	Measured	Specified
C1	4.66	4.7 ±10%	0.015	<0.06	4.83 X 10^{11}	>10^{11}
C2	4.63		0.017		4.47 X 10^{11}	
C3	4.58		0.016		5.70 X 10^{11}	
C4	4.71		0.017		6.93 X 10^{11}	

e. TRIAL SAMPLES

The process of capacitor attachment and application of epoxies is a manual process. Training was provided to the operators to control the quantity and application method so as to avoid spread due to excess quantity of Conductive epoxy / Non-conductive epoxy. Several samples were realized with the existing process of capacitor attachment. Visual inspection prior to encapsulation revealed excess quantity of conductive and non conductive epoxy.

The capacitors were then sheared from the Ceramic substrate. Visual inspection of the attachment area revealed mixing of conductive / non-conductive epoxy. During attachment process when Conductive and Non-conductive epoxy is applied and the component is placed/pressed, epoxy has spread and mixed. Mixing of conductive epoxy created a resistive path between the two terminals of capacitors.

f. ROOT CAUSE

Based on the above analysis on failed sample and trial samples it was concluded that due to application of excess quantity and the application method, Conductive and Non-conductive epoxy has spread and got mixed below the failed capacitor after placement which in turn reduced the gap between two terminals thereby causing reduction in IR. This failure has occurred after repeated thermal excursions like soldering, cleaning, power ON/OFF cycling which occur during the realization of electronic hardware. Since the failure is in short mode / low resistance path across capacitor, no output will be present in the signal line affected.

IV. CORRECTIVE ACTION

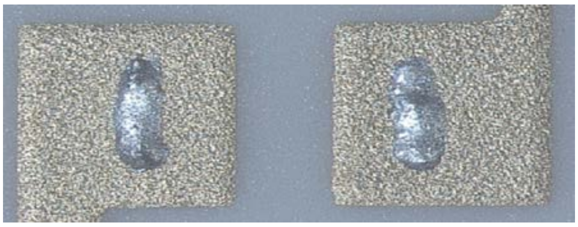
a. EXISTING RC NETWORKS

Several batches of RCNWs of all six types realized using the above process for capacitor attachment was cleared for FM usage after successful screening. Samples were drawn from all batches and subjected to Humidity test (with burn-in configuration used as part of screening) as per MIL-STD-202[1], Test Method 106 for 240hrs at 65^0 C /-10^0C and 80-98% RH. Visual Inspection and Electrical test conducted prior to and post Moisture Resistance test met visual/electrical specifications. Based on these results the batches of RCNWs fabricated with the above process are cleared for flight usage.

b. PROCESS IMPROVEMENT

Since this process of dispensing epoxy is manual, application of controlled amount of epoxy to avoid spreading/mixing on placement of capacitor was difficult. The process of attachment of ceramic capacitor was revisited and modified to avoid spreading/mixing of epoxies with identification of in-process QC check points. All RC Networks realized in future shall be realized using following modified process:

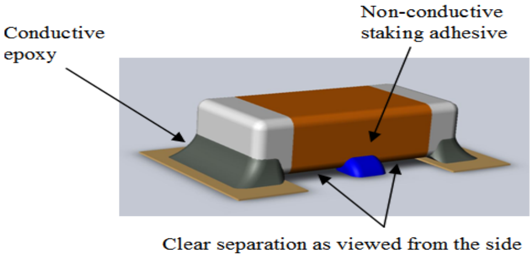
a. Minimum conductive epoxy is to be dispensed (using 10mil tip spatula) on the pads as shown in photo:



b. Non conductive epoxy shall not be dispensed.
c. Capacitor to be placed & pressed gently and subjected to scheduled curing. After curing the attachment area shall look as shown in photo:

d. QC Inspection to be carried out and observations are to be recorded.
e. Conductive epoxy build up is to be given from 3 sides and made sure that build up is up to 20% of die height.

f. A minimum dot of non conductive epoxy (using 10mil tip spatula) is to be applied at the center of capacitor body on both sides of capacitor. The cured capacitor assembly shall look as shown in the photo below.



g. QC Inspection shall be carried out and observations are to be recorded before and after subjecting to scheduled curing.

V. INCREMENTAL PROCESS QUALIFICATION

Samples were realized with the modified process. Each sample consisted of four discrete Chip Capacitors. The samples were subjected to process qualification tests as per the requirements of ISRO-PAS-206[5] and samples successfully completed the required tests as given in Table-4.

Table 4: Qualification of discrete chip capacitor attachment process

Sl No	Test	Condition	Remarks
1	R, C & Electrical Measurements	As per procedure	Pass
2	Visual Inspection		Pass
3	Temperature Cycling	-55^0C, $+25^0$C $+70^0$C 15min 5min 15min	100 cycles
4	R, C & Electrical Measurements	As per procedure	Pass
5	Visual Inspection		Pass
6	Mechanical Shock	3000g, half sine, 0.3msec, 5pulses	
7	Visual Inspection		Pass
8	R, C & Electrical Measurements	As per procedure	Pass
9	Die Shear	2019 of MIL-STD-883[4]	Pass

Based on the successful completion of evaluation, **Modified Process for attachment of discrete Chip Capacitor attachment in RC Networks is qualified**.

VI. CONCLUSION

Failures observed in RC Networks were attributed to spreading / mixing of conductive and non conductive epoxies which are used for attachment. This spreading/mixing was prevented by revisiting and modification in the process. The new process of capacitor attachment has successfully completed the process qualification. Samples from first production lot of RC Networks realized using modified process will be subjected to Incremental Product Qualification. Upon successful completion of Incremental Product Qualification, the process will be cleared for fabrication of FM RC Networks.

ACKNOWLEDGEMENTS
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Highly Accelerated Thermal Shock Testing of Printed Circuit Board Plated Through Vias

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Abstract **- Finished hole size of PCB via has changed from 32 mil to 16 mil to facilitate the attachment process of fine pitch devices in high density designs. Microsectioning is the most commonly used via integrity assessment tool in PWB industry today. It requires extensive sampling and experience in the areas of sample preparation, polishing & etching. Microsectioning is a critical operation that uncovers the minute flaws that occur within vias and the results of this operation determines a PCB's acceptability or rejection. The variability in terms of location accuracy and polishing dynamics of micro-sectioning operator/equipment can influence the decisions pertaining to acceptability. As via sizes are reducing, these uncertainties get more widened and require additional tests to assess the reliability of the PCBs. Also the acceptance test methods practiced today do not address the reflow soldering cycles which the PCB is expected to undergo during assembly wiring operations.**

This paper briefly describes the current acceptance tests conducted for the clearance of onboard PCBs, limitations and proposal to introduce additional tests for the acceptance of fine via PCBs for onboard application. The thermal stress test system used in the paper is not an alternate but the extended test method to assess the plated through hole integrity specifically when we are employing reflow soldering process at assembly stage. As part of HATS testing (Highly Accelerated Thermal Shock Cycling Test) the specimen undergoes six reflow cycles followed by thermal cycling wherein the daisy chain resistance is monitored and compared at every cycle with value observed at initial cycle. Percentage change in the resistance value is plotted against the number of cycles and 10% change is set as the threshold. The specimen is a modified IPC-D coupon so as to capture the thermal stress defects at shorter number of cycles. This paper also presents the details of the test coupons designs, rationale for changes made and their effectiveness in finding the defects.

Keywords-Printed Circuit Board; Reliability Testing; Electronic Fabrication; Space borne systems

I. INTRODUCTION

PCB interconnect technology is becoming more and more complex due to miniaturization of electronic assemblies. Use of Miniaturized Surface Mount Devices [SMDs] like CQFPs (Ceramic Quad Flat Packs) are becoming dominant due to the requirements of increased functionality and performance. These devices having large number of I/Os, occupy small foot print area and demand high interconnection density on the Printed Wiring Boards [PWBs].

Table 1depicts the design rule and feature size reductions evolved in onboard PCB layouts from IRS-1A to Cartosat-2D.

Table 1. Feature size reduction in PCBs

Feature	IRS-1A Year 1988	Cartosat-2D Year 2017
Minimum Line width	0.50 mm	0.125 mm
Minimum Line Spacing	0.50 mm	0.100 mm
Minimum Via Diameter	0.80 mm	0.40 mm
Via feature	Open via	Filled Via
Maximum No. of layers	2	14
PCB thickness (Typical)	1.6 mm	2.4 mm
Copper Thickness	1 + 1 ounce	½ + 1 ounce
Via type	Through via	Through via & Buried via
Device complexity	DIP ICs 2.54 mm pitch	0.5 mm pitch CQFP

The term "difficulty factor" is used to quantify the effects of increasing board thickness and smaller via size on plating, by the relationship

Difficulty Factor[3] = Aspect Ratio x Board Thickness $= \frac{t^2}{d}$ where t is the board thickness and d is the finished diameter of the vias. Since the effect of board thickness is squared, doubling the board thickness from 1.6 mm to 3.2 mm will increase the plating difficulty factor by four, given the same via size. The difficulty factor of standard 0.8 mm via on 2.4 mm thick PCB is 7.2 and 0.4 mm via on 2.4 mm thick PCB is 14.4.

Microsection Analysis

Microsectioning analysis is the most commonly used PTH quality assessment tool used at PWB industry today. It requires extensive sampling and experience in the areas of sample preparation, polishing & etching. Microsectioning is a critical operation that uncovers the minute flaws that occur within the PCB and the results of this operation determine a PCB acceptability or rejection. The variability in terms of location accuracy and polishing dynamics of micro-sectioning operator/equipment can lead to different opinions or conclusions about quality assessment. An additional coupon testing method detailed here uses the standard IPC test pattern which is modified based on the experiments conducted on solder dip coupons.

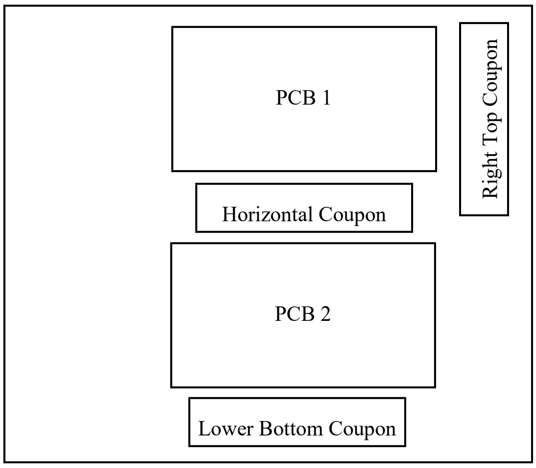
Thermal shock cycling is conducted as per IPC-TM-650-2.6.7.2 which is modified based on the requirement

listed in ECSS-Q-ST-70-10[4] para 7.5.d wherein the delta temperature is set as 200 ^{o}C. Test results are discussed and can be extended for acceptance testing of High Density Interconnect (HDI) PCBs or boards with fine line width, spacing and filled fine vias.

II. PCB ACCEPTANCE TESTING

Acceptance tests defined in ISRO-PAX-304[5] are based on a small set of samples ie., test coupons that are manufactured with the same materials and processes used for the PCB. For the tests to be valid, the samples must be part of the same panel and forms the representative of the PCB. If the manufacturing process, which includes the materials, equipment, and processes, is controlled as per the Process Identification Document, then the test results are valid. Coupons are arranged in the panel as shown in Figure 1.

Figure 1: Coupon arrangement on a PCB panel



Though the test coupons are designed to capture the process deviations to detectable defects, if manufacturing process is not controlled, it can lead to significant variations in quality. The situation further worsens when the line width, spacing, via dimensions are reduced. There are 16 tests conducted on PCB/Coupon prior to the clearance of PCBs for onboard application.

Table 2. PCB Acceptance test plan

Sl No.	Test Name	Test on	Quality Attribute verified
1	Bare board testing	Actual board	Continuity, cross continuity and isolation
2	Mechanical inspection	Actual board	Length, width, thickness, mounting hole pitch, warp, twist
3	Visual inspection	Actual board	Laminate, conductor, surface finish, solder mask, barrel surface quality
4	Peel strength	Coupon	Conductor adherence to laminate
5	Bond strength	Coupon	Plated copper adherence to barrel and Conductor adherence to laminate
6	Rework simulation	Coupon	Reworkability by manual soldering
7	Solder dip	Coupon	Ability to with stand thermal stress
8	Solderability	Coupon	Ability to get wetted by solder
9	Inter connection resistance	Coupon	Conductor width, thickness, plated copper quality
10	Insulation resistance intra layer	Coupon	Surface resistance of laminate
11	Insulation resistance inter layer	Coupon	Resistance across layers
12	Dielectric with standing voltage intra layer	Coupon	Voltage withstanding property of laminate material within the layer
13	Dielectric with standing voltage inter layer	Coupon	Voltage withstanding property of laminate material between layers
14	Microsectioning of initial sample	Coupon	Barrel integrity
15	Microsectioning of solder dip tested samples.	Coupon	Barrel integrity after thermal stress tests
16	Microsectioning of rework simulated samples.	Coupon	Barrel integrity after rework simulation

Plating thickness variation across the panel is about 8 to 21 microns in a PCB fabrication line. Table 3 lists the copper thickness variation noticed in five panels from PCB fabrication line.

Table 3. Copper thickness variation within the panel

Panel	Minimum Copper thickness in H coupon Barrel in µm	Maximum Copper thickness in Right Top Coupon Barrel in µm
1	106	119
2	107	126
3	112	133
4	112	129
5	123	131

Out of sixteen tests listed in Table 2, last three tests are primarily intended for evaluating the barrel integrity wherein the number of vias evaluated/microsectioned will be less than ten. Number of plated through holes (vias) in a medium density MLB will have an average of 1000 vias in it. This will increase by two to three folds when via diameter is very fine and number of interconnects are very large. Also, acceptance testing has not addressed the multiple reflow soldering cycles which the PCB may undergo during the assembly wiring stages. Plating measurement within different panels indicates that the number of via samples to be evaluated for the clearance of panel needs to be increased to make fairly good assessment due to variation in plating thickness across the panel. *These observations are effectively used in the design of test coupon for HATS testing by:*

- Introduction of six reflow cycles on coupon prior to HATS testing
- Using more than 100 vias in the HATS coupon.

III. EFFECT OF HUMIDITY

PCBs are stored at lab environment for longer period of time at different environment. Though ISRO-PAX-304 suggests vacuum sealed storage of bare PCBs, it is required to consider the storage conditions of intermediate assembly phases. Considering this, two dozens of samples were subjected for humidity storage to study the effects of humidity on MLBs and to identify the location of failure during thermal stress. It was found that inter connection resistance of the samples were linearly increasing with the number of storage hour.

Micro cracks in the barrel (at knee of barrel, or in the barrel on Z axis or in the interface of barrel plating to inner layer copper) are responsible for the increase in the interconnection resistance.

Moisture absorbed test samples were subjected to solder dip tests to simulate the failure of PTHs of MLBs during repeated soldering which has absorbed humidity during handling / storage. Interconnection Resistance (ICR) measurements and microsection analysis were carried out on samples to identify the location of failure

Figure 2: Interconnection Resistance Change vs Humidity storage hours

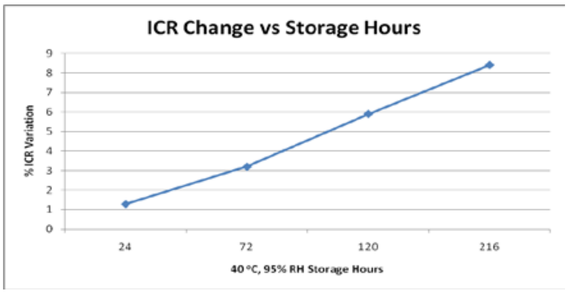
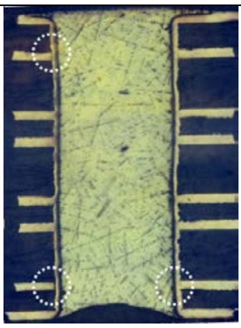
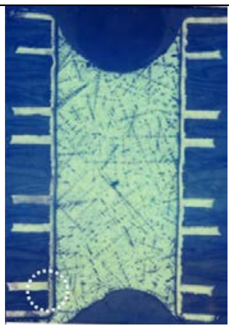
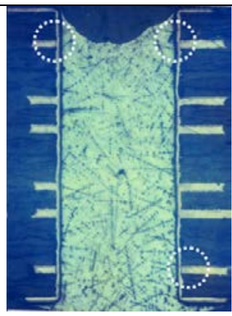
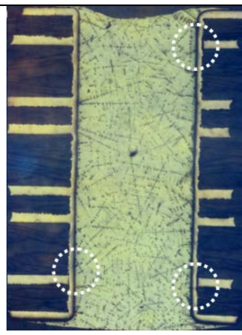


Figure 3: Microsection results after 95% RH, 42 °C humidity storage followed by solder float test.

	
24 h Storage Observation: Thick demarcation line is visible in last but one layer	72 h Storage Observation: Thick demarcation line is visible in last but one layer

	
120 h Storage Observation: Thick demarcation line is visible in last but one layer	216 h Storage Observation: Thick demarcation line is visible in last but one layer

All the above samples were baked as per standard procedure of 85 °C, 3 h prior to the solder dip test. The above test results indicate that:

- PCBs absorbed moisture during their storage.
- Baking at 85 °C / 3 h is not sufficient to remove the moisture absorbed into the PCB.
- Failure location is last but one layer interface of the MLB

This result is effectively used in the modification of IPC-D coupon so as to maximize the resistance variation within a fixed number of thermal stress cycles.

IV. HIGHLY ACCELERATED THERMAL SHOCK TESTING

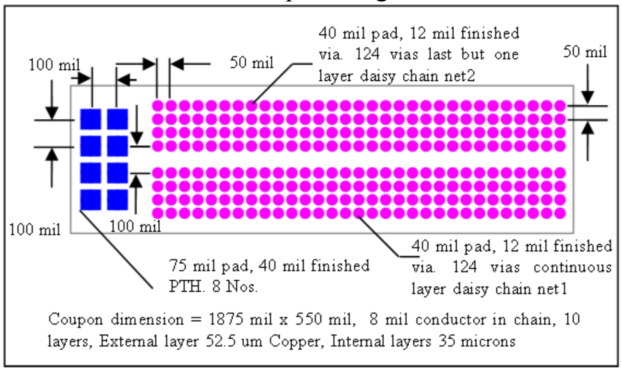
Highly Accelerated Thermal Shock (HATS™) is a traditional air-to-air methods to evaluate the reliability of electronic interconnections within the circuit board and connections between the packages and the circuit board. The HATS methodology is adopted by the Process Capability, Quality and Relative Reliability ($PCQR^2$)[6] sub-committee of IPC for relative reliability testing. The technique utilizes a single chamber that is alternately heated and cooled by an air stream that is forced on the samples. The chamber varies the temperatures from -65 °C to +135 °C during the cycling. Each coupon with daisy-chain nets, is loaded into the chamber with necessary interconnections to conduct 4 wire resistance measurements at every second. Precision electrical resistances of each of the nets is monitored during thermal cycling, providing data that shows the degradation of the nets during the test.

Test coupons are designed with software that is run from the Internet with a web browser. Coupon sizes range from a minimum of ½" x 1" to a maximum size of 1" x 2". Designs can be created for circuits with two to eighty layers. Specific design parameters for each of the four daisy-chain nets include via type (through, blind, buried, or stacked), hole-size, land-size, interconnect track width, interconnect sequence, and grid size. Further, each net can include/exclude teardrops, non-functional lands, and

soldermask coverage. Upon completion of the design process, the Gerber files are "zipped" and emailed/downloaded to the designer. The design shall be added along with the standard ISRO-PAX-304 coupons on the panel areas and manufactured with on-board PCBs to evaluate the reliability of PCB. Following are the modifications in the coupon design and test conditions made.

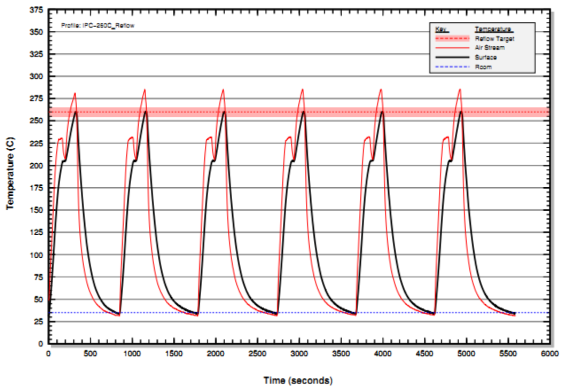
- Out of two nets in IPC-D coupon, Net1 is made with continuous daisy chain involving connections in all layers. Net2 is made with daisy chain comprising connections only in last but one layers.
- Temperature limits were set as -65 °C to +135 °C to get delta temperature of 200 °C.
- Number of vias in each net is 124 and total number of vias per coupon is 248.
- Considering the commonly used line width in 1 ounce designs, 8 mil conductor width is used for connections.
- Total copper thickness in external layers is set as 52.5 microns by considering the commonly used copper thickness of fine line PCB designs

Figure 4: Modified IPC-D coupon design.



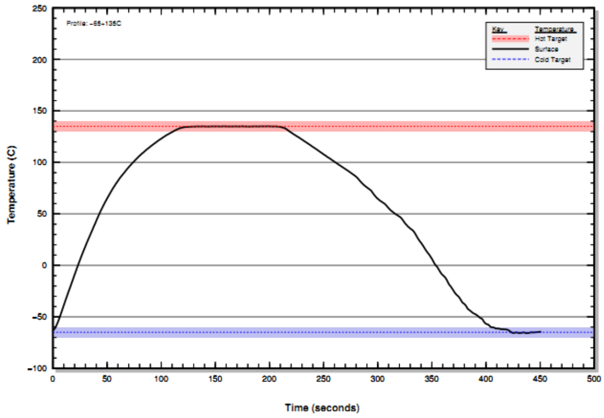
Coupon preparation involves a pre-baking at 120 °C for a minimum of six hour and then exposure to at least six convection reflow cycles of 260 °C (Temperature Control ± 5 °C on set value) which complies to IPC-TM-650 test method 2.6.27.

Figure 5: Reflow temperature profile plot



Thermal cycling of -65 °C to +135 °C (ΔT = 200 °C, Temperature Control: ±2 °C on set value: As per IPC-TM-650 2.6.7.2) shall be carried out on coupon with 1 second per mil PCB thickness dwell time. This is to ensure that the PCB coupon temperature is stabilized.

Figure 6: Temperature cycling profile



During the test, precision 4-wire (Kelvin) resistance measurements were made on each daisy chain net, at a rate of 1 reading per second. Both the high resistance and low resistance reading during each cycle are recorded for each net.

Absolute percentage change in resistance is referenced to the highest resistance recorded during the first cycle, and is calculated by:

$$100 * \left[1 - \frac{\text{Resistance high in cycle [i]}}{\text{Resistance high in first cycle}}\right]$$

Where i is the cycle number.

Each of the nets experiences very small change in resistance over the first 200+ cycles. Beyond this point, a gradual increasing trend can be observed mostly on the nets which are made through last but one layers.

V. RESULTS AND DISCUSSIONS

Two coupons each having two nets were subjected for Highly Accelerated Thermal Shock Cycling tests listed above.

Net1 is made with continuous daisy chain involving connections in all layers wherein Net2 is made with daisy chain comprising connections only in last but one layers.

Figure 7: Resistance Variation in continuous layer daisy chain

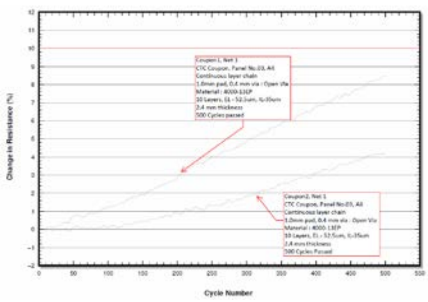
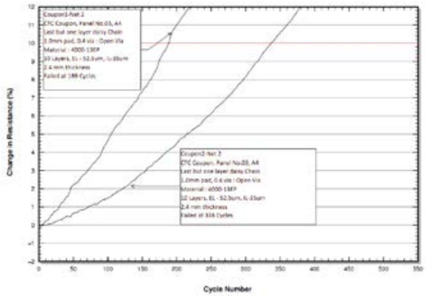


Figure 8: Resistance Variation in last but one layer daisy chain



Coupon 1&2 Net1 (Figure 7) resistance variation was within 10% for 500 thermal cycles. Whereas Coupon 1&2 Net2 (Figure 8) resistance variation was above 10% at 189 and 338 cycles. This indicate that last but one layer chain is more effective as compared to continuous daisy chain.

Micro Section Results Analysis

Micro section analysis results of 2.4 mm thick, 10 layer PCB with 0.4mm open via is shown below.

Figure 9: Micro section of 0.4 mm via after three solder dips

Microsection test result is satisfactory. Coupons/PCB have passed all the tests listed in Table 2 whereas HATS coupon from the same panel has shown high slope in resistance plot. Comparing the results of micro section analysis and HATS testing, it is inferred that HATS testing is more effective. Based on the test results, effectiveness of each test method is compared in Table 4.

Table 4. Comparison of test methods

Sl No.	Test description	Test specimen	Strengths & Weaknesses
1	ISRO-PAX-304 Acceptance tests	Actual board plus Coupons	Strengths Continuity, cross continuity and isolation, conductor peel strength, Barrel integrity Weaknesses Reflow soldering conditions are not simulated. Does not provide relative reliability
2	Modified HATS Testing	Modified HATS coupon	Strengths Reflow soldering conditions are simulated. Comparison of resistance plot slope provide relative reliability. If coupons are tested until failure, it is possible to establish margin Weaknesses Actual board is not tested. Measurement of dielectric thickness, inner layer copper thickness are not feasible.

VI. CONCLUSION

Acceptance testing, micro section analysis and HATS testing conducted on PCBs/Coupons indicate that coupons have passed typical acceptance testing listed in ISRO-PAX-304. However, coupon failed to meet 500 HATS thermal cycle requirements when via structure is using last but one layer daisy chain. Last but one layer daisy chain is more effective in HATS coupon structure.

Thermal shock cycling test with continuous resistance monitoring on last but one layer daisy chain structure could effectively assess the barrel integrity in lesser number of thermal cycles as compared to continuous daisy chains. We can also test multiple coupons at a time and compare the number of cycles to fail for assessing the relative reliability of PCBs from different vendors/manufacturing facilities. Comparison of slope of the resistance plots or cycle to fail can be used for assessing the relative reliability of PCBs.

When via dimensions are very small, micro section analysis technique is reaching its limits of assessing the barrel integrity. Introduction of HATS testing on coupon therefore becomes essential to assess the reliability of the PCB with very fine vias (where difficulty factor > 10). The HATS testing is not an alternate but the extended test method to assess the plated through hole integrity specifically when the PCBs have smaller vias and intended for reflow soldering process at assembly stage.

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Multilayer Ceramic Chip Capacitor Stacking & Soldering Using Reflow Process

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***Abstract* - Multilayer Ceramic Chip Capacitors of X7R type are extensively used in onboard electronic assemblies. Their smaller size, higher temperature stability and ability to operate within wide temperature range of -55 °C to +125 °C make them as a choice for use in miniaturized DC-DC converters. However, DC-DC converters require still higher capacitance value than what is available with single capacitor. This higher value is obtained by stacking the capacitors one over the another in parallel combination and soldering the end caps such that it becomes a single unit. Manual soldering process was used till recently in ISAC, whereas the capacitor manufacturers recommend reflow/wave soldering. Stacked MLCCs (Multi-Layer Ceramic Chip Capacitor) showed crack induced failures even after conduct of screening tests subsequent to manual soldering process.**

This paper briefly describes the existing manual stacking & soldering process, anomalies noticed at various realization stages, new reflow process developed, qualification test results and summarize the advantages. The new process uses the convection mode of heat transfer for the soldering operation and it pre-heat the assembly so that the thermal stress is almost fully eliminated. Since the process is semi-automated, it saves time, improve productivity, repeatability and reliability.

I. INTRODUCTION

The need for low feature size, high capacitance and high temperature stability coupled with high performance led to the use of MLCCs in stacked form in DC-DC converters at ISAC.

Stacked Capacitors were first introduced into onboard assemblies a few years back at ISAC to meet higher capacitance value requirement, wherein the manual soldering process was used for stacking and soldering operations. Capacitor manufacturers have specifically mentioned in data sheets that these devices are intended for reflow/wave soldering only and if manual soldering is essential, soldering iron tip shall not touch the capacitor metallization. However, stacking of capacitor using manual soldering process invariably require soldering iron tip to touch the capacitor metallization. Therefore, manually stacked/soldered MLCCs (Multilayer Ceramic Chip Capacitor) at ISAC had large number of crack related failures even though screening tests were conducted after manual soldering process before soldering onto the PCB. Failure analysis reports also confirmed that the cause of the failures were due to thermal stresses within the component body resulting from the manual soldering process. Hence, an alternate soldering process using reflow technique was developed and qualified.

This paper summarizes the limitations of manual stacking and soldering process currently used at ISAC, details of the new reflow soldering process for stacking & soldering operations and results of process qualification tests conducted.

II. MANUAL METHOD OF MLCC STACKING & SOLDERING

Manual MLCC stacking and soldering is process [1] is listed in Figure 1.

Following are the precautions to be taken.

1. Ensure that the Value, voltage, tolerance, make, case style, thermal coefficient etc., shall be same for all components in any given stack.
2. Sorting, kitting, traceability records entry operation shall be done at appropriate stages.
3. Devices shall be free from visual damages like chip off, corrosion, flaking, discoloration.
4. Soldering time shall be limited to 5 seconds and avoid touch ups at end caps.
5. Sn63 solder shall be used.

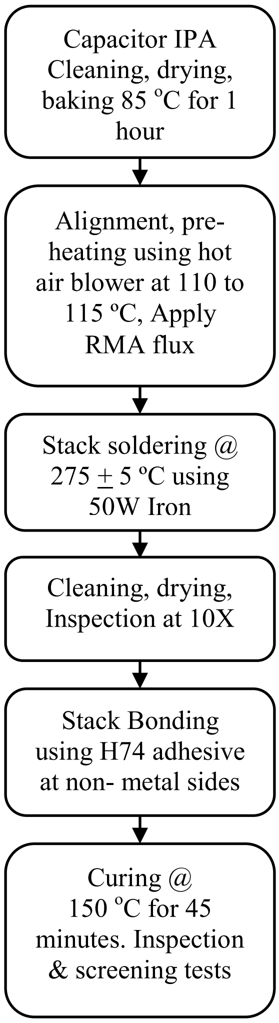

Figure 1: Flow chart for Manual stacking process

Stacked and soldered capacitor is further screened in-house by measuring pre and post capacitance value and Insulation resistance at rated voltage after subjecting the stacks for 20 thermal cycles from -55 oC to +125 oC, 15 minutes dwell at each temperature peak and 5 minutes dwell at ambient & transition is immediate (Refer Figure 2).

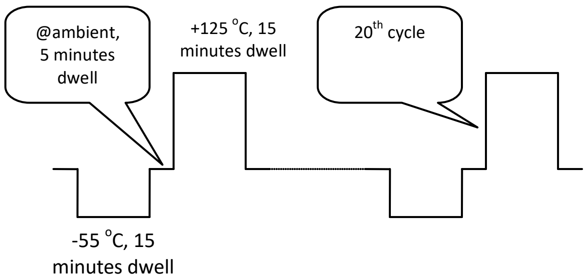

Figure 2: Thermal cycling profile of stacked capacitors

Number of capacitors failed during screening tests is almost zero.

Stacked capacitors after the screening are soldered onto the PCB using standard pre-heating process used for other ceramic chip capacitors as below:

Manual soldering of MLCC stacks on to the PCBs[1] is listed in Figure 3.

Following precautions shall be taken while manual soldering of capacitor stacks

1. Ensure traceability is not lost during pre-heating and soldering.
2. Do not place the capacitors on the hot plate when it is hot.
3. Soldering Time shall be limited to 3 s.
4. Sn63 solder shall be used.
5. Avoid the solder joint touch up to improve the solder joint quality. If rework is essential opt for replacing the capacitor with a n ew one.
6. Apart from regular mounting & soldering inspection, the devices are inspected for crack and discoloration also.

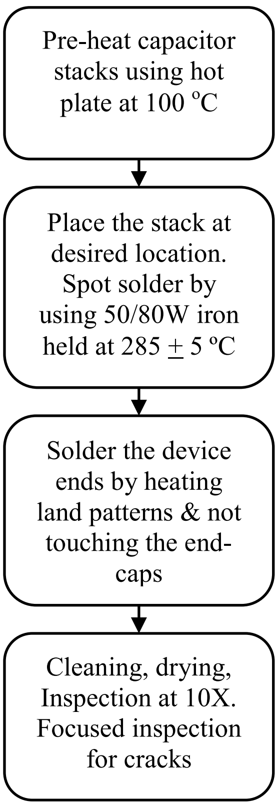

Figure 3: Flow chart for stacked capacitor soldering process by manual method

Discussions on Manual Stacking & Soldering

Since the soldering iron bit set at 280 °C is directly touching the capacitor metallization during the stack soldering, the delta temperature appearing on the capacitor body would be about 160 °C to 170 °C (stack soldering temperature minus pre-heating temperature). This may result in internal cracks and external cracks; internal cracks may develop & appear to external surface at later stages of realization/testing.

It is noted from the datasheet/brochures that temperature gradient allowed for MLCC capacitor vary from 60 °C to 120 °C depending on the make/type used. Since manual soldering process is used for mounting and soldering the stacked capacitor, bottom most capacitor in the stack will undergo thermal shock at two occasions.

Short mode failures were observed at various stages like assembly, testing, thermal cycling etc., due to body crack of capacitors located at bottom, middle and top positions of the stack; number of failures at bottom capacitor being more compared to that of middle or top. Also, FA report indicated that the reason for crack is thermal stress related. This has necessitated the process review.

III. MANUAL SOLDERING VS. REFLOW SOLDERING

Manual soldering process uses soldering iron with a controlled heat source. The iron is kept at a much higher temperature than the melting temperature of the solder. This higher temperature is used to force rapid heating. The set temperature and duration of soldering depend on the operator and the heating capability of the soldering iron. During the stack soldering process, the soldering iron is directly applied on the capacitor end caps which immediately transfer the heat to the intimate layer of the ceramic body, but within the ceramic the heat conduction is not as fast resulting in high thermal gradient/shock. For soldering of capacitors to PCB pads, the operator needs to move the soldering iron bit over the pad for which enough space will not be available in most cases. Hence, there is always a chance for the bit to touch with the end cap of the capacitor which again results in thermal shock to the device.

When it comes to reflow, the mode of heat transfer is not by conduction but by convection. The pre-heating and soldering operations are done using suitable thermal profile. Here, the soldering temperature is very benign and never exceeds 240 °C. Another important point is that the entire device body is heated up together without any temperature gradient within the device body. As a result, there are no chances of having thermal shock.

Since the introduction of reflow soldering process[2] for onboard assemblies at ISAC, around 15000 plus surface mount chip capacitors were soldered and as of now no crack related anomalies are reported. This input has become very handy and useful for the developing the reflow soldering process for stacking/soldering MLCC.

IV. MLCC STACKING & SOLDERING BY REFLOW METHOD

In this case, the individual capacitors are placed one over the another into a stack as per the component list and the end caps are reflow soldered; the stacks are then placed on the respective locations on the PCB along with other SMDs and reflow soldered to the PCB. The Operating Procedure (QOPP-C0016A09)[3] employed for stacking & soldering is as below:

1. Ensure that the Value, voltage, tolerance, make, case style, thermal coefficient etc., shall be same for all components in any given stack and shall be as per the details in component list.
2. Place capacitors one over another as shown in Figure 4.

Figure 4: Stacking of Capacitor one over another

3. Enter capacitor reference designator on the MDB slips to establish traceability.
4. Wrap Kapton tape of suitable width on non-endcap sides of the capacitor stack as shown in Figure 5.
5. Dot mark indicate the location of tape overlap and direction of the placement (i.e. the dot mark shall face us)

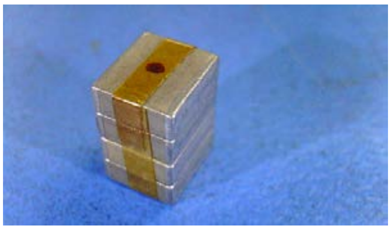

Figure 5: Taping of Stack

6. Straighten/Align the taped capacitor stack using the jig as shown in Figure 6.

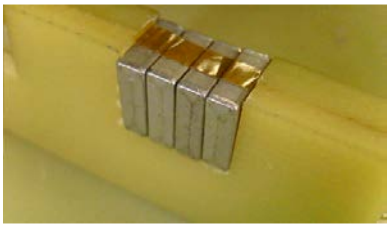

Figure 6: Aligning of stack using Jig

7. Apply a thin layer of properly stirred & prepared solder paste (Sn63, type 3 or 4, with RMA flux) on the top surfaces of the metal terminations/end cap of capacitors preferably using tooth pick stick (Refer Figure 7).

Figure 7: Capacitor stack applied with solder paste

8. Take out the stack from the jig after solder paste application; ensure that the applied solder paste is not disturbed during the process.
9. Place the capacitor stack at the respective locations on the PCB (which is solder paste screen printed), preferably after completing the placement of other SMD components in the card (Refer Figure 8).

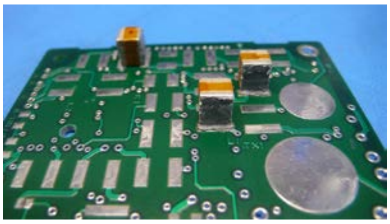

Figure 8: Capacitor stack placed on the PCB

10. Subject it for reflow soldering (Refer Figure 9) using approved reflow profile.

Figure 9: Reflow Soldering of assembly

11. Clean the assembly using IPA/SM110 as applicable using standard cleaning practiced followed at SMT line.
12. If required, ultrasonic cleaning process shall be employed to remove solder balls, if any found in the stacks.
13. Remove the Kapton tape using surgical knife, IPA and tweezers. Care shall be taken during kapton tape removal and ensure that there will not be any crack or damage to the capacitors.

14. Dry the card with clean air jet and continue further fabrication activities as applicable. Ensure that there are no residues of kapton tape adhesive material remaining on the capacitors.
15. During polymer activities, the stacked capacitors shall be staked at non soldered sides using scotch weld 2216, conformal coated using CONAP-CE1155 and potted using RTV3145.

V. MLCC STACKING BY REFLOW METHOD

In situations where already soldered stacks on the PCBs need to be replaced or if any of the capacitor stack is test selectable, separately reflow soldered stack units are to be used. The Operating Procedure (QOPP-C0016A10)[4] employed for this process is as given below:

1. Ensure value, voltage, tolerance, make, case style, thermal coefficient shall be same for component in same stack.
2. Place component one over another as Enter capacitor reference designator on the MDB slips/folder to establish traceability.
3. Wrap kapton tape on non-leaded sides of the non-soldered stack as shown in Figure 5.
4. Place the non-soldered stacked capacitor on the jig vertically and straighten/align all capacitors in the jig as shown in Figure 6.
5. Apply a thin layer of properly stirred & prepared solder paste (Sn63, type 3 or 4, with RMA flux) on the top surfaces of the metal terminations/end cap of capacitors preferably using tooth pick stick.
6. Keeping the stacks in the jig, subject it for reflow soldering (Refer Figure 10) using approved reflow profile and oven.

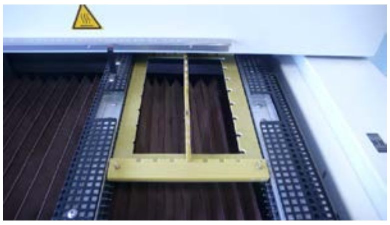

Figure 10: MLCC Stack Reflow Soldering

7. Clean the assembly using IPA/SM110 as applicable using standard cleaning practiced followed at SMT line.
8. If required, clean the assembly using standard ultrasonic cleaning method.
9. Remove the kapton tape using surgical knife, IPA and tweezers. Care shall be taken during kapton tape removal to ensure that there will not be any crack or damage to the capacitors (Refer Figure 11).

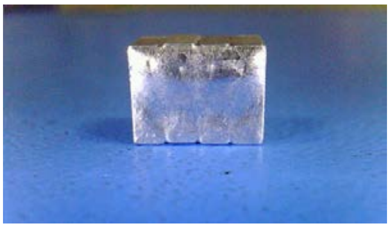

Figure 11: Reflow Soldered stack

10. Dry the stack with clean air jet and continue further fabrication activities as applicable.

VI. SOLDERING OF MLCC STACK UNITS WITH PCB USING MANUAL METHOD

In case of already soldered stacks on the PCBs need to be replaced or if any of the capacitor stack is test selectable, separately reflow soldered stack units are to be manually soldered on to PCBs. The Operating Procedure (QOPP-C0016A11)[5] employed for this process is as given below:

1. Use smart tweezers to confirm the value of the stack (Refer Figure 12). Ensure that there are no damage to the capacitors during handling with smart tweezers.

Figure 12: Value measurement using smart tweezers

2. Sort out the identical value stacked capacitors and place them on the hot plate (Refer Figure 13) when the plate is in ambient temperature. Do not place the capacitors on the hot plate which is already hot.

Figure 13: Usage of hot plate & Hot air bath

3. Set the hot plate temperature to 100-120°C and switch ON. Ensure that it has reached the set temperature.
4. After set temperature is reached wait for 5-10 minutes. Capacitors have to be placed on the hot plate prior to switch of ON the hot plate. Maximum number of capacitors placed on hot plate shall be limited to 20 No's of stack and time shall be limited to 3 hours.

5. Parallel to Sl. No.3, Set the hot air bath temperature to 95-100 °C and place the board to be soldered on the PCB stand.
6. Pre-heat the board to ~100 °C for ~ 5 to 10 minutes using the hot air bath.
7. Pick & place the pre-heated stacked capacitor unit on to the required location on the PCB using a ceramic tweezers.
8. Soldering iron wattage shall be 50W/80W or less and temperature shall be 280 °C. Soldering time shall be as short as possible (~3 seconds). Care shall be taken not to touch the soldering iron tip with the component body/end cap during mounting/soldering. Pre-heating the device to 100 °C will reduce the delta temperature and hence thermal stresses.
9. Spot solder one side of the capacitor stack as quickly as possible (Refer Figure 14). Capacitor stack mounting and soldering to be carried out at a single stretch (no mounting inspection prior to soldering).

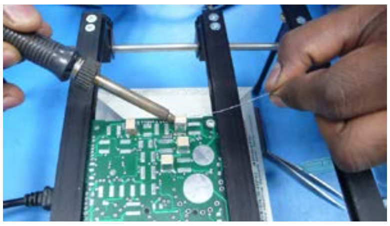

Figure 14: Manual soldering of stack unit

10. Heat the land of non-spot soldered side of capacitor stack using soldering iron without touching the end cap. Place the solder wire and drag it during heating process to get completely wetted solder-joint. Repeat the soldering process for the spot soldered end and complete the soldering process. Avoid solder joint touch up to improve the solder joint quality. If essential, opt for replacing the capacitor stack with a new one.

VII. PROCESS QUALIFICATION TESTS

ISRO-PAX-300[6] is used as reference document for establishing accept/reject criteria of solder joint in onboard assemblies. ESA specification ECSS-Q-ST-70-08C [7] and ECSS-Q-ST-70-38C[8] are generally used for the process qualification of new assembly techniques intended for onboard application. Following are the tests conducted as part of process qualification tests.

1. Visual inspection and performance verification
2. Vibration testing
3. Visual inspection and performance verification after vibration tests.
4. Thermal cycling – 500 cycles.
5. Visual inspection and performance verification followed
6. Micro-sectioning analysis

Samples prepared by direct reflow soldering process and manually soldered capacitors which were stacked using reflow process were subjected for process qualification tests listed above and results were satisfactory.

VIII. CONCLUSION

Stacking process using manual method and reflow method are described above in detail. Deficiencies in the manual soldering process are brought out and reflow soldering process has addressed those deficiencies. There were no crack related failures noticed on chip capacitors soldered using reflow method. Considering the above, capacitors stacked and soldered using reflow process will be free from crack related failures. In case, if direct reflow soldering is not feasible, an alternate process for making separate stack units by reflow method and further soldering the stack units with PCB by manual method is also discussed. Assemblies fabricated using the new processes have successfully undergone process qualification tests listed in ECSS-Q-ST-70-08C and ECSS-Q-ST-70-38C.

ACKNOWLEDGMENT

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Via Filling for Improved PTH Reliablity in Printed Circuit Boards

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***Abstract* - Introduction of fine pitch, high pin count devices in onboard electronic hardware necessitated use of finer line width, spacing, smaller via, higher layer count Printed Circuit Boards. Reducing the size of the plated through via is one of the approaches to increase the interconnect density in the Printed Circuit Board (PCB). However, the integrity of via holes plays a key role in determining the reliability of the Printed Wiring Assembly (PWA). Since the onboard PCBs are expected to operate in the vacuum environment, it is necessary to fill via to avoid entrapment of air and other contamination during the PCB wiring. This risk further escalates when the devices like Ceramic Quad Flat Packs (CQFPs) are to be mounted using thermal interface material such as Chotherm which will block via from one side and therefore act like cavities for trapping the contamination during assembly operations. Manual filling of smaller via using solder & soldering iron is prone for development of measling in PCB laminate and therefore not reliable when large number of via are present in the PCB. Use of filled via PCB is one of the suitable alternates to overcome the above issues.**

In this paper the realization of epoxy filled Plated Through Hole (PTH) followed by copper cap plating is described. Design rules used for typical 14 layers, filled via PCB design, Layer stack details, reference to the accept/reject criterions etc. are discussed. In order to make relative reliability assessment, Highly Accelerated Thermal Shock Cycling (HATS) test is conducted on via structures made by open via and filled via daisy chains. It is observed that, open via structures are showing higher slope in "resistance .vs. number of HATS cycle" plot as compared to filled via structures. This is attributed to the additional support provided by highly stable filler materials that restrict the thermo-mechanical deformation of plated copper throughout the barrel leading to firm contact between plated barrel copper to inner layer copper. Unfilled via have more degree of freedom and hence will accumulate higher plastic strain in every cycle, which leads to increase in resistance and fail at less number of thermal fatigues.

Keywords- Filled Plated Through Vias, Thermo-mechanical stress tests, Accelerated Life Testing, (HATS)Highly Accelerated Thermal Shock Test, Printed Circuit Boards, Reliability

I. INTRODUCTION

A Printed Circuit Board (PCB), is used to mechanically support and electrically connect electronic components using conductive pathways, tracks or signal traces etched from copper sheets laminated onto a non-conductive substrate. It is also referred to as printed wiring board (PWB). Most of the PCBs used for spacecraft applications are made of FR4 laminate material and applied with solder mask on bare copper to avoid the corrosion of copper conductors and also to avoid solder bridging during assembly soldering processes.

Introduction of fine pitch, high pin count devices in onboard electronic hardware necessitated use of finer line width, spacing, smaller vias, and higher layer count Printed Circuit Boards. Traces or tracks on a layer is intended for intra layer interconnections and plated through holes (PTH) are intended for inter layer interconnections

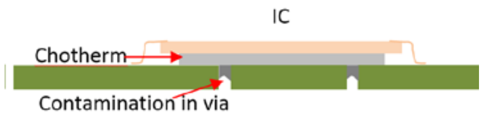
For PTH, additional steps of electroless deposition are done after the holes are drilled, then copper is electroplated to build up the thickness.

Through hole vias are the most common type of vias used in onboard PCBs. Standard dimensions of through hole via structure is 0.8 mm on a 1.5 mm pad on ~2.4 mm thick PCBs. However, in the recent past, requirement of higher interconnection density necessitated reduced via sizes to 0.4 mm on 1.0 mm pad on ~2.4 mm PCBs. This reduction in via dimension on reduced pad size has introduced following constraints on fabrication and assembly.

1. Increased registration requirements to maintain annular ring
2. Tighter drilling and plating process parameter controls to maintain the barrel quality and uniformity of plating across the barrel
3. Increased difficulty of filling the holes by hand soldering method and time consuming.
4. Filling of vias by reflow soldering method was tried and not successful.

Recently, thermal interface requirement below the CQFP devices necessitated the use of chotherm below the ICs which is resting on the PCB surface. This will cover the vias below the devices while the bottom side of the vias will be open to trap the flux and other cleaning solvents. In order to avoid the possibility of low resistance path development below the chotherm, these vias are masked using solder mask. H owever, it is noticed that this masking is not 100% effective across the barrel height. Exposure of copper in the masked barrel make the vias more sensitive to contamination related failures.

Figure 1: Pictorial view of contamination trap in the via when blocked by chotherm



A. Via Fill Methods

Generally molten solder is used in filling PTHs, but filling small PTHs pose measling problem on the laminates when the holes are at close proximity [1]. Popular techniques to plug the vias using suitable pastes are screen-printing, stencil printing and roller coating [2], [3]. In screen and stencil printing, paste is pushed inside the vias using squeeze blade and filled paste is then cured. Due to the mesh structure in the screen, it is difficult to plug the small diameter vias. In case of stencil printing method using photo-chemically etched and laser-ablated stencils, due to low paste transfer efficiency, voids get incorporated in the vias. Though the methods such as electroforming and photo-defined electrically assisted etching are explored in the literature, to achieve optimum paste transfer efficiency, the applications to fill the vias using these stencils are still debatable due to their higher thickness [4], [5]. In roller coating, though the paste filling is a mass process, due to complexity and cumbersome procedure it is not considered as the best industrial practice.

B. Via Fill Materials

There are several filling materials, either conductive or non-conductive pastes, are known to plug the through hole vias. Liquid Photo Imagable (LPI) ink typically with 60 to 70% solid contents used as filling material has been reported. However during curing process, evaporation of solvent leads to shrinkage of plug, which results in the gap between hole wall barrel and filled material. Though the LPI filling is partly successful in industry, it is not a suitable solution for growing interconnection density demand, especially for space electronics where reliability is the major criteria.

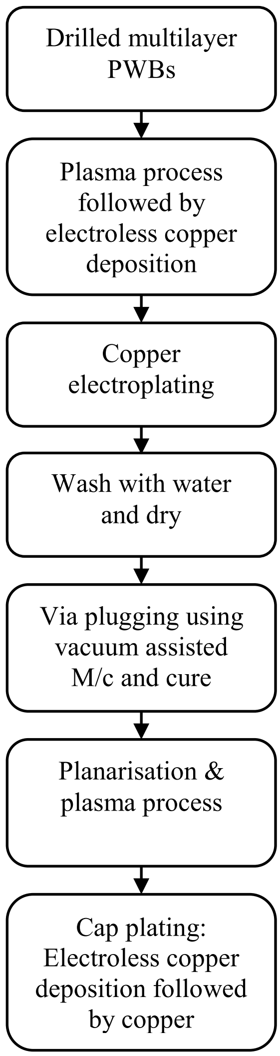
Recently, to overcome the flux residue entrapment inside the fine vias during the assembly of fine pitch devices, silicone based RTV compound-filling technique using photo-defined stencil method is proposed [6]. However, RTV filled via PCBs are not suitable for reflow soldering operations.

In our study we have used modified epoxy dielectric paste as filling material and vacuum assisted equipment to plug inside plated through holes [7]. After paste curing filled vias are copper plated from both sides.

II. EXPERIMENTAL METHODOLOGY

In this study, a 14 layer rigid Multilayer Printed Wiring Board [MLBs] was constructed using high Tg glass epoxy copper clad laminate [Source: Park Nelco, 4000-13-EP,Tg 210 °C,] as per standard fabrication process. Test coupons comprising 0.4 mm via on 1.0 mm circular pads connected in daisy chain with one ounce copper were laminated at a temperature of 220 °C, pressure 450 bar with curing time of 90 minutes in vacuum assisted press. Total thickness of the pressed laminate was 2.2 ± 0.15 mm. Laminate was baked in oven at 120 °C for one hour before drilling. Drilled panel was cleaned in jet water spray and dried at 120 °C for ten minutes. To remove dirt inside the drilled hole, panel was degreased in ultrasonic tank containing 1, 1, 2 trichloroethylene for three minutes and plasma process was done. To remove debris inside the drilled hole, panel was degreased in ultrasonic tank containing 1, 1, 2 trichloroethylene for three minutes followed by mechanical scrubbing using 320 grit roller.

Figure 2: Process Flow For Via Filling



Finally laminate was kept in air circulated hot air oven at 140 °C for half an hour. Panel was dried and fabricated as per the standard fabrication method. Brief description of important process flow steps of standard fabrication is given in Figure 2

A. Metallisation of plasma trated drilled vias

After the plasma de-smearing and etch back process, panel was cleaned with 1,1,2 Trichloroethylene for three minutes with gentle shaking and dried in air circulated oven at 100 °C for ten minutes. To metallize the drilled holes, low build electroless copper plating (Source: Rohm and Hass Plated Through Hole chemistry) was used as seed layer and to build copper thickness up to 35 microns inside the PTHs and acid copper electroplating technique (Source: MacDermid Electroplating chemistry) was used. Panel was cut into two specimens, each contains five test coupons

B. Via filling and cap plating process

One set of the specimens was subjected to via filling process. In this study, modified epoxy based paste [Source: Taiyo Make THP100 DH] was used as filling material and automatic vacuum assisted via filling

equipment [Source: ITC-Intercircuits, THP-3] is used for filling the holes with paste. Filling process and planarisation parameters as indicated in the Table 1. Panel was kept in air circulated oven at 150 ºC for one hour to cure the filled paste inside the plated through vias. Automatic planariser machine [Wise make] used to remove the excess of protruded cured paste from the vias.

Table 1. Via Filling & Planarization Process Parameters

Parameter	Value
Front pressure	0.5 bar
Rear pressure3	2.5 bar
Filling speed	180 mm/minute
Squeeze pressure	0.5 bar
Planarisation pressure	2 kW at 30%
Conveyor speed	0.5 mm/minute

After the planarisation panel was washed in water, dried and subjected to standard plasma process. Electroless copper plating followed by copper electroplating was carried out to build copper thickness of 35 microns across the panel surface.

Panels were further solder masked and subjected for Hot Air Solder Levelling Process which are common for standard PCBs. **Figure 3** (right) shows the filled vias with electroplated copper cap.

C. Qualification, Accepatnce & Reliability Testing Of Coupons

Specimens have successfully passed the qualification testing listed in ISRO-PAX-304[8]. Since tests necessary for assessing the ability of the PCB to undergo repeated reflow cycles is not listed in ISRO-PAX-304, specimen were subjected for six reflow cycles followed by visual inspection, continuity and isolation checks. Also, for establishing the relative reliability between filled and unfilled vias, coupons were subjected to thermo mechanical reliability testing.

The thermo mechanical reliability of copper plated through holes (PTH) in printed circuit boards is normally determined by different tests e.g. thermal cycle test (TCT), interconnect stress test (1ST) or highly accelerated thermal shock (HATS)[9]. During these tests the plated copper is exposed to stresses and strains which are below the tensile strength and the fracture strain, respectively, which leads to a strength-dependent fatigue failure mechanism. We have used Highly Accelerated Thermal Shock Cycling tests to compare the results. In this test method, the chamber temperature varies from -65 °C to +135 °C during the cycling. Each coupon with daisy-chain nets, is loaded into the chamber with necessary interconnections to conduct 4 wire resistance measurements at every second. Precision electrical resistances of each of the nets is monitored during thermal cycling, providing data that shows the degradation of the nets during the test.

III. Results and discussions

Micrographs at **Figure 3** are the optical photographs [Source: Leica DM5000 Metallurgical] of 0.4 mm plated copper vias with and without epoxy filled. It clearly shows that paste is filled uniformly inside the PTHs and there is no crack in the filled epoxy bulk and no damage to the hole wall copper. Since ISRO-PAX-304 does not address the requirements for filled via PCBs, accept /reject criteria listed in IPC-6012C[10] is used for qualification/acceptance tests/inspection related to filled vias.

Specimen made of filled and unfilled vias have successfully passed six solder dip cycles followed by visual inspection, continuity and isolation tests. **Figure 4** shows the micro section views of filled and unfilled vias after six solder dip cycles.

Figure 3: Micro section view of unfilled via (left) and cap plated filled via (right) after hot air solder levelling

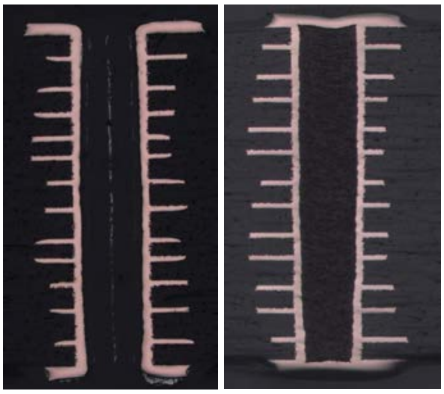
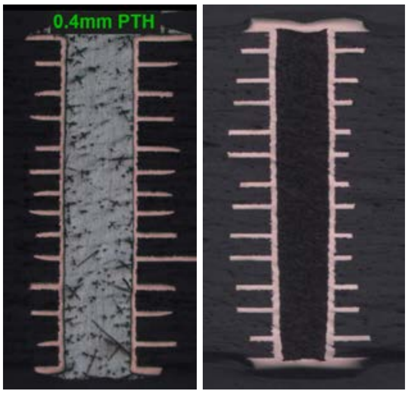


Figure 4: Micro section view of open via (left) and cap plated filled via (right) after six solder dip tests



Specimen made of filled and unfilled vias have successfully passed six reflow soldering cycles followed by visual inspection, continuity and isolation tests.

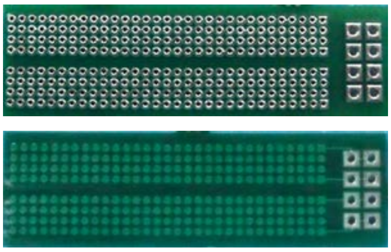
Filler material Total Mas Loss (TML) and Collected Volatile Condensable Material (CVCM) was measured

and found as 0.29% and 0.009% as against <1% and <0.1% requirement.

A. *HATS test results*

Coupons specifically made for HATS testing is subjected for 500 cycles of HATS testing.

Figure 5: HATS test coupons of filled (bottom) and unfilled (top) vias



Percentage change in resistance is referenced to the highest resistance recorded during the first cycle, and is calculated by:

$$100 * \left[1 - \frac{\text{Resistance high in cycle [i]}}{\text{Resistance high in first cycle}}\right]$$

Where 'i' is the cycle number.

This % change in resistance is plotted against the cycle's number and is shown below.

Figure 6: HATS Resistance plot of 0.4 mm filled vias coupons

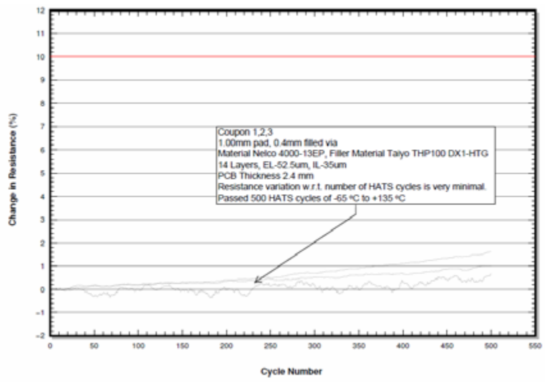
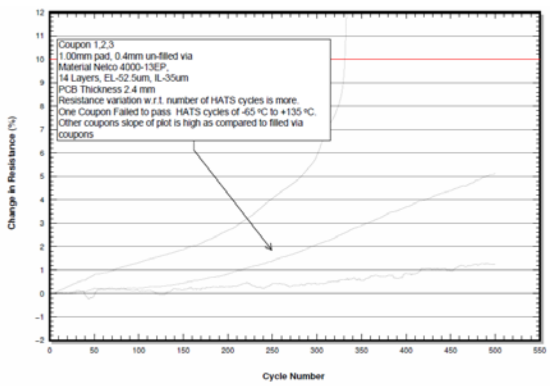


Figure 7: HATS Resistance plot of 0.4 mm unfilled vias coupons



It is evident from the plot that, tendency of increasing resistance of filled PTH is very low and there is 2% increase in the resistance at 500 numbers of thermal cycles. However in case of bare PTH, there is greater than 10% increase in resistance after 300 numbers of thermal cycles in one net and slope of other is much higher than that of filled via. This is attributed to the additional support provided by cured filled material, resulting in the reduced plastic strain of the plated copper barrel.

IV. CONCLUSION

In this paper we have studied the relative reliability of epoxy filled PTHs and bare PTHs. The thermo-mechanical stress test results reveals that there is no significant degradation of filled epoxy material and no voids and copper barrel defects in thermal cycling and thermo-vac test conditions. In addition highly accelerated stress test confirms that filled PTHs had very low increasing tendency of resistance and exhibit ~3% change in the resistance after 500 thermal cycles. However bare PTHs had greater than 10% changes in resistance. Lesser slope of filled via daisy chain is attributed to the reduced plastic deformation of plated copper in case of filled PTHs, which indicate higher reliability as compared to unfilled vias. Use of filled via PCBs will eliminate the manual solder filling time and possibility of contamination entrapment. The methodology and the material used for filling PTHs in PWBs could produce defect free PCBs consistently and passed all the necessary qualification tests listed in ISRO-PAX-304, additional multiple reflow cycles tests and HATS tests.

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Reliability Improvement Using Modified Solar Panel Fabrication Process

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***Abstract* - Over the last 40 years, Solar cells usage in ISRO spacecraft is evolved from silicon cells to multi junction solar cells and the efficiency of solar cell has improved from 13% to 30% over the same period. Different solar panel fabrication methodologies were qualified and implemented for using these cells for onboard application. However, from the introduction of multi junction solar cells, bypass diode has become an integral part of the cell to take care of the reverse voltage condition arising from the shadowing effect.**

For multi junction solar cells, new process of cell layup along with old fabrication process was tested on life cycle coupons. During different stages of process qualification, it was occasionally noticed that cells by-pass diode exhibited weld discontinuity in old and new fabrication processes during thermal cycling. Analysis was carried out to understand the observation. Two measures were adopted to resolve this issue. One is by strengthening the diode weld interface and other by modifying the cell bonding process onto the substrate. The coupons fabricated and tested with the above improvement have successfully passed the thermal cycling test. This paper details the current solar panel fabrication process, results of qualification tests wherein the marginality was noticed and process improvements made. The coupon fabricated with modifications was tested for Life cycles and has successfully passed visual, electrical, bypass diode continuity and insulation test at intervals of life cycling and after completion of life cycling.

Keywords- Solar Cells, Solar Panel Fabrication, Accelerated Life Testing, Reliability.

I. INTRODUCTION

The fabrication process of solar panels comprises of interconnecting solar cells into modules by welding, bonding the modules onto solar cell substrate with silicone adhesive and wiring the panel to draw power. [1] The process development, product realization and qualification is carried out jointly by the PSG and PMPG. Quality control team ensures that quality requirements pertaining to each of these activities are compiled at relevant stages by inspection and testing.

When a new material/process needs to be used, process qualification exercise is carried out to ensure that the process is able to produce defect free products consistently and product meets the functional requirements during the expected product life cycle with sufficient margin. Products realized through the qualified process is acceptance tested prior to use in Spacecraft.

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II. TRIPLE JUNCTION CELLS

The cell dimension of Triple junction cells procured is typically 4 x 8 cm^2. The by-pass diode is located at the cell crop corner of solar cell (Figure 1 and Figure 2). The function of the bypass diode is to protect the cell from reverse bias when the cell is shadowed.

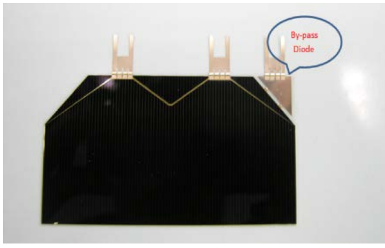

Figure 1: Triple Junction Solar Cell Front Side

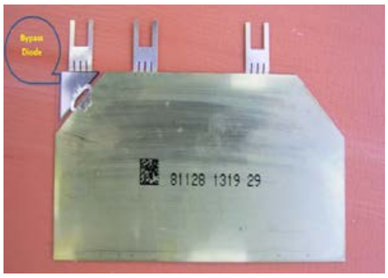

Figure 2: Triple Junction Solar Cell Rear Side

III. FABRICATION PROCESS

Fabrication of Solar panel consists of cell welding as per approved panel design drawing, bonding interconnected solar cells modules on to the Solar panel substrate and wiring of modules to form strings which in-turn connected to solar array drive slip rings through connectors.

A. *Cell Welding*

Solar cells are interconnected using parallel gap resistance welding process. Resistance welding is a type of

welding process in which coalescence is produced by the heat obtained

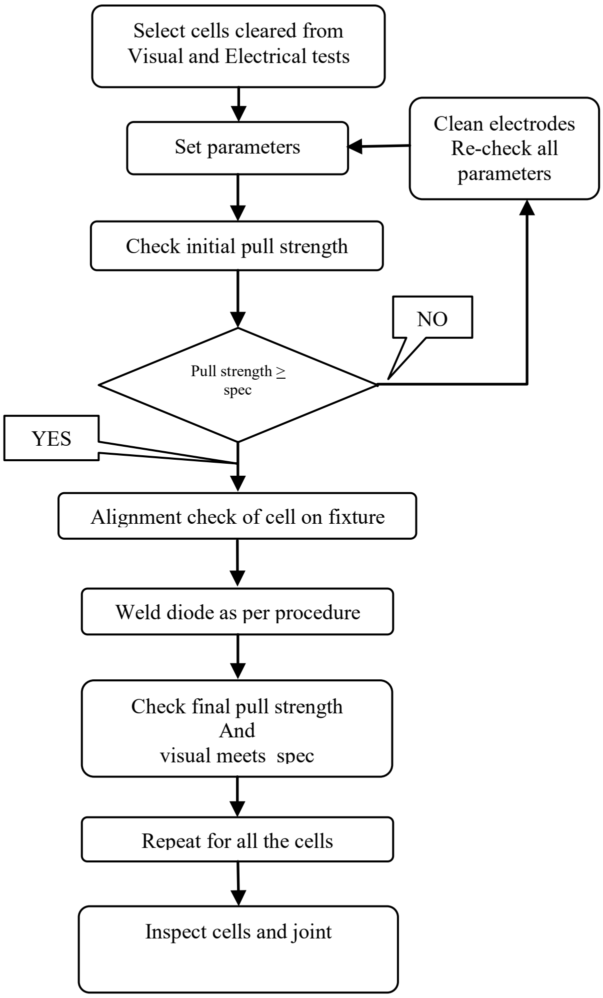

Figure 3: Solar cells weld process flow

from resistance of the work to electric current in a circuit of which the work is a part and by the application of pressure. There are at least seven important resistance-welding methods. These are flash welding, high frequency resistance welding, percussion welding, projection welding, resistance seam welding, resistance spot welding, upset welding and parallel gap resistance welding. Considering the features of solar cells parallel gap resistance welding process is employed for interconnecting solar cells. In parallel gap resistance welding heat is generated by the passage of electrical current through a resistance circuit. The force applied before, during, and after the current flow forces the heated parts together so that coalescence will occur. Pressure is required throughout the entire welding cycle to assure a continuous electrical circuit through the work.

H (heat energy in joule) = $K * I^2 * R * T$

In this formula, I = current in amperes, R is the resistance of the work in ohms, T is the time of current flow in second, and K is a constant that represents the heat losses through radiation and conduction. Welding heat is proportional to the square of the welding current. If the current is doubled, the heat generated is quadrupled. Welding heat is proportional to the total time of current flow, thus, if current is doubled, the time can be reduced considerably. The welding heat generated is directly proportional to the resistance and is related to the material being welded and the pressure applied. The heat losses should be held to a minimum. It is an advantage to shorten welding time. Mechanical pressure which forces the parts together helps refine the grain structure of the weld. Resistance welds are made very quickly; however, each process has its own time cycle. Resistance welding equipment utilizes programs for controlling current, time cycles, pressure, and movement. Considering above, welding programs for resistance welding can become quite complex and also dependency of operator skill in realizing quality weld joints is gradually reducing.

In order to ensure the quality of joints, welding machine is validated/calibrated prior to use for solar cell welding process. Welded joints are tested for their integrity by nondestructive and destructive tests. Process parameters, operator, welding machine and cell details are logged to establish traceability. After completion of cell welding process, following inspections are carried out:

- Visual inspection of cell surface for cracks or any other damages.
- Verification of weld process parameters
- Weld joint visual inspection
- Electroluminescence inspection to check for micro cracks/cracks

Cells welded are further bonded on to the solar panel substrate.

B. Bonding process

Welded cells units in sub module to module form is bonded on the solar panel substrate to form the solar panel. This layup process is generally carried out by either masking or grouting process. RTV S 691 adhesive is used for this bonding application.

a.Maksing Process

In this process, adhesive is applied by screen printing on to substrate with 40/60 mesh and 100µ thick masks. Area of adhesive application is controlled through the mask. Mask opening rules are shown in Figure 4. Shaded region in the picture is opening area of mask for RTV S 691 application. Thickness of adhesive in masking process is 100 to 150 µm.

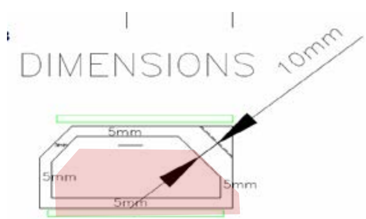

Figure 4: Mask opening rule for masking process

Area below the diode and cell edges is not applied with adhesive. This is to ensure that the inter cell and cell to diode gaps are free of adhesive and adhesive does not over flow above the active front surface of the solar cell cover glass. This process is used in almost all arrays up to the point of introduction of 70V bus in Spacecraft. When the bus voltage was increased to 70V, it became mandatory to flood the adhesive to cover the cell edges so as to minimize the risk of arcing in the plasma environment of space from developing into sustained arcing. This has necessitated a change in the solar cell bonding process and the use of grouting process for cell bonding.

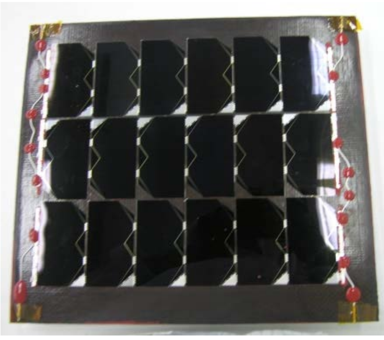

Figure 5: Coupon fabricated by masking process

b.Grouting Process

In grouting process, adhesive is screen printed on substrate using mesh and spray coated on the solar cell's bonding surface. Here the entire cell surface gets embedded in adhesive and hence reduce effectiveness of the stress relief loops and introduce additional stress on cell diode weld joints. Adhesive applied is shaded in Figure 6.

Figure 6: Adhesive application for grouting process

In this process, not only the cell bottom but also the inter cell gaps are filled with adhesives. Thickness of adhesive in grouting is 200 to 250 µm.

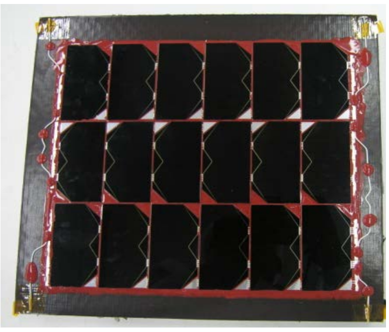

Figure 7: Coupon fabricated by grouting process

During process qualification of solar panel fabrication process utilizing Triple Junction cells, coupons were fabricated using masking and grouting processes.

Number of thermal cycles and temperature limits for generic GEO mission listed for 15 years' service life and 50% margin. This is derived from the data available from earlier similar spacecraft.

Table 1: Number of thermal cycles and limits

	No of cycles	Temperature limit
Eclipse cycles	2025	-160 °C to +100 °C
Shadow cycles	4500	-100 °C to +100 °C

This number is around 30,000 cycles for LEO missions with temperature extreme of -100 to +100 °C. There is no need for considering shadow effect for LEO missions [3].

The concept of shadow cycling has evolved based on the on orbit observations of GSAT-2/3 Spacecraft. This additional number of thermal cycles was attributed to gradually moving shadow formation on panels due to appendages of spacecraft. This phenomenon also limits the negative temperature excursions from -160 °C to -100 °C. Number of such shadow cycles per annum observed is ~200 cycles per year.

Cells in the shadow prone region of the solar array can under certain conditions, experience reverse biasing by the other cells in the same series chain which are illuminated. In this condition, bypass diode is essential to protect the cells from damage. Therefore, as a standard practice, diode continuity was monitored in situ during thermal cycling. During GEO life cycling tests, diode interconnect weld joint failures were observed in a few samples between 2025 and 2025+4500 cycles in both mask and grouting process coupons. Since the usage of grouting process is mandatory, and since failures were observed in coupons bonded using Mask process also, it was therefore necessary to adopt alternate methods for ensuring survival of the diode weld joints.

IV. BYPASS DIODE FUNCTIONS & OBSERVATIONS

Bypass diodes are silicon diodes, which are interconnected to solar cell in such a way, that diode gets forward biased when the cell is shadowed [2]. Hence, Solar cell string is protected from degrading by reverse bias. During thermal cycling of a coupon, by pass diodes continuity were checked during hot and cold cycles. Solar cells diode discontinuity was observed during thermal cycling of the coupon.

Both the process of Grouting and Mask showed discontinuity (opening of weld) of by-pass diodes, on the back side of the diode. This is due to marginality in the strength of the diode weld joints. Therefore, an approach of additional weld on back side of the bypass diode was worked out and implemented.

V. CELL WELD STRENGTHENING

Cell weld parameters

Weld Parameters were optimized and checked for visual defects and electrical parameters after welding. Solar cell diode Samples with additional weld were checked for visual, electrical, dark forward characteristics to gain confidence that the extra weld has not degraded the solar cell.

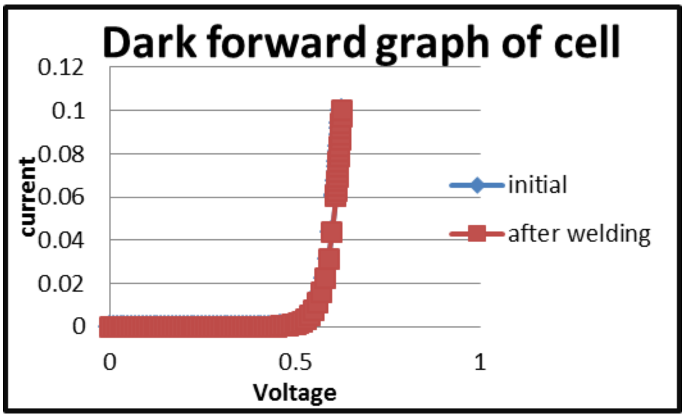

Figure 8: Forward characteristic of Solar cell

Due to the geometry of the diode interconnect, it was not possible to independently evaluate the joint strength by pull test. Further, the samples were electro luminescence (EL) tested for any micro cracks on cell surface. Weld joints were evaluated using acoustic scanning microscope to quantify the area of the weld joints and results were satisfactory. Location of additional weld is shown in Figure 8.

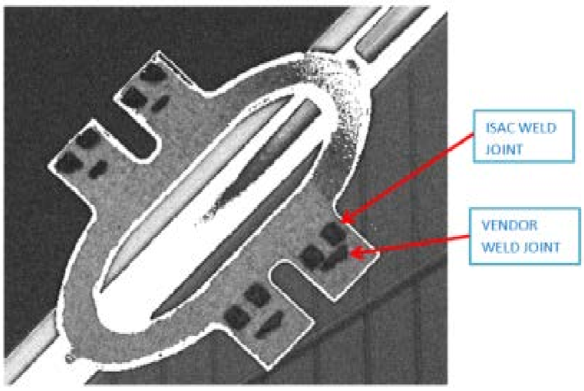

Figure 9: Scanning Acoustic Micrograph of weld joints

VI. MODIFIED CELL BONDING PROCESS

The cell bonding process was modified, restricting adhesive on the diode. Adhesive was sprayed on the substrate and to restrict the adhesive only on the cells back surface and ensure that it is free from diode interconnect surface, a mask is prepared as shown in Figure 9.

Figure 10: Cell mask for spray coating

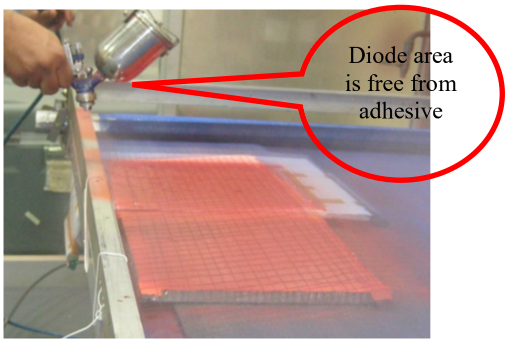

Figure 11: Spray coating of adhesive on substrate & cells

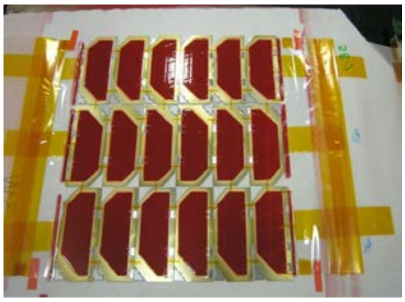

Figure 12: Spray coated adhesive cells

VII. QUALIFICATION TESTS & RESULTS

Based on the results obtained from trial samples, work instructions/ check lists were generated, accept reject criteria were established. [4]Three coupons were fabricated for life testing.

- Coupon-1 was fabricated with grouting process and without additional weld.
- Coupon-2 was fabricated with masking process and without additional weld.
- Coupon-3 was fabricated by masking process, additional weld, adhesive spray on substrate and cells.

The visual inspection, electrical evaluation, insulation resistance and by pass diode continuity checks after life cycle of coupon 3 was satisfactory.

Coupon-1 diode interconnect failure was noticed before 2025 cycles which is less than the GEO requirements. Coupon-2 diode interconnect failure was noticed between

2025 and 4500 cycles. Coupon-3 has successfully passed all the process qualification tests. Salient observations are listed in following tables.

Table 2: Coupon -3 Visual inspection report

Stages	After fabrication	After Storage and 5 TVC	After 30000 TVC
Cell cracks	Nil	Nil	Nil
End to end CG cracks	Nil	Nil	Nil
Other defects	Nil	Nil	Nil

Table 3: Coupon -3 Electrical evaluation report

Stages	Isc	% Dev	Voc	% Dev	Iop	% Dev	Vop
After fabrication	0.513	-	48.08	-	0.491	-	42.3
After Storage and 5 TVC	0.516	0.58	48.22	0.29	0.492	0.20	42.3
After 30000 TVC	0.516	0.58	48.17	0.19	0.493	0.41	42.3

Table 4: Coupon -3 Other tests report

Stages	Insulation resistance Value (Spec. >1x10⁸ Ω)	By-pass diode Continuity	EL Test
After fabrication	$2x10^9 \Omega$	Exists	No Anomalies
After Storage and 5 TVC	$2x10^9 \Omega$	Exists	No Anomalies
After 30000 TVC	$2x10^9 \Omega$	Exists	No Anomalies

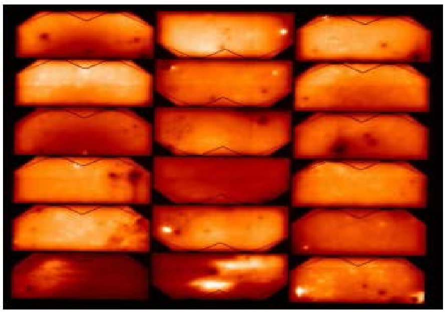

Figure 12: Coupon-3 EL Image

Figure 13: Coupon-3 Photograph

VIII. DISCUSSIONS

Coupon-1 diode interconnect failure was noticed before 2025 cycles which is less than the GEO requirements without considering shadow effect. Coupon-2 diode interconnect failure was noticed between 2025 and 4500 which is less than the GEO mission requirements including shadow effects. Coupon-3 have successfully underwent the process qualification tests and life test for LEO missions. In addition, another coupon fabricated using the grouting process with a n ew batch of solar cells from the manufacturer with improved diode interconnect welding and a Kapton tape patch over the diode joints has successfully passed the LEO life cycle test. One more coupon will be subjected for GEO also .Though the pull test results are not available, the ability of additional weld joints to withstand 30000 thermal cycles indicate that new process has improved the process and established margin over the requirements.

IX. CONCLUSION

Solar panel fabrication process being practiced at ISAC is discussed. Adequacy of strengthening of diode joints using additional welds made at ISAC is validated. This additional weld, done at ISAC and other improvements made by the cell manufacturer in the form of improved weld joints and use of Kapton patch over the diode joints have ensured that coupons fabricated using either mask or grouting process of panel fabrication successfully passed the life tests. The process improvements implemented have successfully passed the tests and are approved for use in flight solar panels.

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Elucidating the Process of Multilayer Ceramic Capacitors (MLCC) For Highly Reliable Space Applications

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Abstract—**Highly reliable applications in the space, defense and medical domains mandate extremely trustworthy passive electronic components. Multilayer Ceramic Chip Capacitor (MLCC) plays a vital role in various places in space systems ranging from launching to monitoring and communications with satellites. Manufacturing and processing conditions of MLCCs is the stepping-stone to achieve highly reliable end products to work until the end of life of a satellite. We have explained the process flows of MLCCs to achieve military or space-grade ceramic capacitors. The most important steps involved in this manufacturing process of MLCCs are batching, slurry preparation, tape casting, printing, dicing and sintering. The steps and the challenges encountered during the fabrication of highly reliable MLCCs are explained in-detail. The testing of MLCCs is also described.**

Keywords: MLCC, Multilayer ceramic capacitors, Highly Reliable

I. INTRODUCTION

As the momentum of Indian Space Mission (ISM) programs and defense equipment manufacturing are focusing towards more and more of indigenization, self-reliance for sourcing of simple passive components to complex engine and structural composites need to be addressed that how to produce with hi-reliable qualities to use in extreme environments. MLCC has found wide range of applications in electronic equipment used for data processing, automotive applications, medical instrumentation, space application devices, military systems, telecommunication equipment and other applications.

It is a paramount importance to learn and understand about the process of MLCC and its reliability to use effectively in extreme electronic applications. In order to achieve the desired high reliable properties of MLCC to use in such hostile environmental conditions, processing is a basic stepping-stone to obtain required final product.

In this article, we have discussed about the raw materials, processing flow of MLCC and its reliability.

A. Brief on Basics of Multilayer Ceramic Capacitor

A ceramic capacitor is an un-polarized fixed capacitor made up of two or more alternate layers of ceramic and metal. The ceramic material will act as a dielectric and the metal act as an electrode. Generally, the ceramic material is a para or ferroelectric materials that are modified by adding additives to achieve and meet out the desired temperature characteristics of capacitors.

B. Types of Capacitors

Based on the temperature characteristics, stability of capacitance and DF, there is two broad categories of MLCCs.

1. Class-I
   These capacitors are having very low loss and high stability of capacitance with respect to temperature in resonance circuit applications. In EIA standard, it is called as C0G or NP0, etc, and as per MIL standard, it is named as BG and BP.
2. Class-II
   These capacitors are having high volumetric efficiency with high loss and less stability with respect to temperature when compared with Type-I capacitors and are used as buffer, by-pass and coupling applications. As per EIA standard, it is named as X7R, X8R, Y5V, etc, and in MIL standard, it is called as BX and BR.

C. Design of MLCCs

Design part of MLCC is a most important foundation step. While designing of MLCC, the following things have to be considered which is based on application like commercial or hi-reliable.

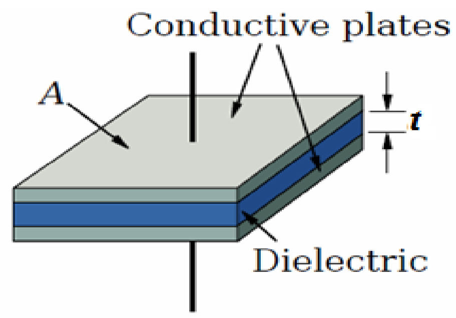
1. Selection of raw materials for fabrication
2. Electrical requirements
3. Mechanical requirement

D. Construction of Ceramic Capacitors

Construction of a simple ceramic capacitor is shown in Figure 1. Two conducting layers (Electrodes like Ag, Ni, Ag/Pd, Pt, Au) separated by a d ielectric (Ceramic formulation like X7R or X8R or BX or BR) medium form a capacitor. By way of manipulating area, thickness and dielectric constant, the required capacitance value, rated voltage is achieved for a finished capacitor.

Multilayer ceramic chip capacitor MLCC) is shown in figure 2 and 3. As the active layer thickness of dielectric

medium and area are restricted while design and fabrication, the multilayer concept is introduced to obtain large capacitance value combining with higher rated voltage. Figure 3 shows the cross sectional view of a finished MLCC where one can see the alternating electrodes with dielectric layer. Figure 4 shows different sizes of finished MLCC. The smallest MLCC available in the market is “01005” (As per EIA standard), that is, 0.4mm X 0.2mm.



$$C = \frac{KA}{t} \text{ Farad}$$

Figure 1. Basic Capacitor

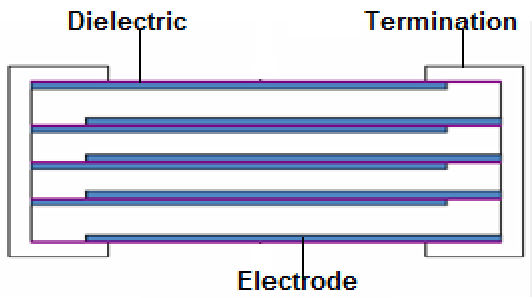
Where C is the capacitance value

K is the dielectric medium (constant)

A is the active area

t is the active layer thickness

N is the number of layers



$$C = \frac{KAN}{t} \text{ Farad}$$

Figure 2. Construction of Multilayer ceramic capacitor

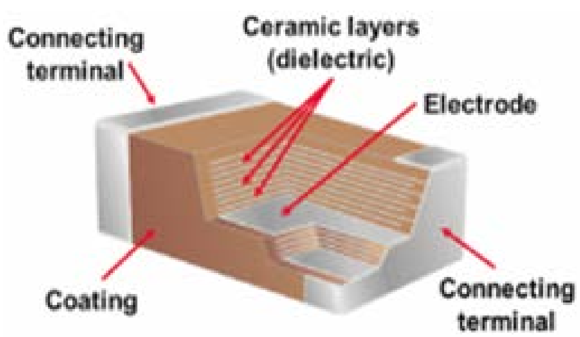


Figure 3. Architecture of MLCC

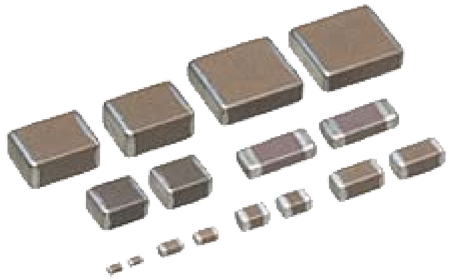


Figure 4. Finished MLCCs of different sizes

II. MANUFACTURING PROCESS STEPS OF MLCC

The manufacturing process of MLCC involves many complex steps.

- **Raw Material Selection**
  Dielectric Powder: Very fine powder of formulated oxide ceramics material, which depends on the type of MLCC. Normally the base powder is Barium Titanate.
  Electrode: This is a conducting material of type Silver or Silver-Palladium
  End Termination: Silver or Silver-Palladium, Gold or combination of these materials are used
- **Materials Mixing or Batching**
  Dielectric powder is mixed with organic binder, dispersants and solvents to produce slurry.
- **Tape Casting**:
  The slurry is poured onto a moving conveyor belt inside a drying oven, resulting in dry ceramic dielectric tape. This is then cut into square shape pieces called sheets.
- **Screen Printing and Stacking:**
  The electrode paste is made from a fine metal powder that is mixed with organic solvents yield electrode ink. The electrodes are now printed onto the ceramic dielectric sheets by means of a screen-printing process. Many such sheets are printed and stacked one over the other to create a multilayer structure.
- **Lamination:**
  Pressure is applied iso-statically to the stack to create a monolithic structure. The resulting bar is called a green ceramic bar.
- **Cutting:**
  The bar is then cut into individual separate pieces and called as ‘green’ capacitors.
- **Sintering:**
  The parts are sintered in furnace with slow moving conveyor belts. The temperature profile of the sintering process is very important to achieve the characteristics of final capacitors.
- **Termination:**

The end termination provides the first layer of electrical and mechanical connection to the capacitor. Both sides of terminals of capacitor is then dipped in silver paste and the parts are fired in furnace which gives proper strength.

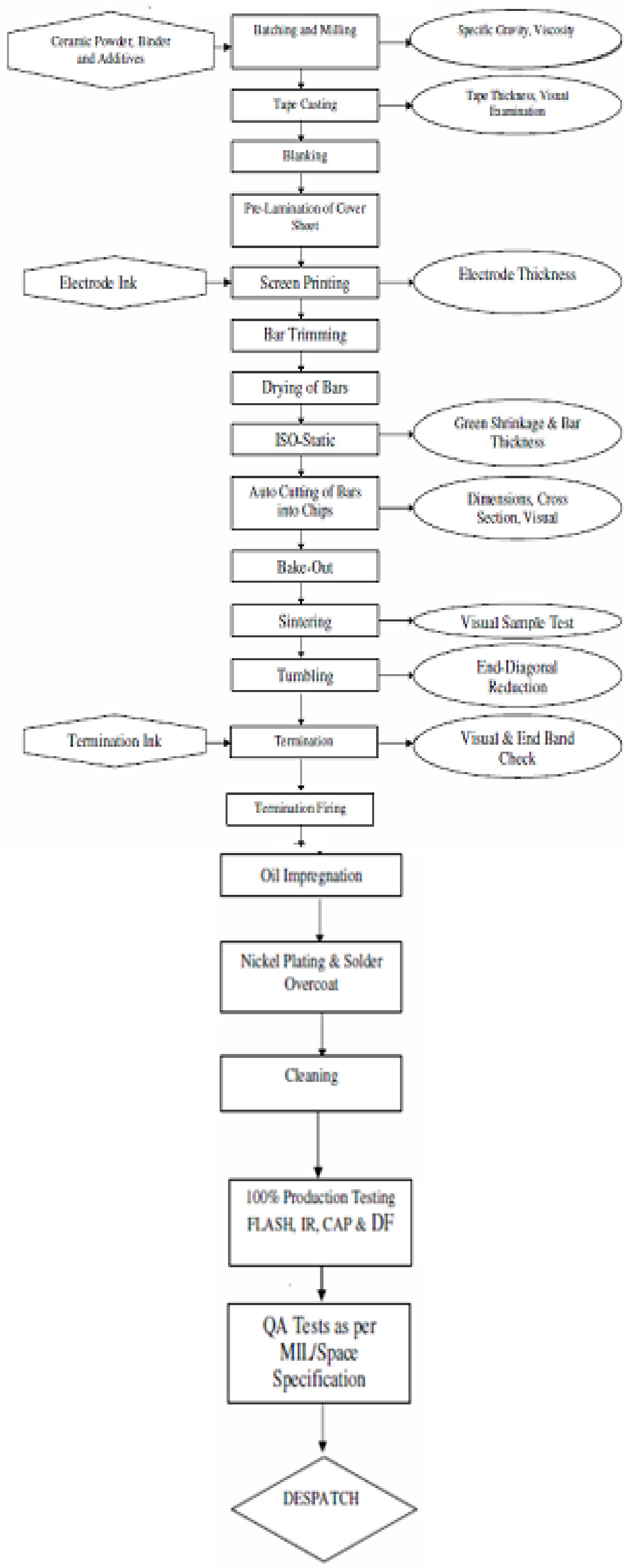


Figure 5 Process Flow Chart of MLCC

- **Plating:**
  By means of electroplating process, the silver termination is plated with a layer of nickel and then a layer of desired metal finish. The nickel is a barrier layer between the termination and the tin or solder plating. These are final finished ceramic capacitors.
- **Testing:**
  The finished parts are tested and sorted to their correct capacitance tolerances.

The required tolerance of parts will be shipped to customer either packaged on tape and reel or as bulk.

III. Defects and Failures in MLCCs

Although the reliability of MLCCs are very high in the order of decades, introduction of different types of defects either during manufacture or assembly process leads to failure. As the energy storage is large in capacitors, due to internal shorts, heat generated is enormous which leads to burning of capacitors and in some times it explodes. This causes not only the failure of capacitors, the neighboring components in the circuit board also affected and failed.

Generally, failures in MLCC do not happen on its own. Failures may arise during any of the following phases

- Design of MLCC
- Manufacture of MLCC
- Assembly on circuit board
- Testing and screening
- Packaging and storage
- Transportation
- Installation, operation and maintenance

The failure due to defects may not be possible or it is difficult to detect until later phase of life cycle. Therefore one should take utmost care during the process of above steps.

A. Types of Defects

The following are the broad classification of defects in MLCCs

1) Intrinsic defects
2) Extrinsic defects
3) Customer induced defects

1) Intrinsic Defects

The intrinsic defects are mainly introduced during manufacturing process of MLCCs, which are

- Printing defects
- Sintering cracks
- Knitline cracks
- Voids

Properly constructed MLCC is shown in the figure 6. It is seen in the structural view that the electrodes are uniformly spaced between the dielectric layers and there are no defects. Observation of continuity of electrode is also uniform and it touches the end termination to provide electrical connectivity to the outside world.

The figure 7 shows the non-uniformly printed electrode which leads to short of capacitors which is a printing defect.

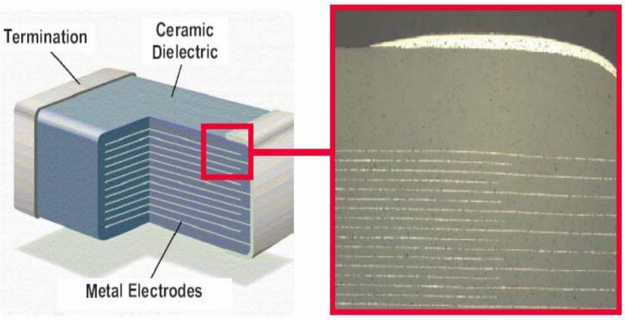


Figure 6 Cross sectional view of Printed Electrode

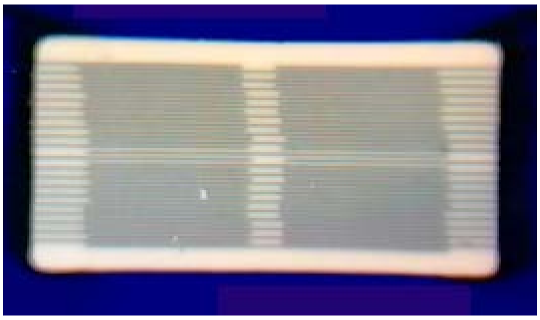


Figure 7 Cross sectional view of unevenly Printed Electrode

a) Sintering or Firing Defects

An example of firing crack is shown in figure 8. The firing crack generally starts at the edge of electrode but not always, and propagates perpendicular to the electrode.

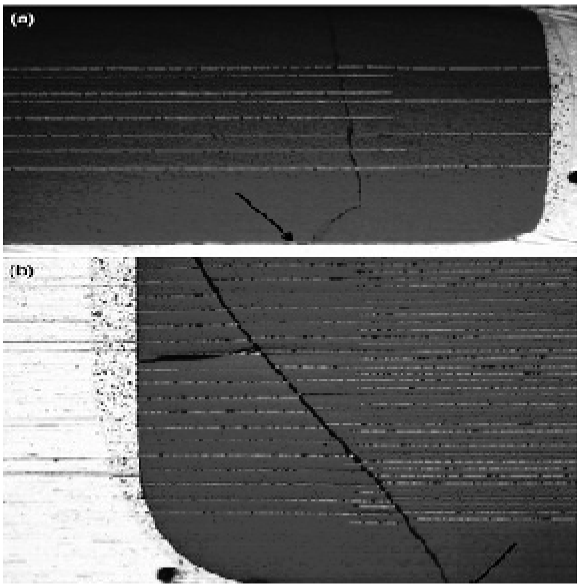


Figure 8 Thermal shock cracks in MLCC

b) Knitline Crack

An example of knitline crack is shown in figure 9. This type of crack runs parallel along with the printed electrode.

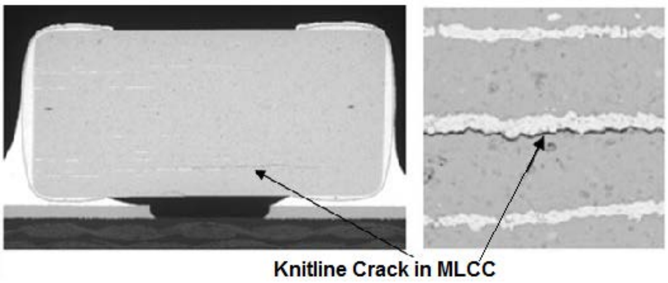


Figure 9. Knitline crack

c) Void

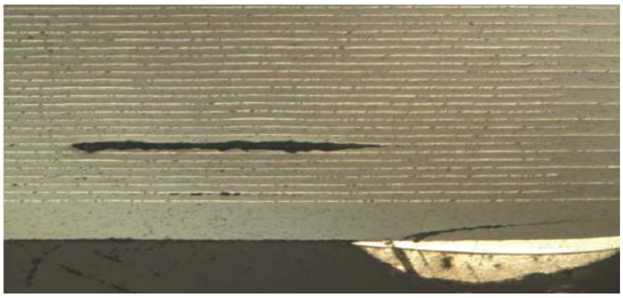


Figure 10 Presence of Void in MLCC

An example of void defect is shown in figure 10. This type of crack runs parallel along with the printed electrode. The voids are normally bridges the inter electrodes and hence creates passage path for electrical conduction, which eventually leads to fail.

2) Extrinsic Defects

The extrinsic defects are mainly introduced during assembly process of MLCCs in the application site, which are

- Handling crack
- Thermal shock cracks
- Flex cracks
- Silver migration

a) Handling Crack

The handling crack appears mainly during packing in tape and reel; and also pick and place during the assembly process. The excessive stress during these processes induces the cracks.

b) Thermal Shock Crack

The thermal shock cracks appear in MLCC due to rapid change in temperature in the process of wave, reflow and hand soldering and, during cleaning and rework. Figure 11 shows the thermal shock crack in MLCC, which is near to end termination.

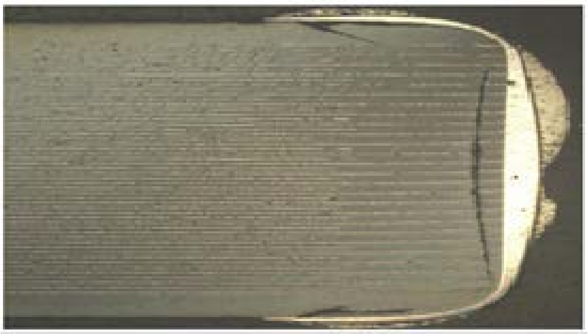


Figure 11 Micro-crack due to thermal shock in MLCC

c) Flex Crack

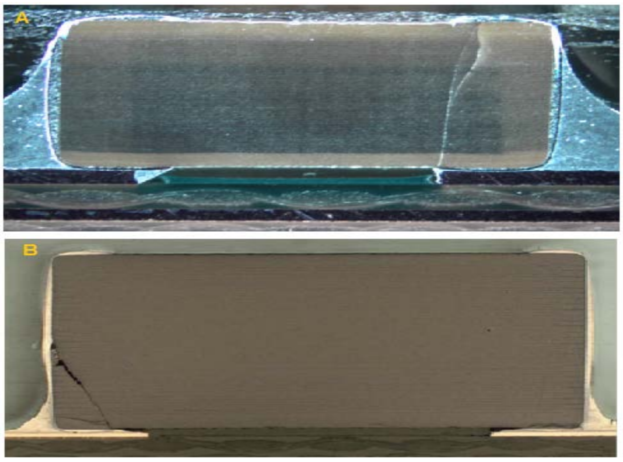


Figure 12 Flex cracks in MLCC A-Extreme and B-Corner

The flex cracks appear due to excessive usage of flex during assembly. Excessive tightening of screws and insertion of connectors, which generate stress around the place on the board eventually, induces cracks on MLCC. The figure 12 shows such type of cracks in MLCC.

IV. SCREENING OF HI-RELIABLE MLCC

Screening of capacitors is an essential step to remove defective components particularly for hi-reliable or extreme electronic applications. Generally the following sequence is used to 100% screen the hi-reliable MLCCs

- Electrical (Go-No Go)
- Thermal cycling
- Visual
- Electrical (Absolute measurement)
    - Cap, DF and IR
- Burn-in
- Electrical (Absolute measurement)
    - Cap, DF and IR
- Dielectric withstanding voltage (DWV)
- Elevated IR (sample basis)
- Solderability (sample basis)
- Terminal strength (sample basis)
- Adhesion strength (sample basis)

In order to remove the tolerances beyond required values, the Go-NoGo test greatly helps.

The thermal shock test helps to vied out the intrinsic defectives like internal micro-cracked capacitors, small void components, etc.

Physical damages like chip off, blacking on terminal edges, improperly plated capacitors, thin end bands, surface cracked chips are removed by means of visual inspection.

Pre-, and post burn-in electrical screening test paves the way to remove electrically defective components. This is the test to decide that a production lot can be allowed to pass or fail based on the desired percentage of defectives.

DWV is the test, which decides the capability of taking of electrical stress applied for a short duration. In this process, if a component is properly designed, it will fail during this test.

Insulation resistance (IR) is a measure of leakage current of capacitor. If the construction and microstructure of capacitors are improper, then the applied current and voltage gives the way to fail the component. The measurement of IR at high temperature is a powerful and vital test to determine the quality of construction of capacitors.

Solderability test gives the cosmetics of coating of solder on the termination. De-wetting, non-uniform coating and dissolution of solder plating in the solder bath are the indications of improper solder plating.

Terminal strength test indicates the integrity of end termination with ceramic body of capacitor. If there is a mismatch of TCE between ceramic body and the termination, the terminal strength failure occurs.

Solderabilty, terminal strength and adhesion tests are destructive tests and hence these tests are conducted on sample basis.

V. RELIABILITY TEST

Table-I Life test data for reliability prediction

Life Test Data on Ceramic Chip Capacitor made by M/s Dalmia, Bengaluru

2-Dec-15

No	Centre	Life Test Data	Batch (Year)	Types #	Sample of each Type	Time	Dev.Hrs	Failure @	Actual Oper. Time	λFIT
S1	ISAC	Qual Batch	2006	28	25	2,100	1,470,000	2	1,467,800	170
S2	ISAC	Qual Ext	2006	10	10	10,000	1,000,000	3	991,000	378
S3	ISAC	Requal Batch	2011	28	25	2,100	1,470,000	5	1,046,700	597
S4	ISAC	Requal-Ext	2011	20	10	10,000	2,000,000	3	1,983,992	189
S5	VSSC	Qual	2011	13	25	2,100	682,500	2	680,300	367
S6	VSSC	Qual Ext	2011	13	10	10,000	1,300,000	2	1,291,000	194
S7	ISAC	Re-Qual	2015	2	50	1,000	100,000	0	100,000	0
		Total					**8022500**	**17**	**7560792**	281

@ 1 Faliure allowed in the batch with 25 samples;
The failure was distributed with only one failure observed in chip capacitor on one typ

Acceleration Factor as per Mil-PRF-55681E 8

Failure Rate (FIT) 281

Reliability is predicted based on the life test of components. Life test have been conducted on different batches of the Chip Capacitor fabricated by Dalmia, containing various styles, values, tolerances and rated voltage cumulating about 80 million device hours. Based on the test data, the calculated FIT is 281. Table-1 shows the details of the capacitors tested and actual device test hours. The FIT will further come down with life testing in future batches of the capacitors.

VI. CONCLUSION

The article explains about various steps involved in the processing of MLCCs and discusses about various defects in the MLCCs. Screening of hi-reliable MLCCs and the reliability is also presented.

ACKNOWLEDGMENT

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CCGA Assembly Process Design, Fabrication and Qualification Testing at Centum Electronics

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Abstract— Moors Law has made sure that the density of the active devices in the Silicon to reach the zenith. The corresponding packaging technology however has hit a road block due the size constraints of conventionally leaded packaging. This situation has led to the mode of Chip Scale packaging. In this context, the Column Grid Array packaging represents a k ey leveraging technology that offers high density packaging for high performance on Chip scale for FPGA devices with reliability performance levels that have the potential to meet Space application requirements. Thus, the Column Grid Array (CGA) is now an accepted packaging design replacing the Ball Grid Array (BGA) for high reliability applications. For qualifying the assembly process, at Centum Electronics, CCGA packages with daisy chains have been assembled on Polyimide laminate and their reliability performance is being evaluated. This treatise is the discussion on the Process Design, Fabrication and Qualification testing of CCGA assembly process that is currently in progress at Centum Electronics.

Keywords—SMD, CCGA, Temperature Cycling, ATC, reflow, PCB, PCBA, Daisy Chain,

I. Introduction

Surface mount soldering technologies and accompanying designs for Space and Aerospace applications are trending towards the high pin count devices to meet the ever increasing demand for miniaturization and reduction in weight with emphasis on increased performance and reliability. These grid array package configurations provide better signal integrity for high speed applications required by many field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuit (ASIC) devices. In this context Ceramic Column Grid Array and Ball Grid Array packages have allowed significant gains by offering shortest electrical paths between substrate and PCB and also improved thermal and electrical performances.

CCGA packages consists of Solder columns of predetermined length attached to Land Grid Array (LGA) package. Contrary to CBGA package where in high melt solder balls collapse and establish physical connection between PCB and the component package, CCGA packages maintain sufficient amount standoff distance between PCB and the package. CCGA columns which are made of SnPb alloy adds significant flexibility for the assembly and improve the reliability of the assembly for Hi-Rel applications.

Solder joint fatigue has been the major reliability problem observed in grid array packages which arise at interface of PCB and the package. Solder joint fatigue failure (Cyclic Stress) over period of time because to various stresses due to CTE mismatch between PCB and package. CCGA packages offer reliable standoff gap between PCB and the package and reduce the strains that is transferred to solder joints.

This paper addresses the complete Assembly Qualification activity for 1.27mm pitch 624 pin and 376 pin CCGA packages on multilayer non-woven Thermount Polyimide base PCB. Solder columns of these CCGA are made up of Sn20/Pb80 configuration with copper wrap around the columns throughout column length. The CCGA packages are assembled on the Qualification boards using automated pick and place and convectional reflow oven in controlled environment. Assemblies are subjected to various environmental tests such as Thermal cycling, vibration, shock, thermo-vacuum and humidity tests to evaluate the reliability of solder joints and column integrity. Dummy packages from Microsemi (624 pin) and Texas Instruments (376 pin) with copper wrapped columns of configuration Sn20/Pb80 are used in two types of Qualification board placement configurations to simulate the multiple placement configurations. At the time of this reporting, 700 cycles thermal cycling of the assembled qualification boards have been completed and no deleterious observations have been encountered. Remaining 300 cycles of thermal cycling is in progress.

II. Test Vehicle configuration

A. Package Details

For the CCGA Assembly Process Qualification purpose, two types of PCBs are designed wherein each board consists

of 4 CCGA packages with Daisy chain connections are routed to connector point for resistance measurement during environmental tests. The details of the packages used for qualification activities are shown in Table -1

TABLE-1
CCGA PACKAGE DETAILS

	AX2000-1CGG624B	**ADC12D1600CCMLS**
Column Information		
Column Attach Site	Six Sigma	Six Sigma
Column Composition	80Pb/20Sn	80Pb/20Sn
Copper Ribbon	Yes	Yes
Column Height	2.21 mm	2.21+0.135mm
Column Diameter	0.51mm	0.51+0.051 mm
Package Information		
Body Size	32.5 mm square	27.94 mm
Column Pins	624	376
Column Pin Notes	Orientation pin A1 – no column	None
Lead Pitch	1.27 mm	1.27 mm 1.0mm Heat sink pins at Centre
Ceramic Thickness	2.25 mm	2.790+0.280

B. Assembly Process Qualification board details

Qualification boards are fabricated using Polyimide base material which offers excellent CTE parameter which is crucial for reliability of space grade electronic assemblies. Details of the qualification boards are as provided in Table2 and Table 3.
Assembled qualification cards for Type A and Type B cards are shown in Fig 1 and Fig 2 respectively.

TABLE-2
PCB DETAILS-TYPE A

Size	149.00mm x 136.2 mm
Thickness	2.7 mm
No of Layers	16
Laminate Material	Non-Woven Thermount-Polyimide
PCB Finish	HASL
CTE	6 – 9 ppm/°C

TABLE-3
PCB DETAILS -TYPE B

Size	274 mm x 126.1 mm
Thickness	2.7 mm
No of Layers	16
Laminate Material	Non-Woven Thermount-Polyimide
PCB Finish	HASL
CTE	6 – 9 ppm/°C

Fig 1 Assembled Qualification board Type A

Fig 2 Assembled Qualification board Type B

C. Test Pattern Design

Land pattern for CCGA devices are designed as per the design recommendations provided by the component

manufacturers. “Dog-Bone” Via design with solder mask window of 0.05mm for CCGA pad is followed. Via holes are filled with qualified insulating epoxy material which eliminates the risk of solder flowing through via holes during reflow process. Fig 3 explains all relevant parameters considered for pattern design [6].

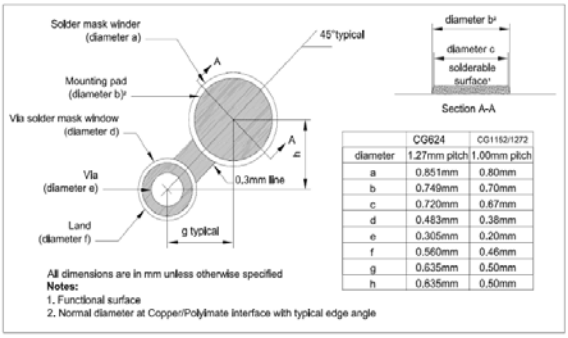


Fig 3 – Qualification test pattern for CCGA packages

The dummy CCGA devices (manufactured by OEM themselves) are internally wired to facilitate the electrical resistance measurements with the complementary circuit design at PCB side so as to form complete Daisy chain pattern. The 624 pin dummy CCGA package comprises of 5 independent loops and 376 pin dummy CCGA packages comprise of 1 loop and these are wired on the board and all connections are tapped through a 90º bent PTH connector. Collectively, Type A board has 8 loops and Type B board consists of 12 loops.

Fig 4 and Fig 5 show the Daisy Chain scheme for both 376 and 624 pin CCGA packages.

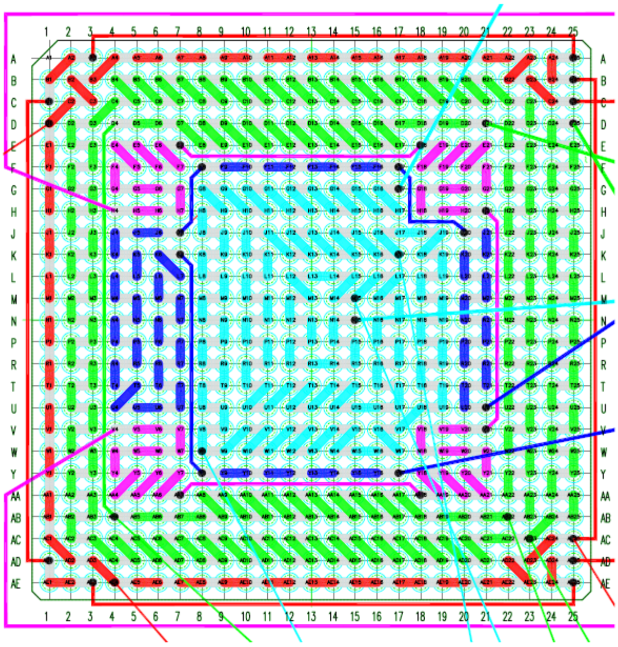


Fig-4 Daisy chain scheme for 624 pin CCGA

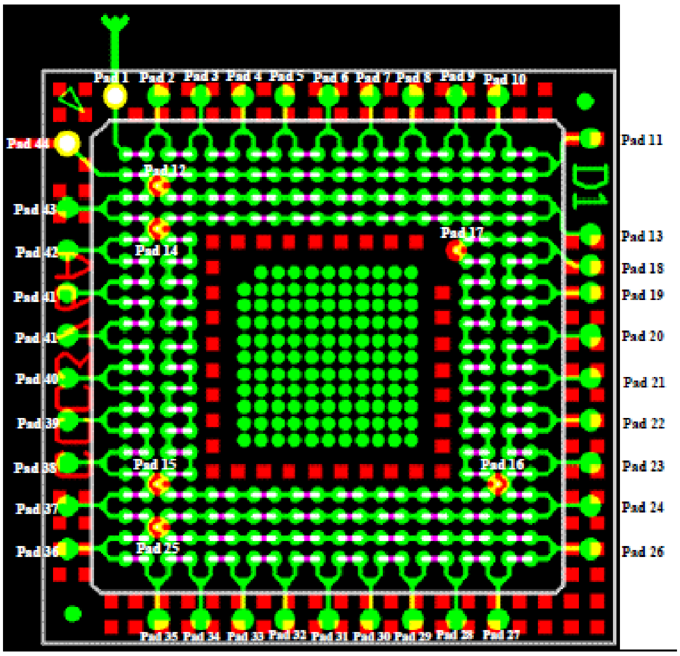
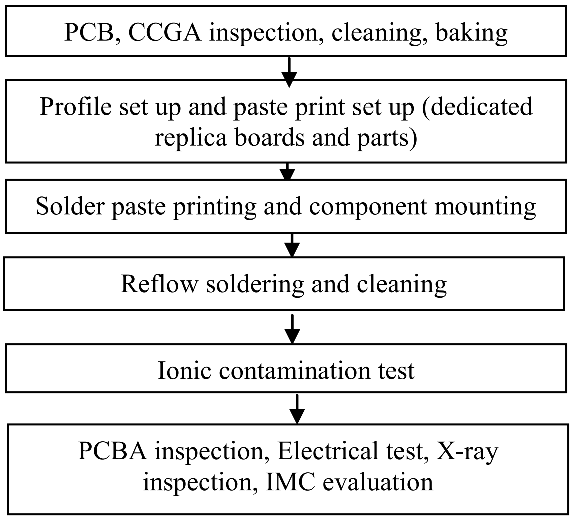


Fig-5 Daisy chain scheme for 376 pin CCGA

III. PCB ASSEMBLY PROCESS

Assembly of SMD components is carried out using an automated placement equipment with high placement accuracy followed by convection reflow oven in Nitrogen environment. The assembled boards are cleaned using DI water in cleaning machine as per the recommendation by the solder paste manufacturer. The process flow followed for the complete assembly process is as below.



Flow chart -1 Process flow for PCB assembly

Paste printing: Paste printing process is verified for solder paste volume and thickness uniformity before proceeding with the paste printing activity. Solder paste stencil is designed to achieve the optimal solder volume by selecting the appropriate opening dimensions. Solder paste volume and thickness are measured by 3-D optical

inspection equipment which measure the specified parameters across each component pad and also verifies for the missing prints and scattered prints.

Reflow soldering: Twelve zone convectional reflow oven is used for reflow soldering. Profiling of the oven is carried out for the leaded solder combination of Sn63/Pb37 water soluble paste using dedicated PCB which is exactly same as the actual qualification PCB by placing temperature sensors at predefined locations to simulate the actual temperatures at critical locations throughout the reflow process.

Reflow profile is designed considering the recommendations from the component manufacturer and complexity of assembly process which are the key parameters to achieve reliable solder joints for High-Reliability assemblies. Temperature on the component body and at the solder joints are kept well below the max parameters defined by the manufacturer. Fig 5 and Fig 6 show the typical reflow followed for the PCB assembly.

Setpoints (Degree Celsius)

Zone	1	2	3	4	5	6	7	8	9	10
Top	120	140	150	160	170	170	190	200	235	265
Bottom	120	140	150	160	170	170	190	200	235	265

Conveyor Speed(inch/min): 34.0

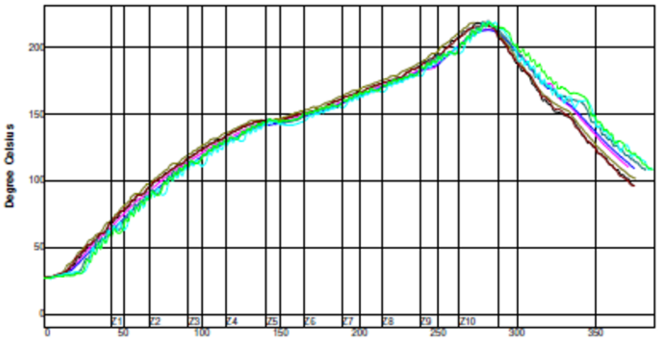


Fig-5 Reflow profile for Type A boards

Setpoints (Degree Celsius)

Zone	1	2	3	4	5	6	7	8	9	10
Top	120	140	150	160	170	170	190	200	230	260
Bottom	120	140	150	160	170	170	190	200	230	260

Conveyor Speed(inch/min): 34.0

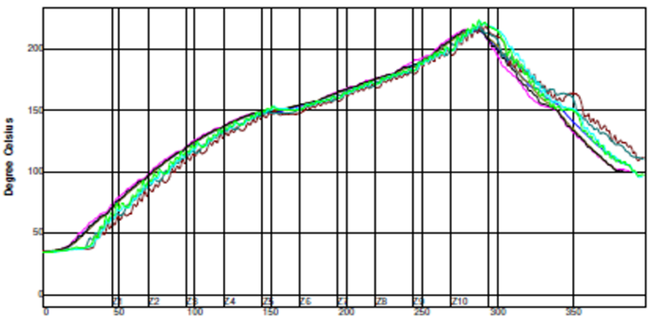


Fig-6 Reflow profile for Type B boards

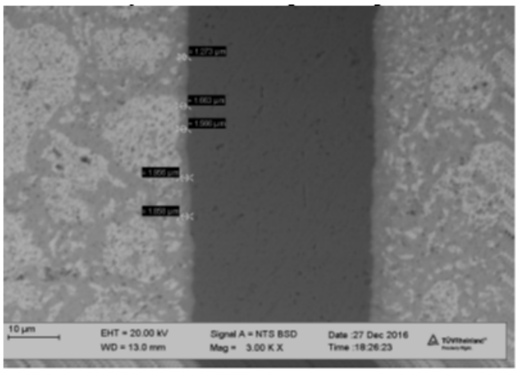
Cleaning of assembly:

Boards are cleaned in automated cleaning equipment using forced DI water method to remove flux residues from the assembly and the boards are tested for contamination level in Ionic contamination tester and found acceptable.

IV. QUALIFICATION TEST PROGRAMME

Considering the various failure modes of the solder joints in the operational period in High-Reliability applications, the qualification test plan has been designed. The qualification test scheme is focused on the simulation of stresses experienced by the space grade PCBA during its operational life time. Each test is followed by electrical and visual inspection to ensure that all the relevant aspects of the effect of the applied stresses are addressed.

Immediately after assembly of the CCGA packages one of the CCGA assembled board was taken through Inter Metallic Compound (IMC) Evaluation. The cross section of the sample was inspected and SEM photos were acquired using the Zeiss Scanning Electron Microscope (SEM-EDX) and analyzed using Olympus Microscope with Image Analyzer. Fig 7 shows the IMC results for the typical CCGA column on the test board.



Intermetallic Layer Thickness (µ)
1.273
1.663
1.566
1.956
1.858
Average Thickness.:1.663µ

Fig-7 IMC test measurements in sample column

Also, measure of tilt on soldered columns was done and tilt on columns were found to be well within the specifications defined inn ISRO PAX-300, Issue 5[2].Fig 8 shows typical measurement of tilt on a sample column.

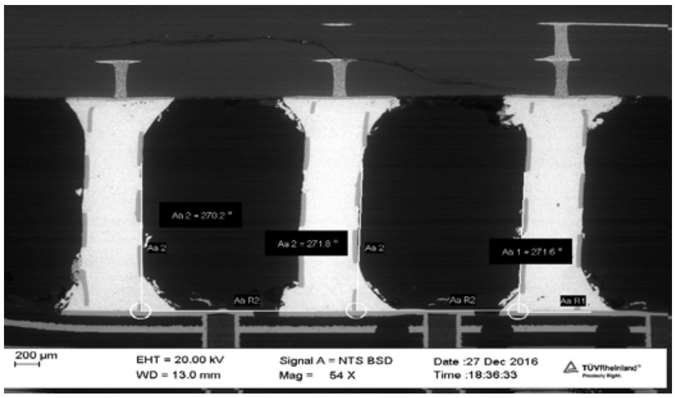
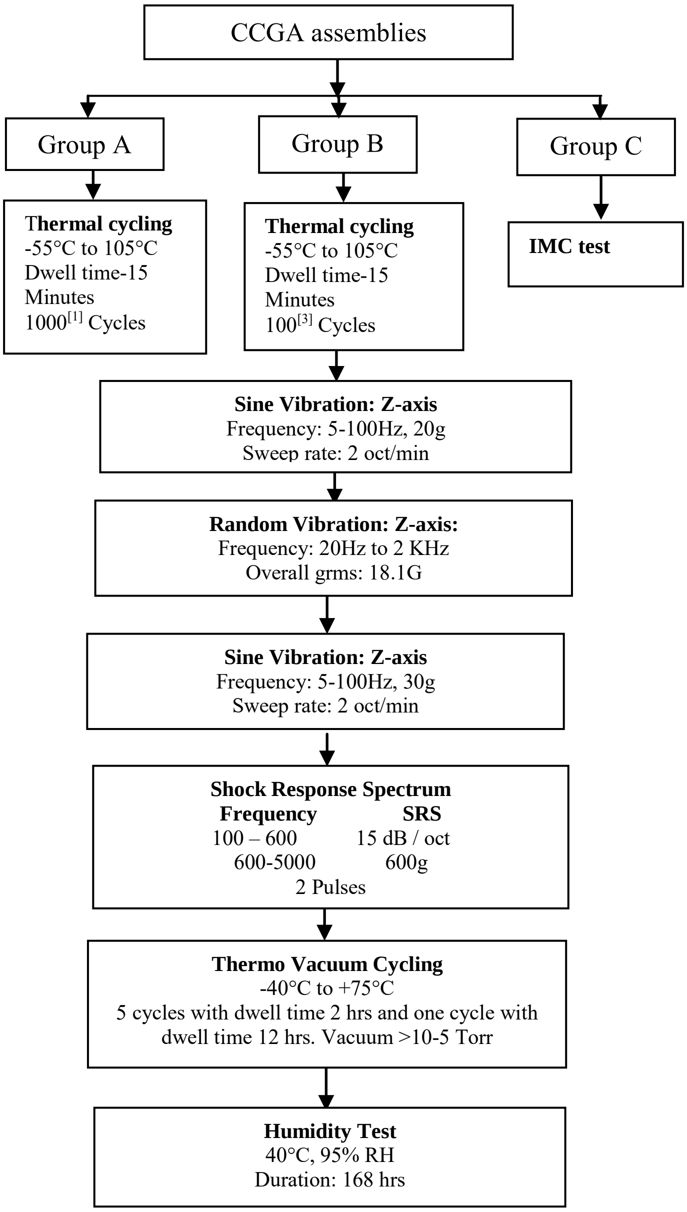


Fig 8 Measurement of angle of tilt in the column

The Columns examined have uniform shape and has formed a homogenous joint. Microstructure of the joints is regular and uniform throughout with Pb-rich phases of uniform dimensions distributed throughout the entire volume of the joint. The Pb has diffused through the entire volume of the joint and present on the component side.

Flowchart -2 shows the detailed qualification test scheme employed for the CCGA assembled units.



Flowchart-2 Qualification Test Plan for CCGA assembly process.

Units under both Group A and B are taken through Accelerated temperature cycling test. The profile for temperature cycling is fallowed as per the profile given in Fig 9.Dwell time of 15 minutes on each side and the ramp rate of 5°C/Minute followed throughout the cycling test. Each qualification boards are wired through individual harness connected to data logger.
Temperature cycling chamber is verified for accuracy of the chamber temperature at appropriate temperature levels. Data logger was programmed to record the readings of 60 individual loops at 5 minute interval with the weighted average of 100 readings in each measurement cycle. Fig-10 shows the thermal cycling test set up for the qualification boards.

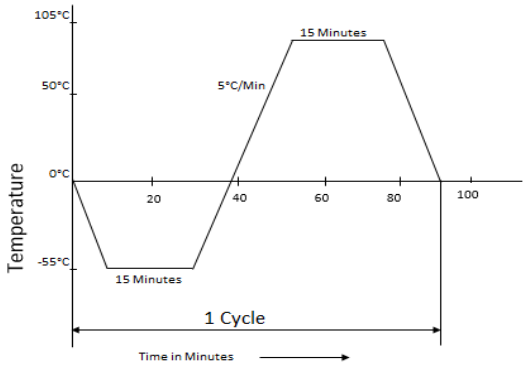


Fig-9 Temperature Cycling profile

Fig-10 Thermal cycling chamber

Below images shows the column and solder joint appearance at different stages of thermal cycling.

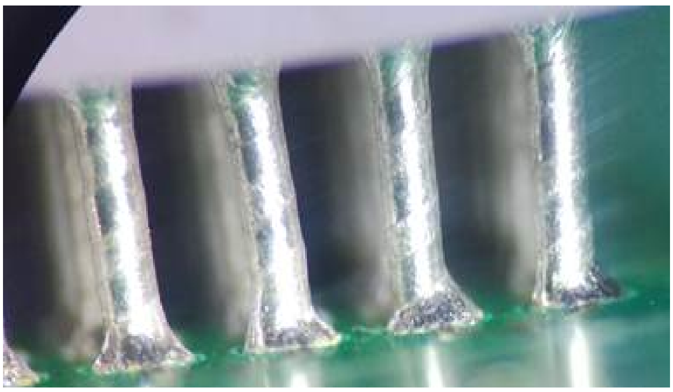


Fig-11A Pre temperature cycling

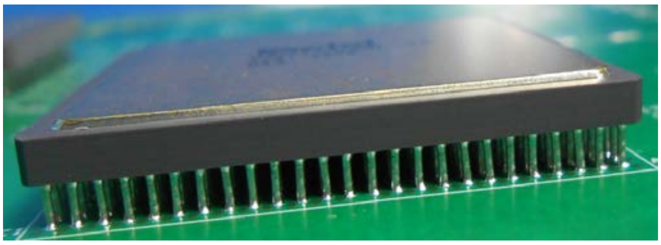


Fig-11B Pre temperature cycling

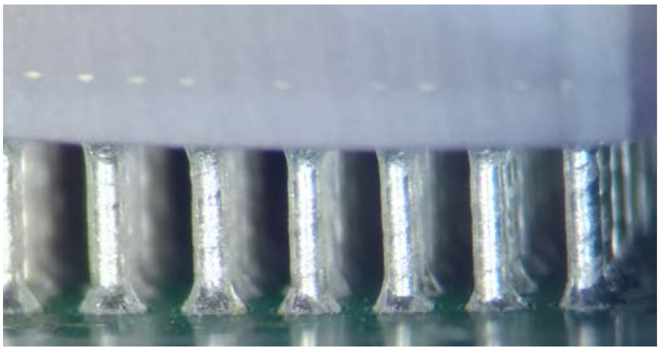


Fig-12A Post temperature cycling -100 cycles

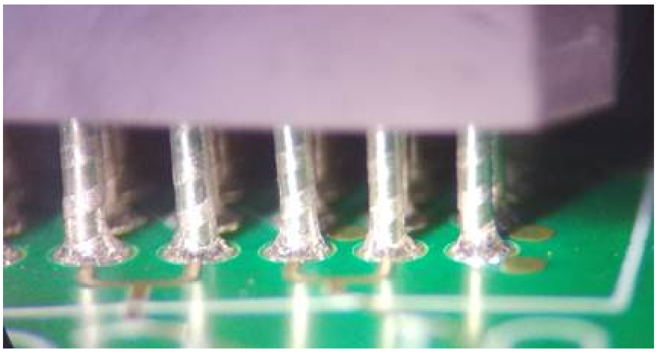


Fig-13A Post temperature cycling –

cycles

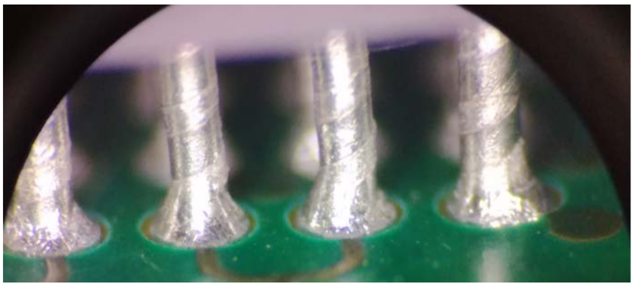


Fig-13B Post temperature cycling -500 cycles

V. TEST RESULTS

The test results after the completion 700 of thermal cycles are summarized in the table 4

TABLE-4

SUMMERY OF RESULTS

Board/coupon Identification Number	**Qualification Tests**	Test Results
Group A Type A_ 12 Type A_ 14 Type B_21 Type B_24	Thermal cycling[4] -55°C to +105°C 700 cycles	No deleterious visual observation such as solder joint cracking, column damages, column bend and grainy appearance observed in the board. The resistance values of the Daisy chains show very marginal increase and very much below the upper limit of acceptance value
Group B Type A_ 15 Type B_25	Thermal cycling -55°C to +105°C 100 cycles	No deleterious visual observation such as solder joint cracking, column damages, column bend and grainy appearance observed in the board.
Group C	Micro section Examination	Meets the requirements of IMC evaluation

VI. CONCLUSION

Based on comprehensive study of all the experimental results so far, it is clear that process qualification of CCGA assembly is well on its way towards meeting all the requirements laid down in the Qualification Test Program.

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Process Qualification of Filled Via and Via on Pad Interconnect Technology for Space Grade PCBAs at Centum Electronics

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***Abstract*—With the increased complexity of designs and with ever increasing need for miniaturization and size reduction, the need for integrating high pin count devices has firmly come into existence. This situation demands incorporation of very high via count in the PCB which results in significant reduction the real estate in PCB for locating other components. This situation demands that the via holes are filled by an automated process keeping in mind the high reliability requirements of space grade hardware. Also it becomes imperative to use the filled via for populating SMD and thereby reduce size and weight of the Space Hardware. To validate this innovative initiative, Centum has successfully carried out the qualification of these two processes to firmly establish their credentials for Space Grade PCBA.**

Index Terms—SMD, Filled vias, Temperature Cycling, ATC, Reflow, PCB, PCBA

I. INTRODUCTION

High density Printed circuit board design often involves complex high speed devices where in the need to meet critical parameters such as Signal integrity, Impedance matching, cross talk. These requirements pose significant challenges on component placement methodology which must be followed to accommodate the placement guidelines mandated by the component manufacturer. With the advent of area array devices board design constraints are pushed to extremes predominantly due to the High pin count and fine pith configuration which limits the flexibility of the designer to exercise proven wire routing practices.

Via in pad technology is in practice for commercial applications where the via holes are directly placed on SMD pads whose connections are tapped in subsequent inner layers. via in SMD can be achieved using mechanically drilled and epoxy filled cap plated through vias. These via holes were filled using TAIYO THP-100DX1 which meets the requirements of space grade material including TML and CVCM parameters. Filling and cap plating process eliminates the need of manual via filling process during PCB assembly

stage which is almost impossible for small via holes (smaller than 0.8 mm in diameter) for boards with higher thickness (2.7 mm, 16 layers) and multiple copper ground planes.

For the qualification purpose, board design involving very fine via hole of size 0.3 mm was employed over which SMD components of the package size 0402 were placed to simulate the impact of the process of SMD assembly over the SMD pad on which cap plated via holes were placed. To simulate real application scenario a 6 24 pin CCGA footprint was used and on the bottom side of the PCB, right under the CCGA package, the chosen SMD components were soldered using automated placement and reflow process. PCB laminate material is chosen as Thermount-Polyimide to reduce the CTE mismatch with CCGA devices.

Via holes are filled with TAIYO THP-100DX1 using mass hole filling equipment which fills the vias at vacuum environment. Co-processed coupons of the PCB manufactured have successfully underwent 500 Highly Accelerated Thermal Shock test cycles wherein the continuity of daisy chain is continuously monitored and compared with the initial cycle value.
Passive SMD parts of package size 0402 are soldered on to the PCB using automated assembly process with tighter process control and the entire assembled qualification board was taken through 500 c ycles of temperature cycling to evaluate the solder joint integrity (to evaluate the possible development of defects like solder joint cracks).

The overall qualification was carried out to cover the major aspects which have the potential to enhance assembly

density for space grade assemblies without compromising on the Quality and Reliability aspects. It is to be noted that the automated via filling using mass filling equipment significantly reduces the fabrication time and also increases the Reliability by reducing the probable damage to boards due to continuous exposure of board for soldering temperatures during manual via filling process.

II. COUPON AND TEST VEHICLE CONFIGURATION

A. Test coupon for HATS test

The HATS test coupons were designed by the PCB manufacturer with daisy chain pattern channeled through all copper layers connected through via holes. Total of 4 nets with each net consisting of 126 via holes (of size 0. 3 mm) per net are configured in the coupon of size 25.4 mm x 25.4 mm.

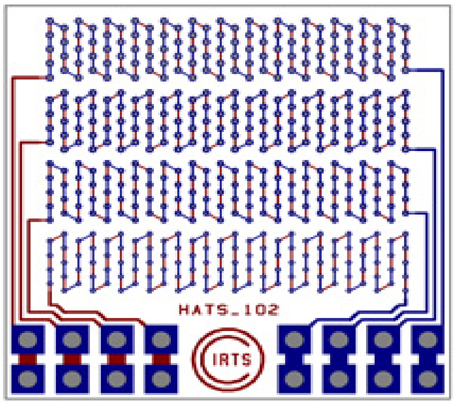

Fig 1-HATS test coupon

TABLE-1
COUPON DESIGN DATA

Size	25.4 mm x 25.4 mm
Thickness	2.7 mm
No of Layers	16
Laminate Material	Non-Woven Thermount-Polyimide
PCB Finish	HASL

B. Test vehicle configuration

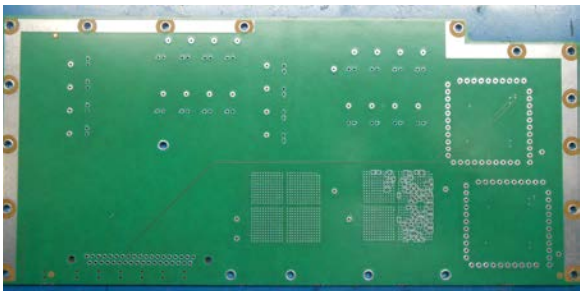

Fig 2-PCB with SMD components mounted on bottom side

TABLE-2

PCB DESIGN DATA

Size	274 mmX126.1 mm
Thickness	2.7 mm
No of Layers	16
Laminate Material	Non-Woven Thermount-Polyimide
PCB Finish	HASL
CTE	6 – 9 ppm/°C

C. Test Pattern Design for SMD on Via Qualification

Via holes are designed as “Dog-Bone” structure on CCGA side (Top side) where in via holes are placed outside the CCGA pad through copper tracks. On bottom side, SMD packages are directly placed on the pads with via holes

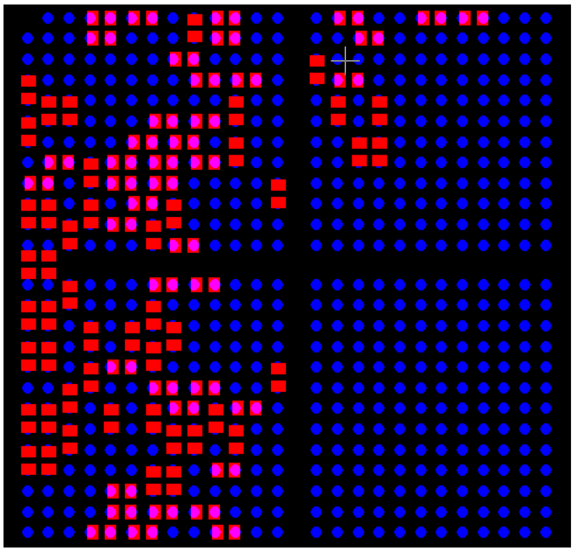

Fig 3 – Qualification test pattern

TABLE-3

LAYOUT DESIGN DATA

Feature	Dimensions
CCGA Lead Pitch	1.27 mm
Via Hole Dia	0.3 mm
Via Pad Dia	0.61 mm
Component (SMD) Pad Dimensions	0.88 mm x 0.66 mm

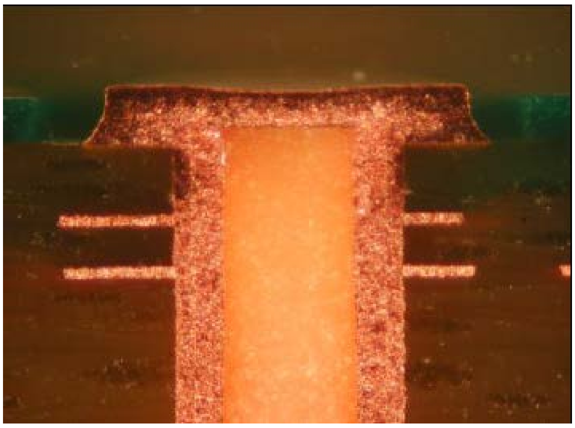

Fig-4 Typical cross section of Via hole filled with Mass hole filling equipment

Above example shows the cross section of filled hole with copper plating. This scheme is employed to improve the space utilization on the board and to achieve the best functional parameters. The risk of solder flowing through via holes is eliminated by the via filling process and surface leveling of via holes are maintained flat to the pad level by controlled plating process at PCB fabrication stage.

III. PCB ASSEMBLY PROCESS

Assembly of SMD components is carried out using an automated placement equipment with higher accuracy followed by convection reflow oven in nitrogen environment .Boards are cleaned with controlled DI water cleaning machine as per the recommendation by the solder paste manufacturer. The process flow followed for the complete assembly process is as below.

Flow chart -1 Process flow for PCB assembly

PCB Inspection, Cleaning, Baking
↓
Profiling of Reflow oven and Paste Print set up
↓
Solder paste printing and Component mounting
↓
Reflow soldering and Cleaning
↓
Ionic Contamination Test
↓
PCBA inspection

Paste printing: Paste printing process is validated for solder paste volume and thickness before proceeding with the solder paste printing activity. Solder paste stencil is designed to achieve the optimal solder volume by selecting the appropriate opening dimensions. Solder paste volume and thickness is measured by 3-D optical inspection equipment which measures the specified parameters (ex: solder paste volume) across each component pad and also verifies for the missing prints and scattered prints, if any.

Reflow soldering: Twelve zone convection reflow oven is used for reflow soldering. Profile set up is carried out for the Leaded solder combination of Sn63/Pb37 water soluble paste by employing a dedicated PCB (which is exactly same as the actual qualification PCB) by placing temperature sensors at predefined locations to simulate the actual temperatures at critical locations throughout the reflow process.

Reflow profile is designed considering the recommendations from the paste supplier and complexity of assembly which is the key parameter to achieve reliable solder joints for High-Reliability assemblies. Temperature on the component body and at the solder joints are kept well below the max parameters defined by the paste manufacturer. Fig 5 shows the typical reflow followed for the PCB assembly.

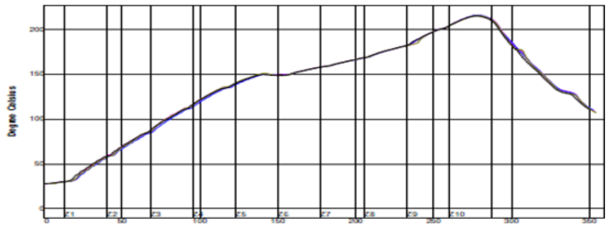

Fig-5 Reflow profile

Cleaning of assembly:

Boards are cleaned in automated cleaning equipment using forced DI water method to remove flux residues from the assembly and the boards are tested for contamination level Ionic contamination tester and found acceptable.

IV. QUALIFICATION TEST PROGRAMME

A. Via fill Process Qualification

HATS Coupons (which are part of qualification PCBs) are initially subjected to six reflow cycles to simulate the (pre conditioning) the real life conditions of filled vias on the PCB that undergo multiple reflow cycles during the actual board assembly process. Optimal number of reflow cycles are chosen considering the maximum number of reflow cycles allowed for the actual assembly process including rework processes.

Thus pre conditioned coupons are later subjected to highly accelerated thermal shock test wherein the coupons are taken through the temperature range from -40°C to +140°C where with each cycle duration is limited to 9.52 minutes. Electrical interconnection resistance of Daisy

Chains for each coupon are continuously monitored over 500 cycles and recorded for further analysis.

Resistance values after 500 cycles and also during the environmental test were within the range and without any open nets in all test loops. Representation of typical net for which change in resistance versus the temperature cycles is shown in Fig 6.

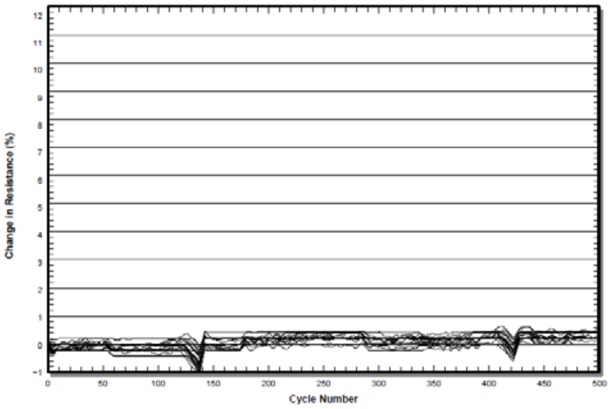

Fig-6 Percentage Change in resistance by cycle.

B. Via on Pad Assembly Process Qualification

Considering the various failure modes of the solder joints in the operational life in space applications, the qualification boards were taken through the accelerated temperature cycling for 500 cycles. Visual inspection was carried out for each 100 cycles to record the observations, if any, and solder joint evaluations. Fig 7 shows the Temperature Cycling set up deployed to carry out the cycling process. Fig 8 represent the temperature cycling profile followed for the Qualification.

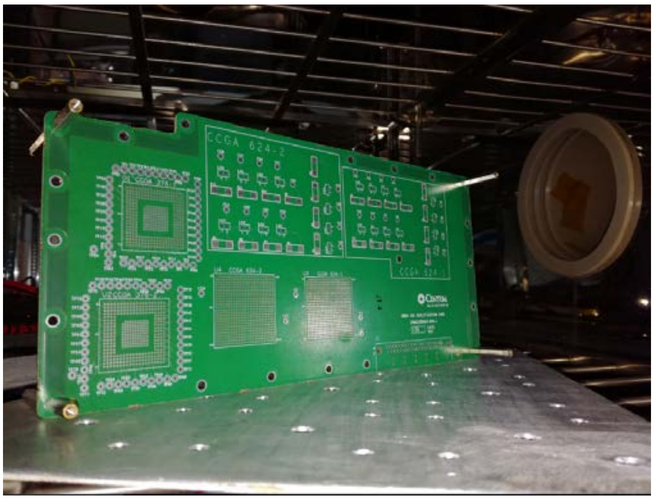

Fig-7 Thermal cycling chamber

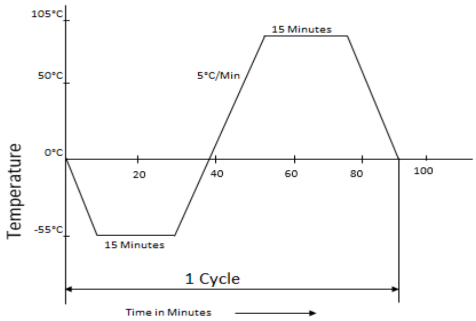

Fig-8 Temperature Cycling profile

A total of 500 Temperature Cycles have been carried out for assembly process Qualification. All parameters related to solder joint evaluation and via whole integrity are verified and no deleterious observations have been found.

Fig 9 and Fig 10A & B show the pre and post temperature cycling images of the solder joints from the via on Pad Process Qualification board respectively.

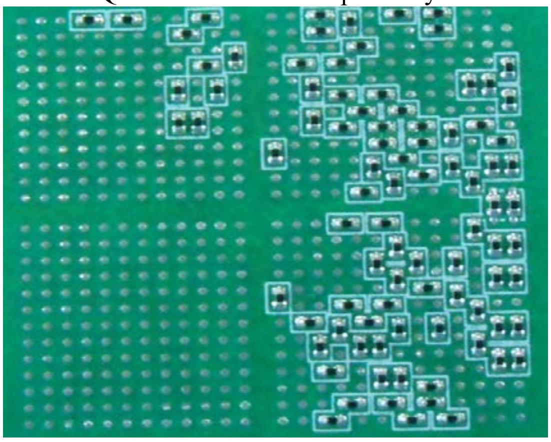

Fig-9 Pre temperature cycling

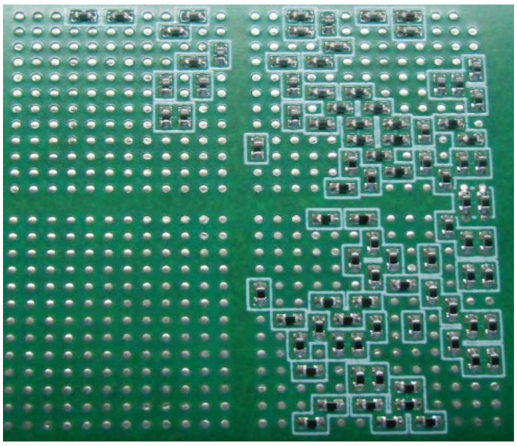

Fig-10A Post temperature cycling

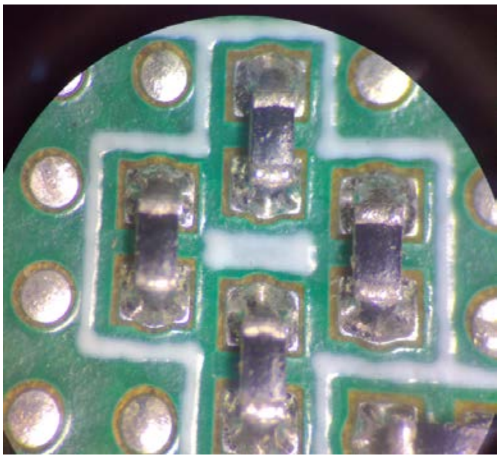

Fig-10B Post temperature cycling

V. TEST RESULTS

The test results after the completion of environmental qualification results are summarized in the Table 4

TABLE-4
SUMMERY OF RESULTS

Board/coupon Identification Number	**Qualification Tests**	**Test Results**
Coupon 1 to 24 (Via Filling)	Thermal Shock -40°C to +140°C 500 Cycles. Immediate transition and cycle time is limited to 9.52 minutes.	No failures in daisy chain resistance measurement. At the end of the test the increase in resistance values of chains are very much below the maximum acceptance limit of 10% indicating very high performance.
Board -B-26 (Via on Pad assembly)	[1]Thermal cycling -55°C to +105°C 500 cycles, 15 minutes dwell	[2]No deleterious visual observations such as solder joint cracking, via damages, grainy appearance observed in the board.

Based on the above results it can be concluded that via filling process and SMD component reflow soldering on the filled via holes have successfully passed the qualification tests.

VI. CONCLUSIONS

Compatibility of non-woven Thermount-Polymide laminate material with epoxy fill TAIYO THP-100DX1 is validated using HATS testing. Based on the results of Qualification Tests conducted on PCB assembly comprising cap plated filled via in pad of 0402 S MD components, it is concluded that both the cap plated filled via and via in pad technologies meet the requirements of Space Grade PCB assemblies.

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Integrated Approach of R&QA and Process-Optimization in RF Cable Assembly for Chandrayaan-2, Targeted Beyond Part Ratings

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Abstract— This paper describes the study on physical behaviour of materials for connectorized RF flexible cable (MF-141) assemblies with SMA/TNC connectors, under forced temperature range of -130˚C to + 120˚C, as required for Synthetic Aperture Radar (SAR) antenna of Chandrayaan-2 (CY-2) [1], and the learning gathered therein was employed for implementation in actual hardware. Such studies and implementations are useful for future Lunar / Deep Space Missions as traditional components/assemblies can be extended in terms of performance and benefit from earlier heritage.

Index Terms— MF-141 flexible cable, SMA/TNC connector, connectorized RF assembly, & Chandrayaan-2.

I. INTRODUCTION

An integrated approach between Component-fabrication and R&QA for an RF system, is presented herewith through a case study from hardware realization activity for Chandrayaan-2. The extended utilization of an available cable assembly, beyond its traditional temperature range with heritage, became necessary in view of the special requirements of the Lunar Mission.

Connectorized flexible cable assemblies (with SMA/TNC) are being widely used to interconnect RF subsystems in the realization of microwave payloads and spacecraft integration [2], [3], [4]. The reliability of these interfaces are well proven for conservative environmental applications of the spacecraft, where the applicable temperature ranges are well below the individual component ratings.

However, usage of these RF interface components for temperature range extended beyond the individual component rating involves the risk of either damage or incompatibility in interface due to part deformation. This use, hence, raises quality & reliability concerns. Therefore, in the event of required use beyond rated temperature limits, the deviation/deterioration of the component needs to be quantized & assessed for possible implementation of corrective/preventive measures to achieve feasible solutions.

For space bound system, the performance of RF interface components are well demonstrated, established and archived and have a l ong heritage under the controlled temperature range of 0°C to 40°C, which is well within the maximum operating limits defined by the individual part/component manufacturer. However, little information is available for usage of these RF components beyond the rated element temperatures.

A requirement arose to use these connectorized assemblies in the SAR antenna of Chandrayaan-2, where the applicable temperature limits are in the range of -130°C to +120°C [1]. These limits are well beyond the limits for which heritage is available. The impact of the extended temperature range, beyond rated limits, was to be studied, understood and employed in the component fabrication. The exercise carried out with the learning generated and the implementation plan is described below.

II. PROBLEM AREA IDENTIFICATION

For the purpose of understanding the impact of temperature beyond the rated limits on the material, a pilot test was conducted on three nos. of connectorized assemblies of flexible MF-141 with SMA & TNC connector, by subjecting the assemblies to a thermal cycling test. The cable-ends were purposefully kept unmated. It was found that the cable dielectric expanded in length as expected but it was learnt that the outer insulation sleeve (jacket) shrunk under thermal stress.

The known phenomenon of expansion in cable dielectric and the knowledge gained on shrinkage of jacket, was used to design a detailed experiment to quantify the deformation.

III. EVALUATION TEST METHODOLOGY

To quantize the physical impact of the extended temperature limits on the cable and cable assembly, an evaluation testing was conducted in two phases, i.e. i) Study of bare cable behavior and its effects after connector assembly for temperature ranges from -70 °C to +120°C ii) Demonstration of connector assembly operation for the required temperature.

A. Phase-1 Testing

Aimed to study the impact of targeted temperature ranges on

i) Elements of bare cable and

ii) Assembly of SMA & TNC connectors with cable.

This testing was carried out on three different sample configurations as explained below,

1) Design of Test Sample

Samples were designed in following three configurations,

Sample Configuration Type-1: In this configuration, behaviour of individual cable elements, as illustrated in figure-1 & table-1, was studied for the required temperature ranges from -70 °C to +120°C.

Sample Configuration Type-2: In this phase, impact of extended temperature ranges on cable assembly using both SMA & TNC connectors were studied for two further subsets, viz. i) with connectorized cable-ends arrested with connector-counterpart ii) Without arresting of connectors with their counterpart as illustrated in figure-3 & 4.

Sample Configuration Type-3:
In this case, cable of 300mm with straight ends, as illustrated in figure-5, were used for Cryo testing

a) Sample Configuration Type-1 (Formed Cable)

This test configuration was used for "*Quantitative analysis of Relative expansion or contraction of individual cable elements" as marked in the figure below.* 3 nos. of formed cable were used for testing. Test cables were fabricated as per sample description given in figure-1 & figure-2. The total length of test sample was 300mm, however both sides of cables were formed as explained in figure-2 with each part of the formed portion i.e. "A", "B" & "C" were 5mm.

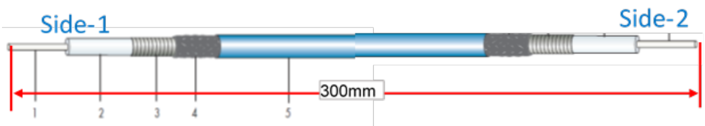

Figure: 1: MF-141 cable with formed cable sides

The detail of cable elements is as per table-1,

Table-1: Cable Elements

Sr. No.	Description	Material Name
1.	Centre Conductor	Solid Silver plated Cu Wire
2.	Dielectric	Solid PTFE
3.	1st Outer Conductor	Silver plated Cu Tape
4.	2nd Outer Conductor	Silver Plated Cu Braid
5.	Jacket	Fluoroethylenepropylene

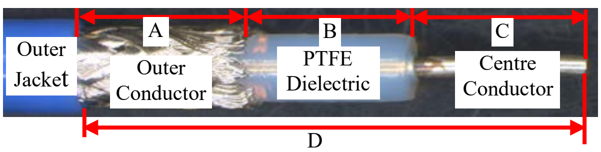

Figure: 2: Description of Sample Configuration Type-1

b) Sample Configuration Type-2

In this sample configuration, size of the cables was same as of sample configuration type-1, however cable end configuration was different as explained below,

i. Connector assembly (2SMA+1TNC) carried out at one side after 10 cycles while other cable-end was kept free, to quantize material elongation/ shrinkage in next 15 cycles.

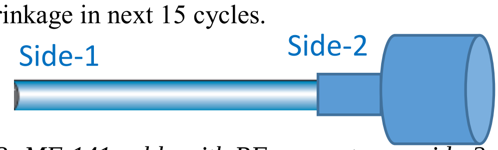

Figure: 3: MF-141 cable with RF connector on side-2

ii. Subsequently, similar connector assembly on other side of the cable to be carried out after compensating for material elongation/shrinkage recorded after total 25 cycles, this assembly to be subjected to further 25 cycles to detect further damage, if any.

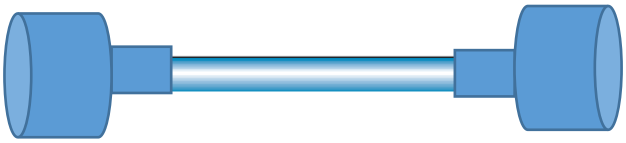

Figure: 4: MF-141 cable with RF connector on both sides

c) Sample Configuration Type-3

In this case, cable of 300mm with in-plane (flat-cut) ends, were used for Cryo- temperature testing.

Figure: 5: MF-141 cable in-plane on both sides

2) Evaluation Test Plan

Table-2: Evaluation Test Plan

Type 1 Bare Cable Group, 3 cables with formed ends + 1 cable with in-plane ends	**Type 2 Connectorized Cable, 3 cables-connector assemblies**	**Type 3 Bare-Cable, Cryo-Test 2 bare cables with straight ends**
Cable ID: ST-1-1, ST-1-2, ST-1-3, & ST-1-4 (in-plane ends)	**Cable ID: ST-2A-1 & ST-2A-2 (SMA) ST-2B (TNC)**	**Cable ID: C-1 & C-2**
Visual + Dimensional	Visual + Dimensional	Visual + Dimensional
10 cycles, -70/+120 [5] 1 °C/min, dwell -15mins.	10 cycles, -70/+120 [5] 1 °C /min, dwell -15 mins.	25 cycles, -196/+120°C Manual transfer
Visual + Dimensional	Visual + Dimensional	Visual + Dimensional
15 Temp. Cycles as above	Assembly of SMA/TNC connectors at one end	-
Visual + Dimensional	15 Temp. Cycles as above	

25 Temp. Cycles as above	Visual + Dimensional	
Visual + Dimensional	Assembly of SMA/TNC connectors at other end	
-	25 Temp. Cycles as above	
	Visual + Dimensional	

3) *Phase-1 Test Results*

a) Sample-Configuration Type-1 (Bare Cable Test Group)

i. Out of three cables; test results for one cable ST-1/1 are mentioned below for reference. The Table-3 (for side-1 of ST-1/1) gives measured values for the microscopic images taken immediately after the proposed temperature step.

For the purpose of measuring the dimensional changes, the cable center conductor, assumed having nil thermal hysteresis manifestation, was considered as the reference point. To quantize the expansion of solid PTFE (Teflon) i.e. dimension “ΔC” & shrinkage/ contraction in the cable outer jacket i.e. dimension “ΔD” (refer Figure 2 above) was recorded.

Table-3 summarizes the expansion/contraction observations throughout the thermal cycling test. This gives the trend of cable behavior over the progression of temperature cycles and also indicates the stage up to which maximum shrinkage of jacket takes place. Other two cables, shown the similar trends.

Table-3: Summary of Dimensional Measurement for Cable Side-1

Feature	**Cable Side-1**			
	Initial	**Post 10 Thermal Cycles**	**Post 25 Thermal Cycles**	**Post 50 Thermal Cycles**
ΔC Teflon Expansion	0 (C = 5mm)	-0.019	-0.296	-0.389
ΔD Jacket Shrinkage	0 (D = 15mm)	0.685	0.734	0.759

ii. It is inferred from the above test results that the maximum ***expansion of the Teflon*** is up to 25 cycles while the maximum ***shrinkage of jacket*** occurs within first 10 cycles but stabilizes by completion of 50 cycles.

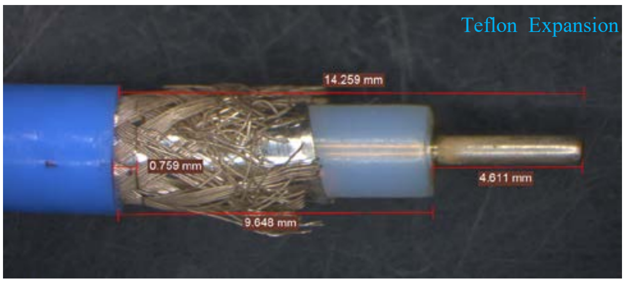

Figure 6: Physical Changes in cable elements

b) Sample-Configuration Type-2 (Connector Assembly Test Group)

i. Cables with straight ends (without formed ends) were used and were subjected for 10 temperature cycling for stress relieving purpose. These cables also showed expansion/shrinkage of PTFE & outer jacket respectively.

ii. After this initial stress-relieving, two out of three cables were assembled with extended Teflon SMA Male connectors (Tyco make, 105298-01) leaving the other end as formed cable only. The remaining one cable is assembled with TNC connector (Radiall make R143413661).

iii. With the understanding developed in testing of Type-1, it was thought of arresting cables with its counterpart (Female connector) during thermal cycling.

This was planned to see two different aspects -

- The net change due to expansion/shrinkage with respect to free end of the cable while other end is arrested.
- The impact of expansion/shrinkage, on t he integrity of solder joints, while the assemblies are mated with their counter parts on both sides.

iv. Subsequently; after another 15 nos. (25 cycles) of temperature cycling, SMA/TNC connectors were assembled onto the other side i.e. free-end of the cable. Then after assemblies were subjected for another 25 thermal cycles.

v. SMA connector assembly with arresting of counter part

- *No protrusion of center conductor observed*

vi. TNC connector assembly without arresting with their counter part

- *No protrusion of center conductor observed*

vii. SMA connector assembly without arresting of counter part

- outer jacket shrinkage indicated by protrusion of center conductor by approximately 1mm (Figure-8)

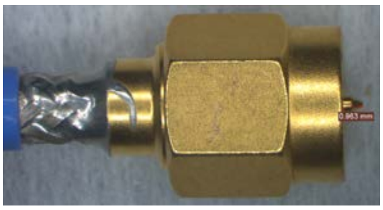

Figure-7: ST-2A-2 showing outer jacket shrinkage

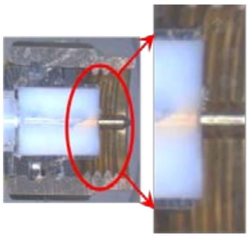

Figure: 8a: Micro-section of good connector

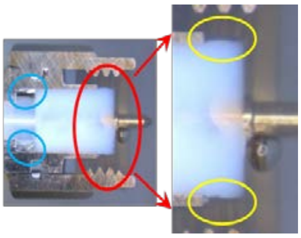

Figure: 8b: Micro-section of connector as in figure-5

Figure-8a and 8b compares the protruded connector with the good one. Post, 50 cycles, no degradation observed in the integrity of solder joints in both cases i.e. arrested/non-arrested conditions.

c) *Sample-Configuration Type-3 (Cryo Subgroup)*

In-plane samples were used for Cryo subgroup testing.

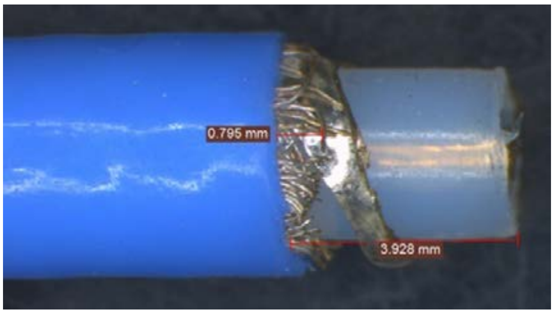

Figure: 9: Expansion/Contraction after Cryo testing

Observations of outer jacket shrinking were matching with the observations as of sample configuration type-1, however, amount of PTFE expansion was more (≈4mm) compared to the type-1 samples.

B. Phase-2 Testing

Phase-2 testing was aimed ***to implement the understanding gained from phase-1*** testing and ***to demonstrate the survivability*** of connector assembly process for targeted CY-2 antenna applications. Learnings of phase-1 were implemented during fabrication of Phase-2 samples by modifying the existing fabrication process sequence.

1) Sample Design

For phase-2 testing, the samples of phase-1 (type-2), with 700mm length instead of 300mm, were used. The extended cable length was used for further investigation of impact of extra cable length on the findings of phase-1 testing, if any.

2) Evaluation Test Plan

Table-5: Phase-2 Evaluation Test Plan

Thermal Shock# Group [5], 6nos. of samples	**Simulated-Temperature Test Group, 3nos.of samples**
SMA-1, SMA-2, SMA-3, SMA-4, TNC-1 , TNC-2	SMA-1, SMA-2, TNC-1
50 thermal shock, -70/+120 °C 15 min dwell	*Same Sample after completion of thermal shock group is used here*
Visual + Dimensional	25 cycles, -130/+120°C 15min dwell, manual transfer
Cable forming with SMA/TNC connectors assembly at end-1, SMA arrested with counterpart while TNC kept un-arrested	Visual + Dimensional
15 cycles, -70/+120 °C 1°C /min. ramp rate, 15 min dwell	RF Characterization
Visual + Dimensional	
SMA/TNC connector assembly at end-2	
25 cycles, -70/+120 °C 1°C /min. ramp rate, 15 min dwell	
Visual + Dimensional	
RF characterization of Cables	

 # Stress relieving was carried out by subjecting bare cables to thermal shock instead of thermal cycling

3) Phase-2 Test Results Summary

a) Thermal Test Group

i. Thermal shock on bare cables, results confirm the observations of phase – 1 testing.

ii. Thermal cycling on Connectorized assembly with their counter-part
- Interface dimension measurement meets the specifications, Pre and Post thermal cycling test, of Male Di-electric (MD) & Male Pin (MP) of ± 10mil
- RF characterization meets the specified requirements, Pre and Post thermal cycling test, of S11/S22 (better than -18dB) and S12/S21 (better than -0.6dB).

b) Simulation-Temperature Test Group - Three samples (2 SMA + 1 TNC) of thermal shock group were subjected to the temperature testing as required for CY-2 antenna. A special test set-up was designed to achieve -130°C temperature, however, normal hot storage chamber was used for +120°C.

A container with heaters was used and cables were mounted on container walls. The cable temperature was regulated at -130degC, after inserting the container in a liquid-nitrogen (LN2) filled Dewar, with controlled heating of the container through pre-mounted heaters, to rise from LN2 temperature (-196degC) to the required temperature of -130degC. The cable was removed from container after pre-scribed dwell time (15min) and loaded in a baking–chamber pre-heated at 120degC (again 15min). The cycle was repeated 25 times prior to assessment of the cable-connector component.

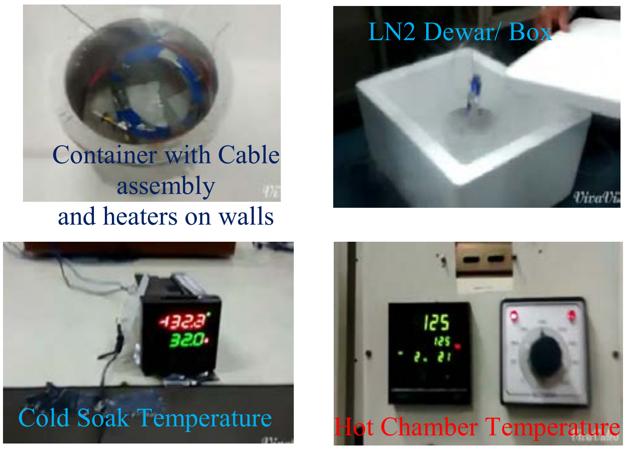

Figure: 10: Test Set-up for Cryo testing

Post Simulated-temperature test, RF characterization and interface dimension measurement meets the specified requirements. ***No damage to the cable or assembly was observed and no deterioration in appearance or resilience of cable was detected***.

IV. Conclusion

The objective of using the RF interface Component, consisting of RF interface component consisting of Flexible-cable connetorized at both ends, ***with required preparation and tailoring the assembly process for the component***, at targeted temperature range of -130 to +120 °C ***was met successfully***. The realization of the component was found meeting the requirements of quality and reliability and the flight component has been fabricated using this technique.

Acknowledgment

The authors wish to thank Head-PMQD(E)/SRG for his continuous effort in motivating us throughout the qualification testing. The authors also with to thanks Shri A. K. Lal, GD-SRG and Shri K. B. Vyas, GH-SRG for inspiring to come forward with this paper on a challenging work. The authors are extremely grateful to director, SAC for his continuous encouragement to achieve higher objectives and the activity under this paper is one such successful attempt.

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D

RADIATION HARDNESS ASSURANCE AND FAILURE ANALYSIS

Failure Analysis Tools and Techniques for Hi-Rel Electronics

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Abstract- Failures in electronics space hardware or any Hi-Rel electronics hardware may occur at any of the stages from developmental or breadboard level evaluation to the final integrated level realization of the flight subsystems. The incorporation of all concepts of quality and reliability has also not eliminated these failures totally. This paper describes the Failure Analysis (FA) tools and techniques employed for Hi-Rel Electronics and how these are employed to detect the root-cause of the failure. The methodology used in the FA investigation depends on the severity and type of problem. Proper failure-history data collection which includes information about component assembly, location, application and optimization environment, part details, past experience relevant to the failed part, failure symptoms and failure mode go a long way in carrying out a precise FA. The techniques used in conducting FA range from simple electrical measurements to examination of decapsulated samples under different types of microscopy to detect failure signatures. The detection and assessment of failure signatures, hypothesis of failure mechanisms followed by failure simulation are employed to reach the root-cause of a failure. The root-cause of a failure can be poor quality of component, wrong component, lapses in assembly, wrong application, so on and so forth. The identification of root-cause leads us to implement the remedial actions that can prevent the recurrence of failure, which is the ultimate objective of FA. The FA tools and techniques can best be well understood with a few case-studies successfully investigated.

***IndexTerms*— Failure analysis, destructive, nondestructive, root cause, EOS**

I. INTRODUCTION

This paper describes the tools and techniques employed in Hi-Rel fabrication, assembly and realization of space hardware. Some of the Failure Analysis cases involving the Hi-Rel parts that failed at different stages of realization of sub-systems of Spacecraft are described here. The details cover initial investigations of failure symptoms and signature, the simulation exercise and the remedial actions (or precautionary measures) implemented during subsequent fabrication/design of circuits/subsystems for Space Payloads. The main objectives of the failure analysis are to analyze all the probable causes and reasons of failure, identify the root-cause and take corrective and preventive actions, so as to improve the probability of success (by preventing recurrence of failure). This goal can best be achieved if all modes of failure are known and understood. Some situations do exist, in which the problem is not at all with the failed component, but lies with the wrong application of the component or lack of proper circuit protection or overstress during fabrication itself. These events may cause the failure of the component by exposing it to higher-than-normal stress levels that the device is rated to withstand, leading to immediate or time-bound failure. Failure analysis effort is directed to determine whether the fault is due to circuit-design, workmanship, environment or part-batch quality. The actual failure analysis is largely dependent on the type of part, expected failure mechanisms, observed failure modes, package construction and technology utilized.

II. FAILURE ANALYSIS TECHNIQUES

Each FA technique in the investigations is designed to provide its own, specialized information that will contribute towards the determination of the failure mechanism of the sample. Although FA techniques are generally independent of each other, their results must nevertheless be consistent and corroborative in order to arrive at a single explicit conclusion or at least a strong indication towards a unique probabilistic event for the completion of an FA cycle. There are many techniques used in failure analysis and choosing the right one is an art as well as science. Sometimes we may need to use many techniques both for better detection as well as independent corroboration so that we can be precise in our interpretation and inference. However, all tests or evaluation methods fall into one of two categories - destructive testing, and **nondestructive testing**. Nondestructive testing is a type of test which causes neither permanent change nor adds any signature to the electronic part under ideal conditions. Conversely, destructive testing damages the components to certain extent or adds an expected signature. Of course, there are times when we have to physically alter the form of the parts in order to analyze the physical form of part-construction and reach inside part structure [1] [2].

A. Nondestructive Techniques

A few of the conventional non-destructive techniques are as follows -

1) *Optical Analysis technique:* Using a stereo microscope, a thorough external visual examination of the suspect part at 10X to 30X magnification should be performed early in the failure analysis process. Magnification levels up to 100X can also be employed to further examine any anomalies identified. The following aspects should be specifically examined for:

- Surface Contamination
- Mechanical damage
- Thermal or electrical damage visible as discoloration
- Part-package Seal integrity

- Termination/Lead integrity

2) *Pin to pin electrical testing:* Pin to pin impedance (electrical) testing is done using curve-tracer, which involves studying the characteristics of each possible combination of I/O for a multiple I/O part, in a failed part removed from the circuit. Each pin to pin path is a combination of various circuit elements, like resistor, capacitance and/or diode and may even include single/both junctions of a transistor. By measuring the electrical characteristics of a failed part and comparing with a known good part a degradation/malfunction is detected. Hence, the failure mode and on-chip failure site location becomes possible.

*3) Radiography:*Radiograph (refer to Mil-Std-883 Method 2012), often referred to as X-ray image, is a very powerful tool for non-destructive failure analysis as X-ray can detect actual or potential defects within enclosed packages. Basic X-ray imaging or Computerized tomography allows internal part examination for detection of:

- Internal particles
- Internal wire bond profile to make sure the wire bonds are not touching each other or package lids
- Die attach quality (voiding, die attach perimeter)
- Solder joint quality for connectors
- Insufficient or excessive solder
- Substrate or printed wiring board trace integrity
- Obvious voids in the lid seal
- Foreign metallic particles within the package
- Internal part orientation, etc.

4) PIND (Particle Impact Noise Detection): Cavity device failures can be caused by internal conductive particles shorting adjacent conductors. While X-ray techniques can be used to detect internal particles, another method is Particle Impact Noise Detection (PIND, refer to Mil-Std-883 Method 2020). PIND Testing can be subjective and may not be easily performed on complex hybrids. However, it can provide evidence of loose internal particles. A common technique employed is to perform X-ray and PIND together; wherein first an X-ray is taken, then the part is PIND tested, and then a second X-ray is taken. This allows one to identify particles that are loose and free-moving within the package.

5) SAM (Scanning Acoustic Microscopy): This is one of the most useful non-destructive examination techniques for FA and also used for evaluation of the construction of electronic parts. Acoustic Microscopy is a technique that uses high frequency ultrasonic energy (typically 10MHz and higher) to look inside objects, detect defects and characterize material interfaces and changes. Here Imaging is based on the difference in acoustic impedance of the materials, i.e. wherever signal sees change in the acoustic impedance, it gets reflected and based on the amplitude of reflection images are created. Layer by layer information is possible. Acoustic microscopy is useful to identify void, crack or delamination because air is having lowest impedance and almost all signal gets reflected back from the location of void or crack. It is used for-

- Distinguishing between different materials of a solid surface.
- Determining the thickness of different material layers.
- Displaying variations in the elastic constants on a microscopic scale.
- Examining regions surrounding dislocations and faults in single crystals that are highly stressed.
- Detecting surface defects, flaws, inclusions and disbonded areas.

6) *IR Thermal mapping:*A primary cause of failure in semiconductor devices is excessive temperature at junctions, leading to thermal runaway or to degradation due to thermally accelerated mechanisms. Thus it is important to have some means of determining temperature profile of a part while in electrical operation. In most parts that fail, direct access to the malfunctioning or over-stressed region/junction in a module may not be possible. Hence, Infra-Red mapping of hot-spot is helpful in such cases to identify the culprit region. IR thermal imager provides visible images and a thermograph shows the corresponding temperature. In case of FA, image of failed part and good part under biased condition is obtained separately and compared to detect any abnormality in the failed part.

B. Destructive Techniques

*1) Part De-Lid Process:*After all Non-destructive examinations are performed; the part is decapped carefully using standard decapping procedures. For cavity parts, this often involves a process called "delidding" where the device lid is removed, often by grinding down the lid around the seal ring or weld seal or with hot temp delidder or TO can/ceramic opener. For Plastic Parts, a combination of H_2SO_4 and HNO_3 acid jet is used.

*2) Cross-Sectioning:*It is a very important means of failure analysis of molded or composite structures like connector, printed wiring board, substrate, solder joint, capacitor, resistor transformer, transistor and diode. Prior to cross-sectioning, the sample is usually molded in a hard setting acrylic or polyester resin. The failed part is cut such that further controlled grinding and polishing reveals the plane of interest to allow detailed microscopic examinations to be made.

3) Internal Visual Inspection: Most of the electrical or mechanical damage, either causing or resulting from a failure is visible under microscopic examination. After decapping, the failed device is visually examined to detect and study the failure site and signatures. These examinations are typically performed using a compound microscope at magnifications of 100X to 1000X. Microscopes equipped with both dark and light field illumination allow those features to be detected which are difficult to detect by direct illumination.

4) SEM (Scanning Electron Microscope): It is an important tool for semiconductor die as well as metallurgical failure analysis. The SEM can provide detailed 3D images of up to 120,000 X magnification, with typical magnifications of 50,000 to 100,000X and a resolution down to 25 Angstroms.

With a SEM image, the depth of field is fairly large, thereby providing a better overall three-dimensional view of the sample. While high power optical microscopes can also reach 1000 X, the depth of field is usually very small and only features in a single plane can be examined. The electrons interact with atoms in the sample, producing various signals that can be detected and that contain different information about the sample's surface topography and composition. Its ability to operate in many different modes coupled with the relative ease of sample preparation has rendered it particularly valuable for device assessment under failure analysis. The various forms of voltage contrast can be helpful in confirming the electrical failure site.

5) IR Microscopy: This method requires the decapping of part and relies on the transparency of target material or semiconductors to IR wavelengths. Using specific IR source and detection system, certain types of failure, such as solder-ball or bump bond defects, attach-voids, intermetallic diffusion, overstress effects, and spiking across layers, internal shorts in bulk semiconductor etc. can be identified. ESD and corrosion damage in the inner layers of devices can also be identified. In some cases, selective etching of glassivation and metallization layer is required. This technique is also very useful to inspect die attach medium.

6) Fault isolationthough ultrasonic/Laser cutting: Once the failure site is identified to a small area of a complex part, individual element on the part may be required to be electrically isolated from surrounding elements and tested. It is carried out through different methods like ultrasonic cutting, Laser cutting etc.

7) *Die probing:*Once individual element in a complex microcircuit is isolated or identified from surrounding circuitry, die probing is done to electrically characterize the element. Probe-station is employed to minimize manual access to the fine geometries on-chip. Movements of the probe tips are observed through the microscope and probe tips are placed on metal traces/pads of the isolated device in an appropriate way to energize and sense it for evaluation.

III. FA CASES DUE TO ASSEMBLY AND FABRICATION STRESSES

Part packaging involves closed packing of a variety of different materials and some of the major problems have occurred due to mismatches in the expansion coefficients between these materials during soldering or assembly [3]. Two such cases are covered below.

A. CWR06 Failure

Post assembly defects like cracking and separation were detected in seal-plug of end-caps of CWR06 style SMD capacitor. These were observed at an advanced stage of realisation of the flight hardware. The two part types affected were 10µF/25V, case-code G and 6.8µF/35V, case-code H. The observations were -

- Separation of end-cap metal termination and epoxy at the negative termination seal-plug.
- Cracking of epoxy at the negative termination seal-plug.

However, in no case any such observation was seen at the opposite end of device, which is the positive terminal.

1) Construction(Fig. 1)

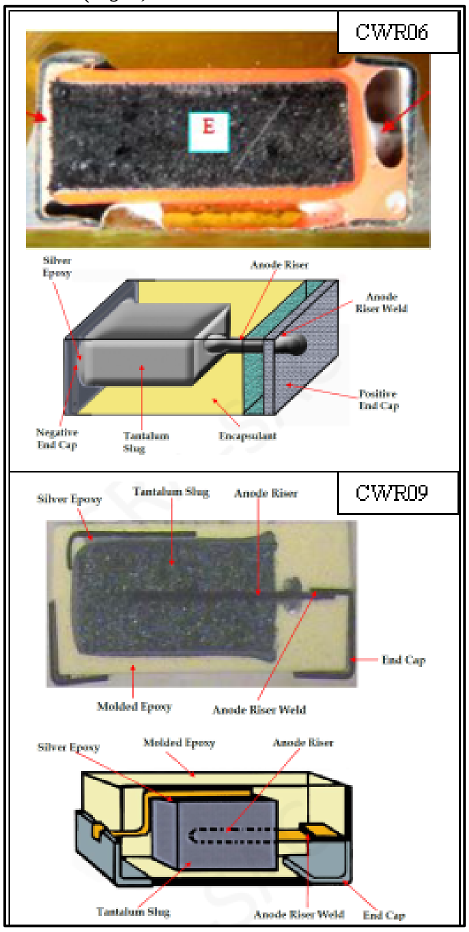

Fig. 1. Construction of CWR06 and CWR09 capacitors

To elaborate the construction of the part, consider a tantalum slug that has a carbon coat followed by silver coat with one end attached to negative terminal end-cap using a silver-filled epoxy[4]. The remaining gap between the end-cap periphery and capacitor body is back-filled with a non-conductive epoxy having “black pigment”. This “black epoxy”, the end-cap, silver filled epoxy attach medium, and the prepared tantalum slug make a closely packed structure at the negative termination. The positive termination at the other end has a tantalum riser (wire), coming out of the tantalum slug that is welded to the positive terminal end-cap. The gap between end-cap at this end and capacitor body is filled up using another non-conductive epoxy having “pink pigment”. The color of the pigment used in seal-plug helps identify the polarity of the termination. The end-cap terminations are basically alloy-42 with gold-plating, a nickel barrier with final top solder coat.

*2) Issues for investigation:** Whether the received part quality was sub-standard, * whether the part is prone to failure under similar assembly stresses, * whether accidental assembly overstress occurred, * whether part location on the

circuit is critical and * whether there are ways and means to eliminate the event.

As per manufacturer datasheet, these capacitors are recommended be reflow soldered at temperature not greater than +250˚C for a period of not more than 30 seconds. However, hand-soldering (as per ISRO-PAX-300, 250˚C for 5 seconds) is preferred at SAC as the cards have parts with a wide variety of case-sizes, requirement of several through-hole parts and the requirement of select-on-test or need for parts-value optimisation.

These failed parts were subjected to four different tests to find out the root cause of the observed deviations from above possible causes.

*a) Test 1: Evaluation of batch quality:*Approximately 325 pieces, inclusive of both values from same batch as the failed parts, were re-inspected at 10x and a smaller sample from within this test batch inspected at 40x.

Results: No cracks or separation was observed in the black epoxy at negative termination of the device in as received condition indicating no anomaly at receipt.

*b) Test 2: Impact of Normal Fabrication (as per ISRO-PAX-300) techniques on FM components:*To evaluate parts capability to withstand normal fabrication and testing stresses, 3 parts each, for both device values were selected and soldered on cards by two qualified fabricators. Both the cards were subjected to thermal cycling (–15ºC to +55ºC, 30 minute at each extreme with transition rate 1ºC/min, 15 cycles). The cards were visually inspected on the completion of 10 and 15 cycles.

Results: No degradation was observed.

Subsequently, to accelerate the generation of any such cracks and study the long term reliability of such cards, these 2 cards were subjected to a total of 75 cycles of Accelerated thermal cycling from -55ºC to +85ºC. After completion of the test, the capacitors were visually inspected at 40x and electrically measured for any change in value. Five components from the above card have been micro-sectioned and inspected.

Results: No separation or cracking at the negative termination seal-plug (black-pigment epoxy).

c) Test 3: To simulate the condition of overstress due to soldering workmanship: Similar to the above cards, a third card was fabricated by a cer tified fabricator from other agency. However, the soldering temperatures and times were different. Subsequently, a crack in epoxy was simulated by application of soldering iron to the capacitor termination, at a temperature of 310ºC for 7 seconds.

Further experiments for soldering & re-touching were carried out on this card;It was observed that application of soldering iron with a tip temperature of 275ºC for 7 seconds, and movement of the iron-tip results in cracking of the black epoxy; in 1 out of 4 cases. Similar cracks could be simulated in 2 out of 4 capacitors after 5 seconds, only at 300ºC. However, in all 3 cases, the soldering iron- tip was not only in contact with the capacitor termination, it w as also moved while in contact with the termination.

Results: (Fig.2)

- With solder-tip temperature of 300ºC or more separation of part termination initiates.
- With solder-tip temperature nominally at 275ºC and tip movement across part termination, the deviation was developed.

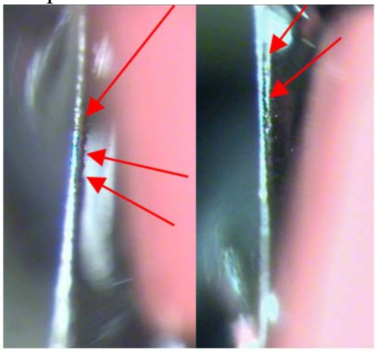

Fig. 2. separation of part termination

d) Test 4: To detect whether correlation exists between device accessibility for soldering and the defect: Layout of cards was studied, inspected and placement locations for this device type verified.

Results: Inspection of pad-placement layout for these devices revealed that,on few locations a device-pair is soldered in an end-to-end fashion or at right angles, bringing-in fabricational accessibility constraint due to pad-placement where terminations of individual devices are separated by a very small clearance, however meeting the layout guideline as per ISRO-PAS-301. Such a separation may not allow normal soldering to be accomplished, where solder-iron tip touches the junction of device-termination bottom and mounting pad. It was found that 66% of devices in these cards with this deviation reported have poor soldering accessibility.

3) *Failure Mechanism:*During the soldering operation the thermal differentials, between the closely packed materials at the negative terminal, lead to release of stress at the black-epoxy, which manifests in terms of cracking in the silver-epoxy and the black-epoxy travelling towards the top of a mounted device. The crack may not extend through to the bottom of the mounted device, as device is rigidly held at PCB due to the solder-joint at mounting-pad. The top being free of any rigid support, cracking or separation of termination under stress is aided. The same does not occur at the positive terminal as there is an empty cavity inside the end-cap that absorbs the expansion of epoxy and end-cap.

4) *Conclusion:*A combination of conditions during soldering, viz. – heating of total termination and movement of Solder –iron bit across termination area or higher Solder-iron bit temperature or all conditions together in addition to poor fabricational accessibility leads to the part failure with this signature, irrespective of value or date code or case size wherever the conditions prevail.

5) Recommendations:

- Based on the observed deviations, hand soldering procedure for this device type of parts was generated and recommended for implementation.
- Clearance available between adjacent solder location should be 5mm minimum.
- Though the recommended guidelines shall be followed, there is a probability of overstress due to human-error; hence, an alternate part type CWR09 was suggested which is different in construction (Figure-3), with no back-filled epoxy being used, the chances of getting such a deviation during hand soldering are remote.

B. Feed-through failure

Bias loading on negative Bias-lines was observed in two MMIC-based subsystems during final stage of Test and Evaluation. Investigation revealed that the feedthrough in the bias line path showed resistive short between centre pin and body. The feed-throughs were removed from box and handed over for FA. Table-I below shows the details of failed parts.

TABLE. I. FAILED PARTS DETAILS

Device type	SFC030
Value range	470 to 22000nF
Voltage rating	100V
Quantity	02
Device quality	ESCC Level B qualified

1) Failure Analysis: External visual inspection and electrical measurement was carried out on failed sample. High magnification visual on the parts did not reveal any external deviation. During electrical measurements, these two feed-throughs showed resistive short between centre pin and body and lowered Insulation resistance respectively. Failed feed throughs were micro-sectioned to detect manifested failure signature. In micro sectioning sample, crack was observed between opposite electrodes near the termination of discoidal capacitor at high magnification as shown in Fig.3.

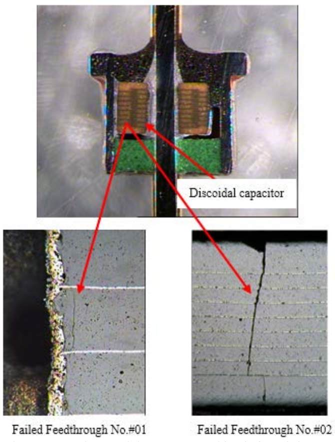

Fig.3. Micro sectioned image-Failed feedthrough

*2) Investigation:*As described above, the part failure signatures of the nature observed in MMIC based units, appear in case there are defects inherently in the bulk-ceramic of the MLCCs or that these get created during assembly. Experience at SAC with similar device type indicates that such failure can even occur in devices from batches of proven quality due to random and accidental assembly induced stresses. However, to eliminate any possibility of poor quality of device batch, two tests were carried out on devices from the same batch as that of the failed devices as details given below.

a) Test No. #01: To accelerate filamentation through inherent defects, if any, two devices were assembled on a test box with required circuit powered with1.5VDC and subjected to a temperature of 85°C for 240 h ours. Observations of initial electrical measurements as well as leakage current measurements and final measurements after 240 hours are taken.

Results:No significant deviation observed after completion of 240 hours of high-temperature bias test.

*b) Test No. #02:*To accelerate filamentation through inherent defects, if any, under combined effect of temperature, bias and humidity, three devices were assembled separately on another test box similar to previous one and subjected to 85˚C, 85% RH for 1000 hours with applied bias of 1.5V.

Results: No deviation observed after completion of 1000 hours of Biased-Temperature-Humidity test.

No signatures of either inherent bulk-defects or assembly-induced cracks were observed in any of the five devices from the same batch as failed devices.

3) Failure Mechanism:

Device construction: The part has a discoidal Multilayer ceramic capacitor (MLCC) with solder-joints at part-body and peripheral termination of the MLCC disc and at MLCC disc-center and center conductor of part. The part is sealed with potting encapsulant at one end and glass-to-metal seal at the other side (Fig.3).

The MLCC is basically made up of ceramic dielectric, which is very brittle. Any defect, like void or a crack, which can overlap the spacing, can easily lead to silver from the Ag-Pd electrodes to migrate under effect of an electric field. The electric field should be just sufficient to sustain the Ag-Pd migration within the spacing between two opposing electrodes, which is provided by voltages around 1.5VDC. In some cases, the silver-migration is aided by high relative humidity where water molecules form a vehicle for silver particles and aids the migration. Migration of Ag particles across opposite electrodes under effect of an electric field, routing through the bulk defects (voids or cracks across opposing electrodes) causes the observed resistive-short. The electrolytic migration takes place in the following way –

- 50% RH maintained in labs is sufficient to provide water molecules and present a medium for Ag+ ions to become mobile

$$Ag^{+} + OH^{-} + H^{+} \rightarrow AgOH + H^{+}.$$
$$2AgOH \rightarrow Ag_2O + H_2O.$$
$$Ag_2O + H2O \rightarrow 2OH^{-} + 2Ag^{+} \text{ (at cathode).}$$

A higher voltage applied after the silver-migration has created a resistive short-circuit, almost invariably fuses out this filamentation, making the failure symptom disappear altogether. However, the failure site exists for a recurrence of filamentation and subsequent faulty behavior of the capacitor in form of high dissipation factor or low resistance.

Thermo-mechanical stress induced during fabrication/assembly could have caused crack in bulk ceramic (between opposite electrodes) which was further resulted in to filamentation under the effect of moisture and electric field and manifested as electrical malfunction during functional testing at advance stage as described above.

4) Conclusion:

- This is an ESA qualified part and the probability of failure being due to poor quality of device batch is remote and the same was confirmed by two tests. Hence, batch quality is acceptable.
- A soldering iron held to the feedthrough terminal of for longer duration (>5sec.), causes thermo-mechanical stress induced micro cracks in the discoidal ceramic capacitor. Over a period of time, the crack aided by atmospheric moisture allows a conductive path of migrating silver particles to form a resistive short, under the low DC voltage (~1.5VDC) as observed in actual failure cases.

C. Electrical Overstress Failure-MOS driver:

Electrical overstress (EOS) is one of the most common causes of failure for an electronic part. It can either be independent of time or can be periodic or totally random and arbitrary in nature. One of the most challenging aspects of failure analysis is to determine whether a part failed from an internal defect or an external overstress. Only rarely manufacturer's specifications for microelectronic parts identify maximum transient tolerance limits for the part. The EOS from the common DC power source will cause severe destruction of the device like bond wires fusing, fusing of metallization etc. One such case study is covered below. Over all die view is shown as in Fig.4.

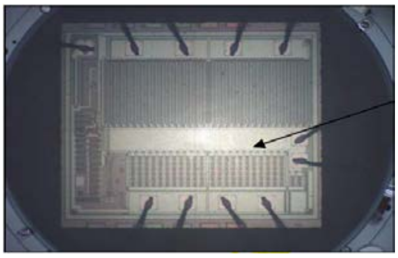

Fig.4. MOS Driver Die View

Multiple nos. of MOS Driver ICs shown in Fig.5, part type 5962-8877003 (4420A), were reported failed in Electronic Power Conditioner (EPC) during functional testing, after final SOT (select-on-test, part-value optimization) was completed at fabrication lab.All the failed devices were subjected to FA [5] [6].

1) Failure Signatures:

Visual: Drain fingers of Lower output transistor were, found fused out to varying extent, in terms of affected fingers as shown in Fig.5a (good device) and Fig.5b (failed device).

Electrical: Pin to Pin impedance measurements for Failed devices, when compared with good device on Curve tracer, showed degraded characteristics between –

- Supply pin and Output
- Output and Ground as shown in Fig.6a to 6d

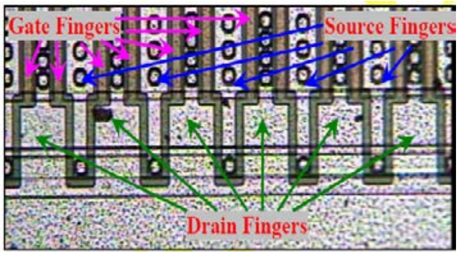

Fig.5a Finger structure of gate, drain and source fingers-Good device

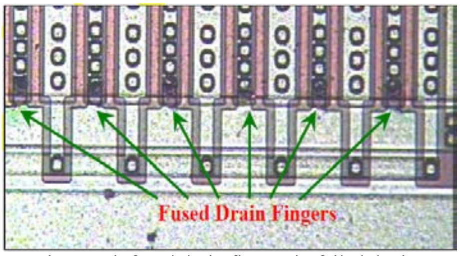

Figure: 5b fused drain fingers in failed device

Fig.6a. Vs-Out Failed Device

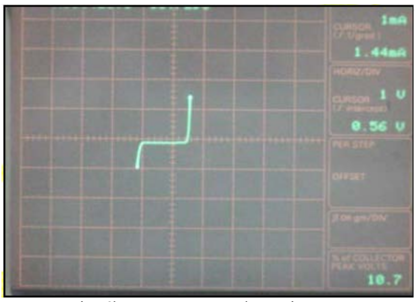

Fig.6b. Vs-Out Good Device

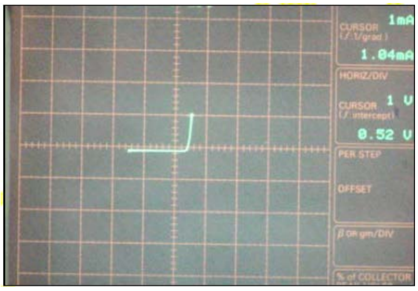

Fig.6c. Out-Gnd Failed

Fig.6d. Out-Gnd Good Device

*2) Failure Mechanism Hypothesis:*For the failed device, the impedance between Vs (+Ve, Pins 1/8) and Output (-Ve, Pins 6/7) as well as Output (Pins 6/7) and Ground (Pins 4/5) was found degraded, indicative of an excessive energy having flowed through output of the device, with lower transistor having fused out. The visual signatures indicated that the fuse-out without any discoloration was **due to short duration high-energy event**, as each finger would have required at least about 65mA or more to fuse out, as per the calculation from cross-section area of the die.

3) Possible causes:

- The device output has a pulse-transformer with MOSFETs as load on transformer secondary. Possibly the rising-edge and falling-edge spikes, depending on the magnetizing current in the transformer, caused the failure (or)
- Housekeeping turn on transients in excess of 20V, detected during investigations with full load (10A) of 100W EPC, could be the cause of failure as it is beyond maximum rated supply voltage of 18V for the device.

4) Failure Simulations:

*a) Simulation-1:*Transformers of 40 turns, 53 turns and 106 turns (with minimum magnetizing current) designed by the Payload team were used, to study the impact on device output.

Results - No degradation as in failed units was observed.

b) Simulation-2: A Pulse (21V, 5ms) similar in amplitude to the observed house-keeping turn-on transient (20.6V, 5ms, Figure-8) was generated and applied to the Vs of devices mounted in the actual configuration.

Results -The pair of devices used in this simulation failed in an identical fashion to that of actual failure (Fig.7c).

*c) Failure Mechanism:*The MOS structure which has a thin gate oxide is highly sensitive to voltage overstress. The failure process is gate-oxide (dielectric) breakdown when the transient voltage creates a field greater than the dielectric strength of the gate oxide. Electric field associated with the applied voltage accelerates electrons to an avalanche condition which produces punch through short a nd thus creates a low resistance path. The ensuing avalanche results in high current over short time duration leading to metal burning and resulting in catastrophic failure.

d) Root cause: In all probability the root cause of failure is turn on transient of housekeeping section in EPC.

*e) Recommendations:*Circuit optimisation to eliminate house-keeping turn-on transient was carried out and a transorb capable of suppressing the observed spike was incorporated in supply line. This resulted in the house-keeping turn-on transient being totally removed as shown in Fig.7a and 7b.

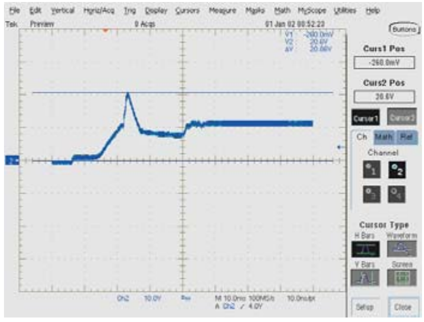
Fig.7a. House Keeping Turn ON transient (20.6V, 5ms) before optimizing the circuit

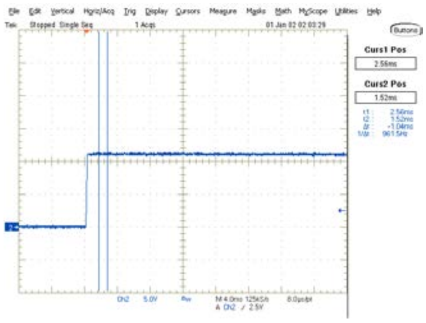
Fig.7b. House Keeping Turn ON transient (20.6V, 5ms) after optimizing the circuit-No turn ON transient

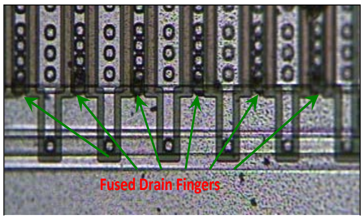

Fig.7c.Fused drain fingers in simulation device

IV. CONCLUSIONS

The FA cases above indicates thermo-mechanical overstress due to fabrication in 1st case and electrical

overstress due to transient generated in housekeeping section of EPC in 2nd case. As established for either case, the failures observed were due to overstress and necessary mechanisms were incorporated with these lessons learnt resulting in elimination of further failures.

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Gear G “MOS/LSI Failure Analysis Techniques”

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High selectivity poly silicon etching for detection of sub micron scale defects in semiconductor devices

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ABSTRACT: Detection and capturing of defects at sub micron scale in a multilayered semiconductor device are quite challenging. The whole process demands non introduction of new defects and retention of original defects. In the present work, development of high selectivity poly silicon etching using Reactive Ion Etching (RIE) System has been described. Very high selectivity of poly silicon etching with respect to silicon oxide and silicon nitride has been demonstrated. The critical process parameters such as RF Power, Gas pressure, Gas composition etc have been discussed. The process developed here is portable with little modifications from one chamber to another. Capability of high selectivity poly silicon etching has been demonstrated in capturing IBC (Insufficient Buried Contact) defects in DRAM devices. Failed DRAM devices having random distribution of single and double bit failure are suspected to have IBC problems. High selectivity poly silicon etching has been used to study impression of poly contacts over silicon substrate. IBC failures noticed in failed devices indicate successful of high selectivity poly silicon etching in capturing sub micron scale defects.

Key words: RIE, DRAM, IBC, DLCT, RF, HF, DI, SF_6, HBr, ECR

I. INTRODUCTION:

Semiconductor devices have multi layer structures. Typically there are more than ten layers embedded in top few microns. The layers consist of Polyimide, Poly silicon, Silicon nitride, Silicon oxide, Titanium nitride, Tungsten silicides, etc. Figure 1 depicts multi layer structure of a typical semiconductor device. Poly plugs are one of the common interfaces which provide structural support and electrical contact with silicon substrate. Electrical contact between poly plug and the substrate is of fundamental importance in performance of the device. Memory cells, DLCT, Metals lines, etc are connected to silicon substrate through poly plugs. Figure 2 shows cross sectional view of a typical DRAM device. Typical DRAM structure has Transistor loop, Memory Loop and Metal Loop.

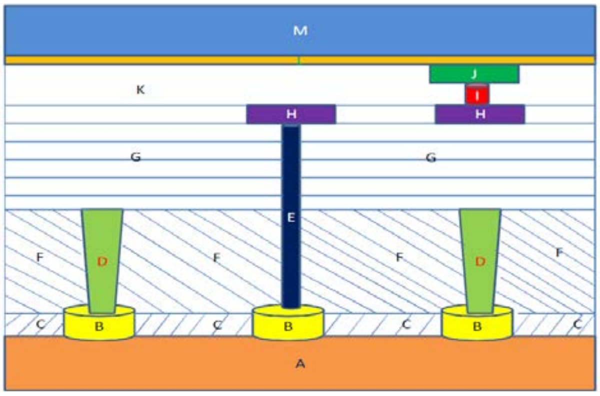

Fig.1 showing multi layer structure of a typical semiconductor device

A: Silicon substrate, B: Poly plugs supporting memory cells and DLCT, C: BPSG 1, D: Memory Cells, E: Digit Line Contacts (DLCT), F: BPSG 2; G: BPSG 3; H: M1; I: Via; J: M2; K : Passivation Layer, M: Polyimide Layer.

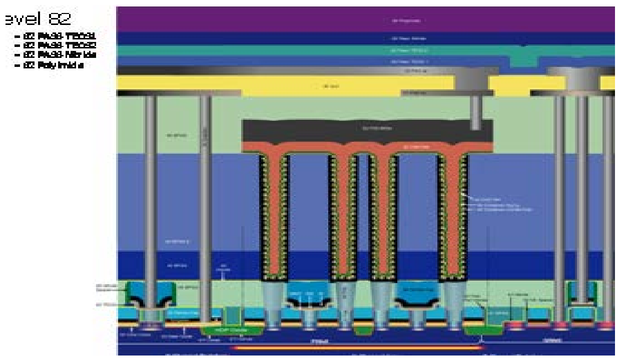

Fig-2: Cross section view of a DRAM device

II. DISCUSSIONS:

A. INSUFFICIENT BURIED CONTACT (IBC)

In order to have good electrical contact, part of the poly plug must get buried into the silicon substrate. This is achieved by dimple etch into the silicon substrate. Due to various problems associated with lithography and or plasma etching processes, the

buried contact between poly plug and the silicon substrate may not be adequately conductive. An insufficient buried contact (IBC) leads to a specific failure mode for that particular memory cells. The electrical contact between poly plug and the substrate can be good, marginal or poor as shown in the figures 3, 4 and 5 respectively.

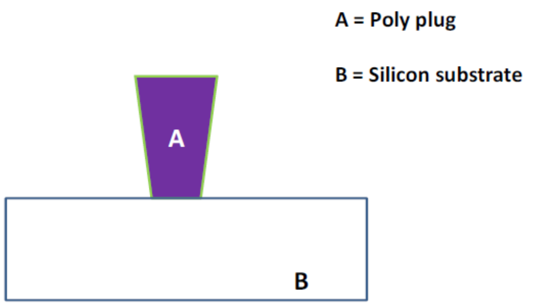

Fig-3: Good contact between poly plug and silicon substrate

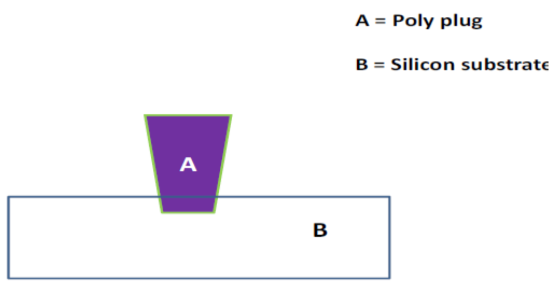

Fig-4: Marginal contact between poly plug and silicon substrate

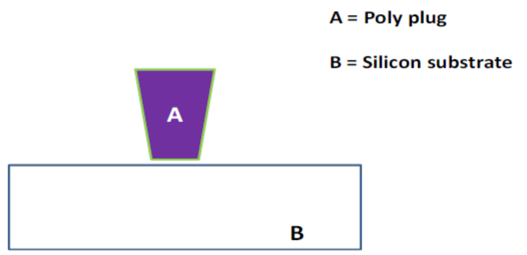

Figure-5: Poor contact (IBC) between poly plug and silicon substrate.

B. ELECTRICAL SIGNATURE

One Digit Line Contact (DLCT) controls functioning of two memory cells (Odd and Even bits). Each bit is connected to a memory cell which is basically a capacitor. Both DLCT and memory cells are connected to the silicon substrate through poly plugs. Therefore presence of IBC defects are reflected through random distribution of odd, even and double bit failures. However, IBC is one of the many reasons for this kind of electrical failure.

C. PHYSICAL FAILURE ANALYSIS:

Confirmation of the IBC defects requires careful and controlled etching of poly silicon with very high selectivity with respect to silicon oxide. The spacing between two memory cells could be 0.2 microns while height of the memory cell is typically 3 microns. Following are the key processes required in observing IBC defects.

- Removal of the polyimide layer
- Removal of the Metal 2 and Metal 1 layers
- Controlled removal of BPSG
- Removal of Tungsten (DLCT)
- High selectivity poly silicon etch to remove both combo poly and the silicon poly plug
- SEM analysis to confirm IBC failure.

Physical Failure Analysis PFA) makes use of intelligent combination of wet and dry etch methods. Following constraints have to be considered in developing methods for PFA:

- Non usage of any mask (Mask less process)
- Compatible to irregular size of the die
- Non introduction of any new defects
- Retention of original defects
- Cost effective

Figure 6 shows 3D view of memory cell. It is challenging to remove poly plate, memory cell, poly plug and yet to retain imprint of the poly plug over the silicon.

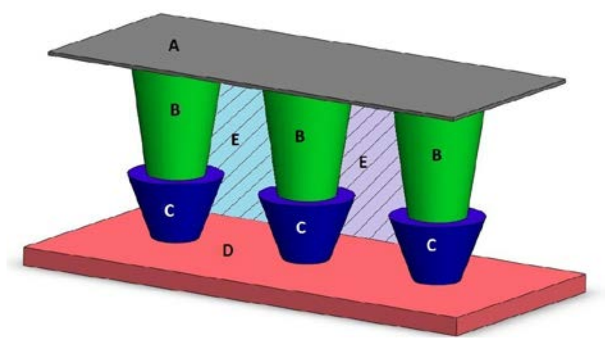

Fig-6: A Poly plate, B: Memory cell, C: poly plug, D: Silicon substrate, E: BPSG

III. EXPERIMENTAL PROCEDURE:

High selectivity poly silicon etching has been reported with dedicated systems [1-2].They are quite expensive and make use of hazardous gases such as HBr, SF_6 etc. [3].The present work shows obtaining high selectivity

poly silicon etching in a simple RIE system with less hazardous chemicals. The high selectivity poly silicon etching has been developed with CF_4, CHF_3 and O_2 [4-5]. The process developed is a dual step and key process parameters are shown in the table below:

Step 1:

RF Power	Pressure	CF_4	CHF_3	O_2	Etch Time
500 W	500 mT	40 SCCM	0 SCCM	10 SCCM	20 Second

Step 2:

RF Power	Pressure	CF4	CHF3	O2	Etch Time
60 W	180 mT	50 SCCM	5 SCCM	4 SCCM	12 Minute

Use of low RF power is quite crucial. The process etches poly silicon without etching oxide layer. An operating pressure of 180 mT allows poly to be etched selectively over oxide. An 8 % concentration of O_2 is found to be optimal to get an etch rate of 0.2 microns per minute [6]. The high selectivity poly etch is followed by 20 seconds dip in buffered HF and one minute rinse in DI water.

A. SEM ANALYSIS

De-processing is carried out on both good samples and devices suspected to have IBC signatures. SEM analysis is carried out on both the samples. Figure-7 shows good imprint of poly plug which is a measure of good electrical contact. Figure-8 shows SEM image of failed devices showing poor imprint of poly plug on the silicon.

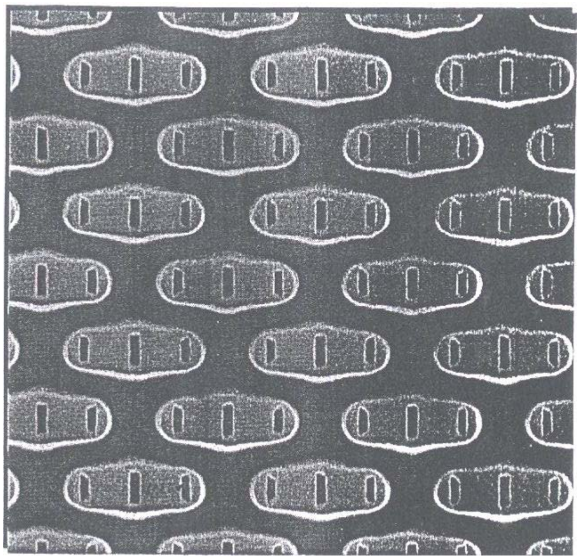

Fig-7: SEM image showing good imprint of poly plug

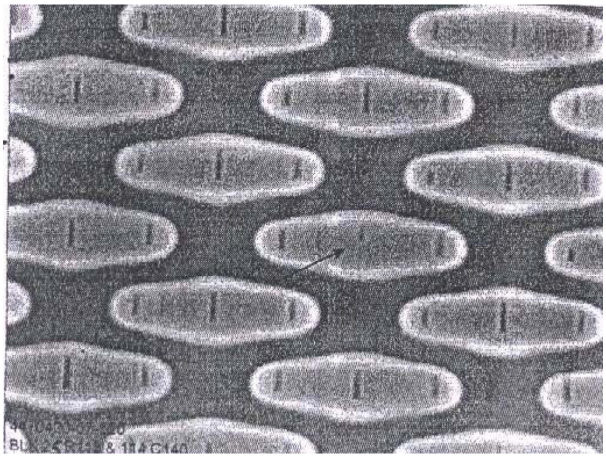

Fig-8: SEM image showing poor imprint of poly plug on the silicon.

IV. CONCLUSIONS

High selectivity poly silicon etching has been developed in a co st effective RIE system with usage of less hazardous chemicals. Effectiveness of the process is demonstrated in capturing hard to find defects such as IBC. This process can be used for effective failure analysis of EEE components by quantifying the damage created by ESD and Soft EOS related failures.

ACKNOWLEDGEMENT:

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Chip Capacitor for RF Applications & Associated Failure Mechanisms

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***Abstract*— In this article chip capacitor behaviour and its role on RF circuit performance is discussed. Theoretical equations of the equivalent circuit are detailed and correlated with the capacitor performance in RF circuits. Various types of capacitors, features, selection criteria at RF frequencies, placement methodologies are discussed. Further critical aspects associated with chip capacitor and its various failure modes are tabulated. Comparison of circuit performance at microwave frequencies using lumped approach and planar topology is also shown in this article.**

***Index Terms*— Radio-frequency (RF), capacitance, chip capacitor, failure mode**

INTRODUCTION

Hybrid microwave integrated circuit is basically employed in radio-frequency and microwave domain. Basic advantages of this approach are tunability, frequency selectivity, higher quality factor, lower parasitics, wide variety of materials and fewer losses. Hybrid circuits employ discrete surface components such as
Discrete IC devices- pin diodes, temperature sensors
Passive components- inductor, capacitor and resistor
High Q components- dielectric resonator, non-reciprocal components (isolator)
Transmission line components- power divider/combiner
Interconnections-bond wires, connectors [1]
Passive components play an important role in RF circuits which are present as inherent parasitic in the circuit or by introducing as an externally mounted element. Capacitor is the basic element in RF circuits and is employed in tuning, matching, biasing and coupling circuits. Basically at high end applications such as satellite systems the reliability of capacitor plays a pivotal role in the circuit operations compared to inductor or resistor. Planar topology and chip capacitor are the widely used capacitors at RF and microwave range of frequencies. Planar topology is basically employed at microwave frequencies due to non-availability of chip capacitors [2]. At microwave frequencies planar topology such as inter-digital topology or gap is introduced for realization of the capacitor in MIC and MIM capacitor in MMIC but the effective realized capacitance values are less along with associated low quality factor. Chip capacitor is having higher quality factor, compact size, better electrical performance and low parasitics. Present TTC transponders at S- and C-band employ large number of chip capacitors in amplifiers, multiplier chains, modulators, filters etc in the receivers and transmitters. Due to better noise characteristics of the chip capacitor applications such as VCOs, PLLs, PAs, and low level analog signal chains also employ them. These circuits are very sensitive to noise on the power supply rail which manifests itself as phase noise in the case of VCOs, PLLs and amplitude modulation of the carrier in RF power amplifiers.
Chip capacitor is basically employed at low frequency end (below 1 G Hz) and insertion in the microstrip at high frequency makes it to act like a folded transmission line with TEM mode of propagation and open at the other end behaving as a resonant circuit. Chip capacitors are not perfect and possess parasitic resistance, inductance, variable capacitance over temperature and voltage bias, and other non ideal properties. Also they are prone to failure due to voltage and current fluctuations along with thermal shock resulting in degraded performance of the system. As chip capacitor is indispensible part of the RF circuits so this article covers an overview of chip capacitor for RF applications covering various aspects such as electrical parameters, theoretical equations, comparative analysis, failure modes and mitigation of the same which will be helpful for understanding and achieving reliable operations in space environment.

CAPACITOR TYPE AND ITS EQUIVALENCE

There are many different dielectric materials used in the fabrication of capacitors, such as paper, plastic, ceramic, mica, polystyrene, polycarbonate, teflon, oil, glass, metal oxide and air. Power dissipation of the capacitor is directly related with the material property. A capacitor is the combination of inductor in series with lumped resistor as shown in Fig 1.

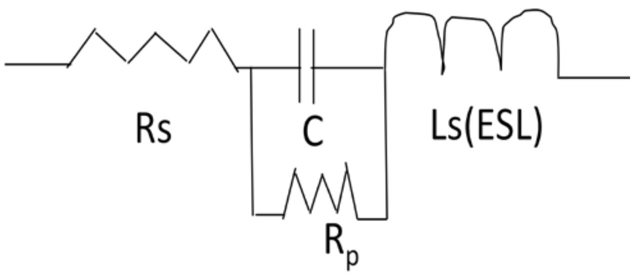

Fig1: Equivalence of chip capacitor

The overall impedance of the above can be written as

Type	ε value	Loss tangent @100MHz	Features	Applications
Low permittivity	30	0.002	NPO ceramics Excellent temp stability	Oscillator, resonant circuits, filters
Moderate permittivity	1200	0.03	Smaller in size, compa. low cost	Switching circuits
High permittivity	8000	0.1	Poor temp characteristics , higher cap. variation	Bypass

$$Z = R_s + \frac{R_p}{1+\omega^2 R_p{}^2 C^2} + j\omega(L_s - R_p C) \text{..........(1)}$$

Various theoretical equations are

$$Q = \frac{X_C}{ESR}; \tan\delta = \frac{1}{Q} \text{..(2)}$$

$$ESR = \frac{powerfactor}{\omega C}; \omega = 2\pi f$$

$$P_{diss}(W) = E^2{}_{rms} \varepsilon_r \tan\delta . f_{Hz} \times (55.5 \times 10^{-4}) \text{....(3)}$$

where P_{diss} is energy dissipated per cubic cm, E_{rms} is rf potential in volts, ε is the material dielectric constant, tan is loss tangent. ESR (effective series resistance) is the combination of resistance Rs and Rp where Rs is the heat-dissipation loss associated with dielectric and ohmic loss and Rp is the insulation resistance. ESL (effective series inductance) is due to inductance of the leads and body and in case of chip capacitor inductance due to lead is eliminated [3].

As shown in equation (1), low Q is associated with higher series resistance which results in temperature instability of the capacitor and leads to thermal runaway. The effective capacitance can be given by equation (4) taking into consideration of capacitor variation over temperature, tolerance and voltage.

$$C_{eff} = C_V(1 - C_{\Delta T}) \times (1 - T) \text{..(4)}$$

where C_v is the effective capacitance at bias voltage, $C_{\Delta T}$ is the capacitance variation with temperature and T is the component tolerances. The capacitance temperature can be expressed as the function of various parameters as shown below:

$$T_{cap} = f(T_A) + f(T_{diss} + T_Q) + f(T_{LOC}) - f(CR)$$

where T_A ambient capacitance, T_{diss} capacitance due to its own power dissipation, T_{LOC} temperature contribution to capacitor due to local heat intensity, T_Q temperature rise due to degradation of Q,CR cooling rate [4].The magnitude of the ESL and ESR depends on the configuration of the capacitor (chip,disc etc), the material (ceramic,mica, porcelain) and the methodology (multilayer,stacking). Capacitor losses are represented by dissipation factor (tanδ) and high value of the same results in higher series resistance, poor quality factor and higher noise characteristics. Dissipation factor is dependent on the frequency and temperature and higher frequency leads to higher losses. Various types of capacitors and corresponding features are shown in Table-1.

Table-1: Various capacitor types and their features

Mostly multilayer ceramic capacitors (MLCC) are used in RF as they combine small size, low effective series resistance and inductance (ESR and ESL) as well as can operate at wide temperature ranges. It has the smallest footprint and is cost effective for wide range of applications. Also they are having quality factor of 1000, series resistance around 0.01Ω, power dissipation of 0.02 W which is one order below than standard capacitor.

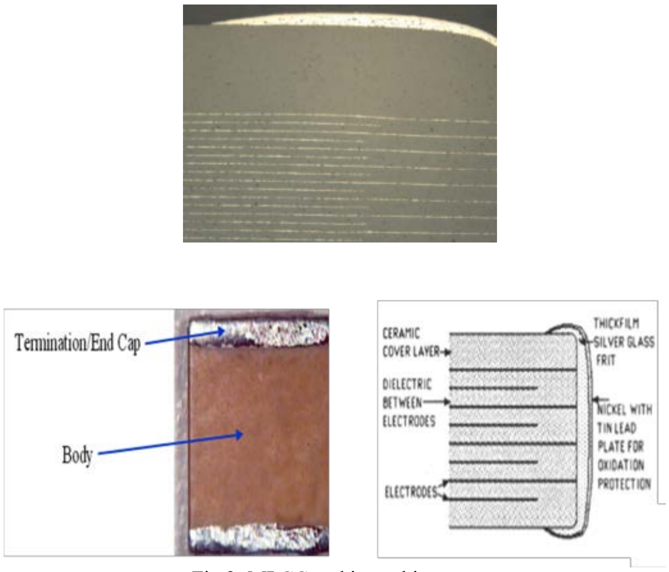

Fig 2: MLCC and its architecture

MLCC construction as shown in Fig 2 is manufactured by two processes namely dry sheet and wet build up. The termination is silver palladium alloy frit with nickel barrier layer and tin over plating. The generic electrical parameters are insulation resistance, overvoltage, capacitance and dissipation factor (loss tangent).

CAPACITOR AT RF FREQUENCIES

I. Chip capacitor to be designed especially for RF frequencies having minimum insertion loss. Selection of the chip capacitor is based on low inductance, low series resistance, high-Q, low power dissipation and presently capacitors employed in satellite based applications are CWR,CDR,CLR,CKR,CRH,JMC and PC 32T types. Improper choice or selection leads to power as well as gain loss per stage resulting in poor circuit efficiency. Mostly CDR capacitor is employed at the input and output of S- and C-band circuits having the coupling capacitor in the range

of 10-20 pF resulting in minimum resistance to the high radio frequency whereas biasing circuit is having CWR capacitor having higher ranges so as to short low frequency components. The major parameters at RF frequencies are: VSWR, insertion loss and series resonance frequency. The power dissipation in chip capacitor is directly proportional to the dissipation factor. As there is considerable amount of internal heat generation in the standard dielectric materials due to large current associated with the circuits so it is necessary to employ special dielectric material having less loss at higher frequencies [5]. Ceramic capacitors are classified as low ε, moderate ε, high ε and possesses temperature compensating performance by employing NPO (negative positive zero) dielectric as shown in Table-2.

II. Table-2: Various types and features of MLCC

High-ε ceramic capacitors are having poor temperature characteristics and their capacitance may vary as much as 80% over various temperature ranges. With the reduction of ε they suffer from higher aging rate due to relaxation of the microcrystalline structure that causes capacitance loss with time. They are used only in bypass applications at radio frequencies. Fig3 shows the placement of chip component (CDR) in the two stage amplifier circuit at S-band.

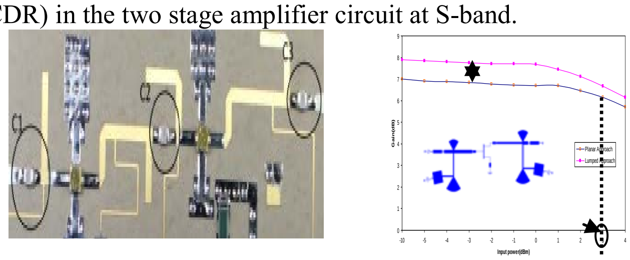

Fig3: Chip capacitor mounted in microwave circuit & performance comparison at Ku-band

Performance comparison at Fig 3 clearly indicates that chip capacitor improves the circuit gain compared to planar approach due to less losses associated with it. Another aspect at radio frequency is the associated resonance behaviour shown by the lumped elements. As shown in Table-3, a 1 00 pF capacitor changes its value with the increasing frequency and after resonance frequency it behaves as an inductor.

Frequency (MHz)	Equivalent Value
20	99 pF
40	103 pF
80	112 pF
120	133 pF
160	181 pF
200	318 pF
240	**Short**
280	1.14 nH
320	1.89 nH

Table-3 Typical frequency response of chip capacitor

The above example shows that particular chip can be employed only below 240 MHz.

FAILURE MODE

There are three types of typical failure modes in multilayer ceramic capacitors; electrical shorts or low resistance, open circuits failure, and finally capacitance value being out-of-tolerance. Voids, microcracks, delaminations, impurities in the ceramic, migration of external electrode materials, contamination on the ceramic surface and solder interconnect can attribute to capacitor failure. Table-4 shows the overview of the failure causes and possible indications.

Table-4: Overview of causes and sources of failure

Failure Causes	Sources	Indications	Remarks
Electrical Overstress : Current/Voltage	Poor design, Component selection	Self heating, Increase current, Discoloration, Micro-cracking, Dielectric breakdown /puncture	Lower loss dielectric, Higher rated component
Mechanical Stress	Component placement/centring, Impact damage to PCB, Shock or pot reflow	Damage to body, cracking in ceramic	PCB routing, placement pressure
Thermal Stress	Hard soldering, PCB rework, Forced cooling /quenching Soldering processes	Cracking in ceramic, leaching of terminal/metallization	Reduce heating/cooling rate
Intrinsic defect	Ceramic contamination, Improper pressing/sintering	Porosity/voids in ceramic, cracks	Material control/clean room contamination, Sintering control
Ionic/metal conduction	Flux residues, sealers, ext sources	Corrosion	Alternative materials

Higher current and surge voltages can cause high temperature and intense heating in the circuit. This degrade the component quality factor (Q) value of the chip capacitor which is dependent on the RF current level, ambient temperature, mounting method, heat removal rate and thermal resistance. The loss tangent of the chip capacitor

also increases with the frequency as its capacitance value decreases. Degradation of loss tangent (dissipation factor) causes increased dissipation losses resulting in temperature rise of the circuit. This raised temperature in the RF card along with high current causes drastic change in the capacitance value which results in degraded circuit performance such as low gain, oscillations, raised noise floor, poor mismatch etc.

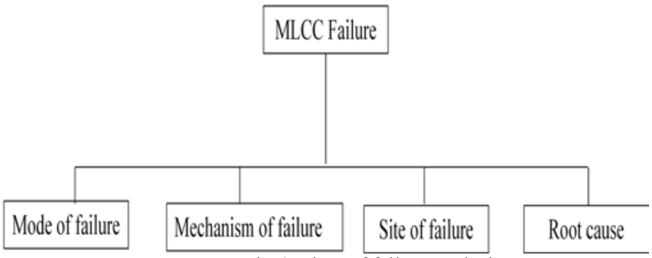

Fig 4: Flow of failure analysis

The root cause of failures can be attributed to various phenomena such as:

- discharge or breakdown due to excessive voltage across the capacitor;
- heating due to ohmic effects;
- heating due to loss within the dielectric .

Failures can be analyzed using optical microscopy, scan electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX). XRD analysis can be useful in finding out the inter-metallic compounds in case of delamination.

A.Mitigation of Failure

Multi-layer ceramic chip (MLCC) capacitors are prone to failure due to sudden changes in temperature to which they may be subjected such as thermal shocks due to TCE (temperature coefficient of expansion). H igh soldering temperatures or mechanical shocks cause microcracks leading to the capacitor failure. Microcracks can absorb moisture and cause short-circuits under some conditions. Such mechanical shocks can also be caused by PCB flexure induced stress, while mounting capacitors close to points of mechanical stress. This can be prevented by using a lower soldering temperature, and a smaller rate of temperature rise in reflow soldering, so that thermal shocks are avoided. Some chip capacitor needs pre heating before carrying out soldering so as to avoid thermal shocks. The HTHH test can be part of the screening process to accelerate this phenomenon [6]. Using high-quality materials and dielectric-manufacturing processes can minimise defects leading to a s lower rate of self-healing. O perating life of MLCC capacitor can be calculated using the formulae by Moglevesky and Shin as shown below:

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^3 \exp\frac{E_a}{k_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

where t is time, V is voltage, T is temperature in K, E_a is the activation energy, k_B is Boltzmann constant (8.62 x 10^{-5} eV/K). The main aspects to be considered for high reliable operations of the chip capacitor are: mounting and placement methodology, rating, frequency of operations and dissipation factor. In overall system level the loading effect enhanced overall current and increasing the rated value provide the desired circuit performance.

DISCUSSIONS

Role and choice of chip capacitor is very important in RF circuit and are preferred over planar topology for biasing and coupling operations. RF circuit performance such as gain, output power, efficiency and bandwidth is directly linked with the chip capacitor performance and employing chip capacitor with low loss dielectric results in improvement in gain and efficiency. Multilayer ceramic capacitors (MLCs) are being widely used in large scale manufacturing for the miniaturized circuits. Choosing the wrong capacitor can lead to circuit instability, excessive noise or power dissipation, shortened product life or unpredictable circuit behaviour. The choice of chip capacitor is dependent on various factors and applications. Further circuit performance depends on t he reliability of chip capacitor and parallel combinations to be incorporated to avoid catastrophic failure. Authors believe that this article will help in better understanding the role of chip capacitor in RF domain and will help RF designer in optimizing design with prior knowledge of various failure modes.

ACKNOWLEDGMENT

Authors are thankful to Director and Deputy Director ISAC for their constant support and encouragement.

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Radiation characterization of in-house DC-DC Converter

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***Abstract** - DC-DC Converters are used for power conditioning and distribution in satellite power systems which convert variable Input Voltage from solar array and battery to multiple regulated DC Voltages as per sub-system requirements. DC-DC Converters are preferred over linear regulators as they can be switched at higher frequency, have better efficiency, reduced size & weight and improved thermal management.*

Many types of DC-DC Converters with different wattages are being built in-house and Radiation hardness Assurance of these Converters is a challenging task. To assess the survivability of Components in space radiation environment, devices need to be radiation characterized with respect to TID (Total Ionizing Dose) and SEE (Single Event Effects). Since bipolar technology is susceptible to low dose rate, ELDRS (Enhanced Low Dose Rate Sensitivity) testing also has to be performed.

In-house designed and developed 30W DC-DC Converters are configured with a fixed frequency, single ended, forward topology, incorporating magnetic feedback and an internal EMI filter. This Converter has triple Outputs (+5V, ±15V) with a DC Input Voltage range of 26V-43V.

A radiation characterization plan was evolved to assess the performance of In-house designed and developed 30W DC-DC Converters in space radiation environment. The plan consisted of subjecting the part to ELDRS and SEE tests. ELDRS testing of these converters was performed up to 100krad at in-house radiation test facility. SEE testing of these converters was carried out at IUAC, New Delhi and proton testing for displacement damage. at TIFR Mumbai. This paper deals with the details of the tests carried out and the results are summarized.

Keywords-TID Total Ionizing Dose, SEE Single Event Effect, ELDRS Enhanced Low Dose Rate Sensitivity, RHA Radiation Hardness Assurance

I. INTRODUCTION

Space Radiation particles such as protons, electrons and heavy ions interact with EEE devices thereby creating electron-hole pairs in the component oxide layers. This generates oxide traps and interface defects due to which the component experiences changes in electrical parameters ultimately leading to failure. This damaging effect called the Total Ionizing Dose (TID) effect, is one of the most serious effects caused by space radiation on EEE Components and poses a grave threat for any space mission. Many bipolar linear circuits exhibit a "true" dose rate effect that is commonly called as Enhanced Low Dose Rate Sensitivity (ELDRS). ELDRS is characterized by a low dose rate enhancement factor that is the ratio of the parametric degradation at a low dose rate to the degradation at a high dose rate for a fixed dose.

The space environment [6] of the Low Earth Orbit (LEO) and the Geo-stationary Earth Orbit (GEO) contain high energy particulate radiations at energy levels of a few to hundreds of millions electron volts. As a result components used in various sub-systems of the spacecraft get exposed to these particulate radiations. When high-energy particles impinge on the semiconductor microcircuits, Single Event Effects (SEE) like Single Event Upset (SEU), Single Event Transient (SET), Single Event Latch up (SEL), Single Event Gate Rupture (SEGR), Single Hard Error (SHE) are observed in semiconductor microcircuits. When charge is deposited in a sensitive volume of the circuit by an incident energetic particle and Collection of charge at the stuck node leads to degradation or mal-function of the device.

Radiation Hardness Assurance (RHA) is the aspect of Product Assurance that consists of all activities undertaken to ensure that the electronics and materials of a space system perform to their design specifications after exposure to the space radiation environment. As part of the Radiation Hardness Assurance (RHA) requirement of electronic parts for space applications the survivability of components in Space radiation Environment has to be assessed for (TID) and Single Event Effects (SEE). A radiation characterization plan was evolved to assess the performance of the in-house 30W DC-DC Converter in space radiation environment. The plan consisted of subjecting the part to ELDRS as Bipolar Technology is susceptible to Low Dose Rate, and Single Event Effects (SEE) tests. This report gives the details of Total Ionizing Dose (TID) and Single Event Effects (SEE) tests and results of the device.

Device Description

The HD3011T [3][4] is in-house designed and developed 30W DC/DC Converter. The HD30XXT series are DC/DC converters with triple outputs. The converters are configured with a fixed frequency single ended forward topology incorporating magnetic feedback and an internal EMI filter. Synchronization input/output allow these converters to operate in a SYNC mode with master converter or an external clock. The output voltages can be trimmed can to suit user requirements up to certain limits. The auxiliary can be made available with fully regulated outputs. Higher efficiency can be achieved with cross regulated auxiliary outputs. The pin configuration and pin functions are shown in fig 1a and fig 1b respectively. T he device internal construction is shown in fig 1c.

Features

- Built-in EMI Filter, Converter meets MIL-STD-461C/ISAC Standards
- Dimension – 3.5” x 3.5” x 0.65 inches
- Magnetically Coupled Feedback
- 26V to 43V DC Input Range
- Up to 30W Output Power
- Triple Output with various settings
- Efficiency > 70%
- 100MΩ@ 500VDC Isolation
- Under-Voltage Lockout
- Overload Protection
- Synchronization Input and Output
- Input Current Telemetry Output
- Inhibit Input Provided
- 250 kHz operation
- Output Voltage accuracy: Mains: 2% ; Aux:2%
- Output Current: Mains: 3A ; Aux: 500mA
- Line Regulation: Mains: 1%; Aux: 1.5%
- Load Regulation: Mains: 1.2%; Aux: 1.5%

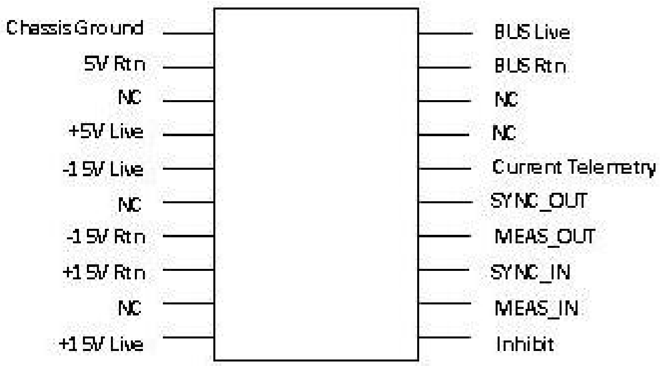


Fig 1a. HD3011T Pin Configuration

Pin no	Pin name
1	Chassis Ground
2	5V Rtn
3	NC
4	+5V Live
5	-15Live
6	NC
7	-15V Rtn
8	+15V Rtn
9	NC
10	+15V Live
11	Inhibit
12	MEAS_IN
13	SYNC_IN
14	MEAS_OUT
15	SYNC_OUT
16	Current Telemetry
17	NC
18	NC
19	BUS Rtn
20	BUS Live

Fig 1b. Pin Functions

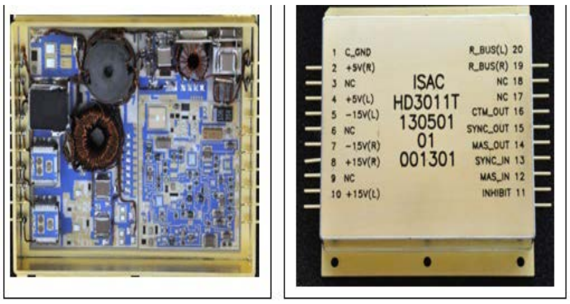


Fig 1c. HD3011T Internal construction

II. EXPERIMENTAL DETAILS

ELDRS Test

Sample size: One Converter (Sl. no 144301/03) was subjected to TID at Dose rate of 56 mrads/sec. Sl. no 144301/01 was maintained as control sample.

Test Facility: Radiation testing was conducted using Gamma chamber GC-5000 at ISITE, which uses Cobalt 60(Co-60) as the radiation source. The dose rate of the source was 56mrads/sec. Testing was done as per MIL-STD-883 test method 1019.9 condition D. [1]

Test Procedure: The Converter was mounted on Heat sink and biased with a nominal input voltage of 35 Volts The device outputs are connected to Resistive loads of value 12.5 ohms (R1) on the main line (+5V) and 250 ohms each (R2 & R3) on the Aux line. The test setup during irradiation and Biasing circuit are shown in Fig 2 & Fig 3 respectively. The Converter was irradiated in steps up-to accumulated dose of 100krad (Si) and electrical performance monitored after each step. Electrical measurement was carried out within 30 mins after irradiation.

Electrical Characterization: Electrical testing was carried out after each exposure using electronic load. With fixed Input voltages, the Output Voltages and input currents were monitored. The Output Voltages were measured at two load conditions i.e

.

- Minimum load - 10% of maximum load on the mains and Auxiliary outputs respectively.
- Maximum load - 3A and 500 mA on the mains and Auxiliary outputs respectively.

Output voltages were measured at three input voltages - 26V (minimum), 35V (nominal) and 43V (maximum). All irradiations and measurements were performed at room temperature (25°C). Case temperature of the Converter was continuously monitored during Radiation test. Setup used for Electrical characterization is given in Figure 4.

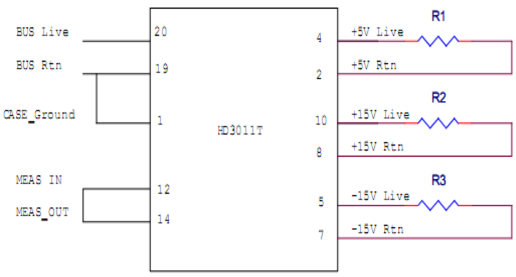


Fig 3: Biasing circuit for ELDRS test

Fig 2: Setup during irradiation

Figure 4: Setup used for Electrical characterization

SEE Test

Sample size: One sample serial no. 152703/09 was subjected to SEE test. Serial no. 144301/01 was used as control sample.

Test Facility: General Purpose Scattering chamber (GPSC) [6] [7] of the pelletron facility at Inter University Accelerator Centre (IUAC) at New Delhi as shown in fig 5. is used for SEE characterization. A direct heavy ion beam produces very high flux in the range of 10^8-10^9 ions/cms^{2}per second where as the requirement as per test method ASTM 1192 is the total fluence of 10^6 ions. As the beam current in the Pelletron facility cannot be controlled and to obtain a very low level of flux, a gold foil of the thickness330nm is placed across the beam path to scatter the direct beam. A low flux chamber

is connected to 15° port of the main GPSC chamber. Before irradiating the heavy ion flux is measured using the surface barrier detector (SBD) and the beam current is adjusted to ensure that the flux fall in the required range of 10^2 -10^3ions/cm^2/sec. Subsequently the DUT is placed in low flux chamber for irradiation. The signals from the DUT are terminated to the 50 pin feed through connector. The test and measure equipment are kept near the low flux chamber.
The Single Event Effects applicable to H D3011T are mainly Single Event transients (SET) and Single Event Latch-up (SEL). SEE test was conducted with heavy ion beams of S ilver (Ag) and Nickel(Ni). SEE test facility is shown in Fig 6.

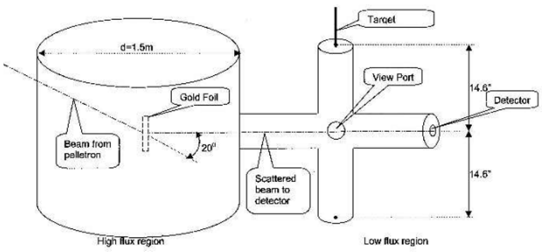


Fig 5. GPSC Chamber for SEE Studies with heavy ions[6]

The following Table presents the corresponding energies and particle flux obtained.

Ion	Energy	LET (MeV cm^2/mg)	Flux (No. of particles/cm^2/s)	Fluence
Ag^{3+}	140 MeV	50	505	10E^6
Ni^{3+}	140 MeV	32	1000	

Test Procedure:

The device was biased with a nominal input voltage of 35 Volts The device outputs are connected to Resistive loads of value are R1=8.33Ω (Main), R2 & R3=150Ω each (Aux).[2]
A decapped device with harness for SEE test is shown in fig 7. Biasing circuit is shown in fig 8. The device outputs are monitored through oscilloscope for SET and the device Input current is monitored for SEL event with a resolution of 100mV, 500nsec pulse and a current of 1 mA.

SEE Results:
No SET or SEL was observed during irradiation of Nickel and Silver ion beams.

Fig 6. SEE test facility at IUAC, New Delhi

Fig 7: Decapped device with harness for SEE test

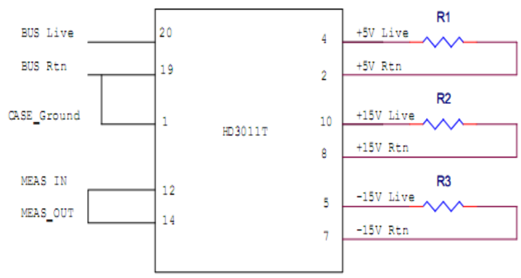


Fig 8: Biasing circuit for SEE test

Proton Test

Sample size: One sample serial no. 152703/07 was subjected to Proton test. Serial no. 144301/01 was used as control sample.

Test Facility: The Pelletron facility at Tata Institute of Fundamental Research (TIFR) Mumbai was used for conducting the Displacement damage test [5]. A proton beam of energy 22 MeV and flux $1x10^9$ protons/cm^2/s was obtained at the Pelletron Facility, TIFR. The samples were positioned at right angle to the direction of beam as shown in Fig 8.

Test Procedure: Using the concept of Displacement Damage Equivalent Fluence (DDEF), it was estimated that for a 22 M eV proton beam, a fluence of around $1x10^{11}$ protons/cm^2 is required to create the same displacement damage effect as is experienced by an electronic component in a typical geostationary spacecraft mission of ISRO for a mission life of 15 years. The fluence requirements for other missions such as low earth orbit, interplanetary etc. is lower than $1x10^{11}$ protons/cm^2. Hence the fluence level of $1x10^{11}$ protons/cm^2 was selected as a qualifying level for on-board usage of the tested devices in various ISRO missions. Also it was decided to test the samples post fluence level of $5x10^{11}$ protons/cm^2 to determine if sufficient design margin is available. Hence the test samples were exposed to proton beam in steps to achieve the following fluence levels:

a. 1 x 10^{10} protons/cm^2
b. 1 x 10^{11} protons/cm^2
c. 5 x 10^{11} protons/cm^2

The test setup is shown in fig 9. The device was biased with a nominal input voltage of 35 Volts. The outputs are connected to Resistive loads of value are R1=8.33Ω, R2=150Ω and R2=150Ω. Shows Biasing circuit is shown in fig 10.

Electrical Characterization: Five elements within the Converter were identified which are sensitive to Proton Irradiation. Electrical measurements were carried out after each five points exposure. With fixed Input voltages, the Output Voltages and input currents were monitored. The Output Voltages were measured at two load conditions i.e.

- Minimum load - 20% of maximum load on the mains and Auxiliary outputs respectively.
- Maximum load - 3A and 500 mA on the mains and Auxiliary outputs respectively.

Output voltages were measured at three input voltages - 26V (minimum), 35V (nominal) and
43V(maximum). All irradiations and measurements were performed at room temperature (25^{o}C).

Fig 8. Pelletron facility at TIFR, Mumbai

Fig 9. Test setup at TIFR

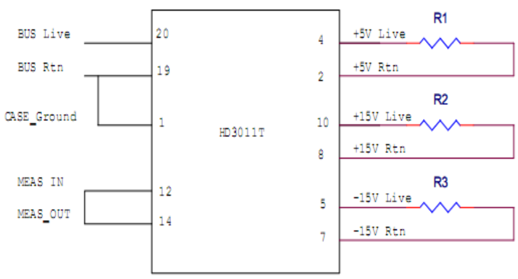


Fig 10: Biasing circuit for Proton test

III. Test Results

ELDRS Test Results:

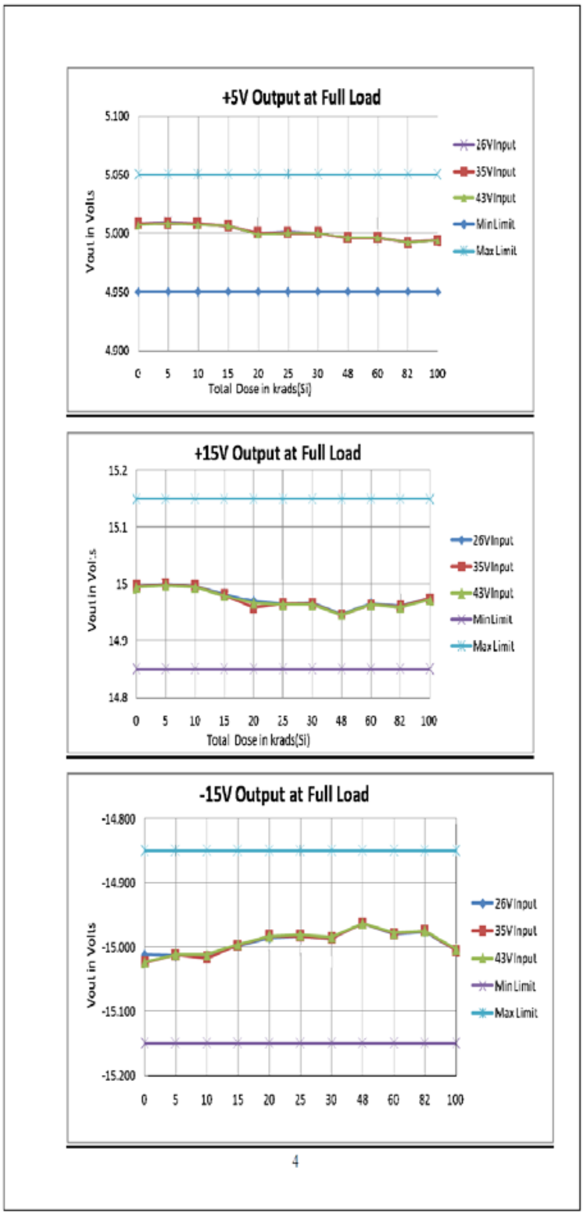
Maximum Load Condition												
Total Dose krad(Si)	**Iin(mA)**			**Vout(M)**			**Vout(+15)**			**Vout(-15)**		
	V_{in} 26V	V_{in} 35V	V_{in} 43V	V_{in} 26V	V_{in} 35V	V_{in} 43V	V_{in} 26V	V_{in} 35V	V_{in} 43V	V_{in} 26V	V_{in} 35V	V_{in} 43V
0krad(Si)	1.521	1.131	0.928	5.008	5.008	5.007	14.996	14.996	14.994	-15.012	-15.024	-15.023
5krad(Si)	1.535	1.137	0.931	5.009	5.008	5.008	14.999	14.998	14.997	-15.013	-15.012	-15.011
10krad(Si)	1.533	1.137	0.931	5.008	5.008	5.007	14.996	14.996	14.994	-15.013	-15.017	-15.012
15krad(Si)	1.538	1.142	0.933	5.006	5.006	5.006	14.982	14.98	14.979	-14.998	-14.997	-14.996
20krad(Si)	1.541	1.142	0.936	5.000	5.000	4.999	14.970	14.96	14.966	-14.985	-14.983	-14.983
25krad(Si)	1.538	1.142	0.936	5.001	5.000	5.000	14.965	14.964	14.963	-14.983	-14.983	-14.981
30krad(Si)	1.538	1.142	0.936	5.000	5.000	5.000	14.966	14.965	14.963	-14.986	-14.986	-14.984
48krad(Si)	1.534	1.144	0.936	4.996	4.996	4.996	14.947	14.946	14.946	-14.963	-14.963	-14.963
60krad(Si)	1.541	1.144	0.936	4.996	4.996	4.996	14.965	14.963	14.963	-14.980	-14.979	-14.978
82krad(Si)	1.543	1.147	0.939	4.992	4.992	4.992	14.961	14.96	14.959	-14.976	-14.975	-14.975
100krad(Si)	1.543	1.147	0.939	4.994	4.994	4.994	14.975	14.974	14.972	-15.005	-15.005	-15.003

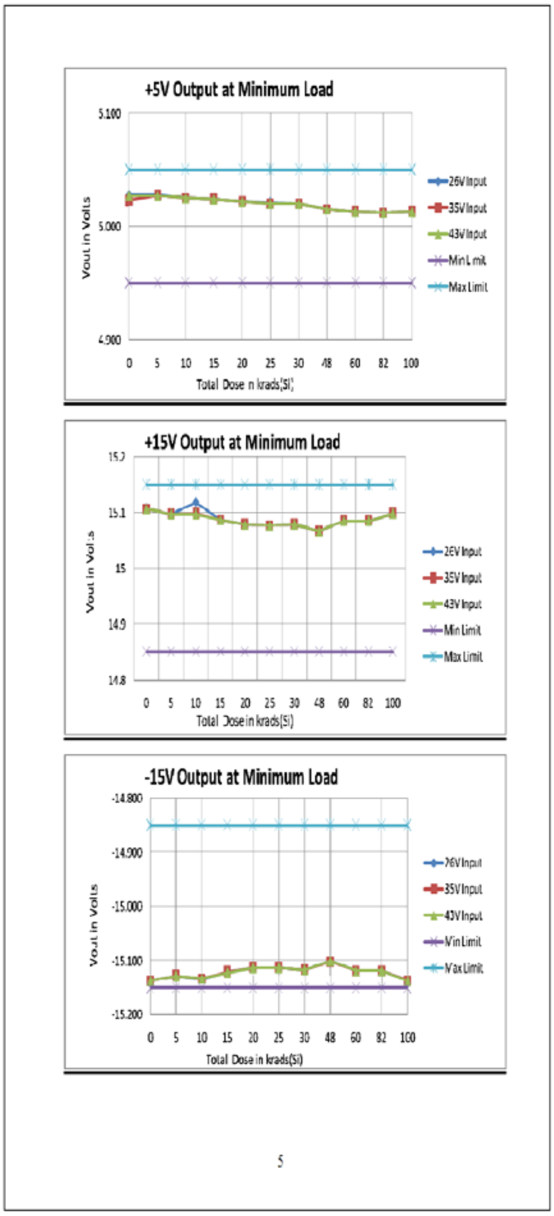
Minimum Load Condition												
Total Dose krad(Si)	**Iin(mA)**			**Vout(M)**			**Vout(+15)**			**Vout(-15)**		
	V_{in} 26V	V_{in} 35V	V_{in} 43V	V_{in} 26V	V_{in} 35V	V_{in} 43V	V_{in} 26V	V_{in} 35V	V_{in} 43V	V_{in} 26V	V_{in} 35V	V_{in} 43V
0krad(Si)	0.203	0.162	0.138	5.028	5.023	5.027	15.108	15.107	15.107	-15.137	-15.137	-15.137
5krad(Si)	0.203	0.159	0.138	5.028	5.027	5.027	15.098	15.098	15.098	-15.129	-15.129	-15.129
10krad(Si)	0.203	0.159	0.138	5.025	5.025	5.025	15.119	15.099	15.098	-15.134	-15.133	-15.133
15krad(Si)	0.203	0.159	0.138	5.024	5.024	5.024	15.087	15.087	15.087	-15.121	-15.121	-15.122
20krad(Si)	0.203	0.159	0.138	5.022	5.022	5.022	15.079	15.079	15.079	-15.113	-15.113	-15.113
25krad(Si)	0.201	0.159	0.136	5.021	5.02	5.020	15.077	15.077	15.077	-15.113	-15.113	-15.113
30krad(Si)	0.203	0.159	0.136	5.020	5.02	5.020	15.079	15.079	15.079	-15.117	-15.117	-15.117
48krad(Si)	0.201	0.159	0.136	5.015	5.015	5.015	15.067	15.067	15.067	-15.101	-15.102	-15.101
60krad(Si)	0.203	0.159	0.138	5.013	5.013	5.013	15.085	15.085	15.085	-15.119	-15.119	-15.119
82krad(Si)	0.201	0.157	0.136	5.012	5.012	5.012	15.085	15.085	15.085	-15.119	-15.119	-15.119
100krad(Si)	0.201	0.157	0.136	5.013	5.013	5.013	15.099	15.099	15.099	-15.137	-15.137	-15.138

ELDRS Test Summary

Parameter		Total Ionising Dose		Delta
		0krad(Si)	100krad(Si)	
Output Voltage (V) max load @ mains	Vin = 26V	5.008	4.994	0.28%
	Vin = 35V	5.008	4.994	0.28%
	Vin = 43V	5.007	4.994	0.26%
Output Voltage (V) max load @ Aux +	Vin = 26V	14.996	14.975	0.14%
	Vin = 35V	14.996	14.974	0.14%
	Vin = 43V	14.994	14.972	0.14%
Output Voltage (V) max load @ Aux -	Vin = 26V	-15.012	-15.005	0.04%
	Vin = 35V	-15.024	-15.005	0.12%
	Vin = 43V	-15.023	-15.003	0.12%
Output Voltage (V) min load @ mains	Vin = 26V	5.028	5.013	0.30%
	Vin = 35V	5.023	5.013	0.20%
	Vin = 43V	5.027	5.013	0.28%
Output Voltage (V) min load @ Aux +	Vin = 26V	15.108	15.099	0.06%
	Vin = 35V	15.107	15.099	0.05%
	Vin = 43V	15.107	15.099	0.05%
Output Voltage (V) Min load @ Aux -	Vin = 26V	-15.137	-15.137	0%
	Vin = 35V	-15.137	-15.137	0%
	Vin = 43V	-15.137	-15.138	0.01%
Line regulation (max load)	Main	0.019%	0%	0.019%
	Aux +	0.013%	0.02%	0.007%
	Aux -	0.073%	0.013%	0.0 6%
Load regulation	Main	0.29%	0.0038%	0.286%
	Aux +	0.74%	0.834%	0.094%
	Aux -	0.75%	0.879%	0.129%
Input Current Max load (A)	Vin = 26V	1.521	1.543	22mA
	Vin = 35V	1.131	1.147	16mA
	Vin = 43V	0.928	0.939	11mA
Input Current Min load (A)	Vin = 26V	0.203	0.201	2mA
	Vin = 35V	0.162	0.157	5mA
	Vin = 43V	0.138	0.136	2mA

All the electrical parameters are well within the device specification limits after irradiation up to 100krads (Si). The variations of Output Voltages are represented in graphs as shown below:





SEE Test Results

Device type	Ion	LET (MeVcm^2/mg)	Flux (No. of particles/cm^2/s)	Fluence	Results
HD3011T	Silver	50	505	10E^6	No transients or latch-up (SET/SEL) observed
	Nickel	32	1000	10E^6	

Proton Test Results

Parameter		Total Ionizing Dose (Fluence in protons/cm^2)				Delta
		Pre Meas	$1x10^{10}$	$1x10^{11}$	$5x10^{11}$	
Output Voltage (V) max load @ mains	Vin = 26V	5.039	5.038	5.024	5.014	0.5%
	Vin = 35V	5.039	5.038	5.023	5.014	0.5%
	Vin = 43V	5.039	5.038	5.023	5.014	0.5%
Output Voltage (V) max load @ Aux +	Vin = 26V	14.991	14.993	14.876	14.877	0.76%
	Vin = 35V	14.988	14.991	14.878	14.874	0.76%
	Vin = 43V	14.988	14.990	14.877	14.872	0.77%
Output Voltage (V) max load @ Aux -	Vin = 26V	-15.019	-15.021	-15.020	-14.990	0.19%
	Vin = 35V	-15.018	-15.020	-15.020	-14.988	0.2%
	Vin = 43V	-15.017	-15.019	-15.020	-14.986	0.21%
Output Voltage (V) min load @ mains	Vin = 26V	5.066	5.064	5.051	5.041	0.49%
	Vin = 35V	5.066	5.064	5.051	5.041	0.49%
	Vin = 43V	5.066	5.064	5.051	5.041	0.49%
Output Voltage (V) min load @ Aux +	Vin = 26V	15.101	15.112	15.017	15.019	0.54%
	Vin = 35V	15.101	15.112	15.018	15.019	0.54%
	Vin = 43V	15.101	15.112	15.018	15.019	0.54%
Output Voltage (V) Min load @ Aux -	Vin = 26V	-15.135	-15.139	-15.139	-15.122	0.08%
	Vin = 35V	-15.135	-15.139	-15.139	-15.122	0.08%
	Vin = 43V	-15.135	-15.139	-15.139	-15.122	0.08%
Line regulation (max load)	Main	0%	0%	0.019%	0%	0.019%
	Aux +	0.02%	0.02	0.006%	0.03%	0.03%
	Aux -	0.013%	0.013%	0%	0.026%	0.026%
Load regulation	Main	0.53%	0.51%	0.55%	0.53%	0.55%
	Aux +	0.75%	0.80%	0.94%	0.97%	0.97%
	Aux -	0.78%	0.79%	0.79%	0.89%	0.89%
Input Current Max load (A)	Vin = 26V	1.530	1.535	1.538	1.543	mA
	Vin = 35V	1.134	1.139	1.142	1.144	mA
	Vin = 43V	0.928	0.933	0.936	0.939	mA
Input Current Min load (A)	Vin = 26V	0.271	0.274	0.274	0.271	mA
	Vin = 35V	0.211	0.211	0.211	0.211	mA
	Vin = 43V	0.177	0.180	0.180	0.180	2mA

All the electrical parameters are well within the device specification limits after irradiation up to a fluence of 5×10^{11}protons/cm^2.

IV. Conclusion

1. In-house 30W Triple output DC/DC Converter meets the Enhanced Low Dose Rate Sensitivity (ELDRS) test requirements up to 100krad (Si). All post irradiation parameters are within the specification and the maximum deviation observed was 14mV, 30mV and 19mV on main and auxiliary outputs respectively. The deviations are well within limits
2. No SET or SEL was observed during irradiation of heavy ions up to an LET of 50 MeV-cm^2/mg.
3. No displacement damage observed during irradiation of protons up to fluence of 5 x 10^{11} protons/cm^2. All post irradiation parameters are within the device specification.

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Failure Analysis, rework and rescreening of BLDC HMCs for Spacecraft application

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Abstract— The Brushless DC motor (BLDC) is used in Reaction Wheel (RW) and Momentum Wheel (MW) for Spacecraft application. The BLDC motor drive has six power switches, power switch drivers, commutation logic and current sense amplifier. The BLDC motor drive electronics circuits are miniaturized as hybrid microcircuit (HMC) package and subjected to screening tests/ Circuit type qualification (CTQ). The flight batch BLDC HMC devices after screening tests were integrated to Wheel Drive Electronics (WDE) and tested. The commutation supply voltage was dipping from +10V to +3.9V, the cause of the problem was analysed in detail and the corrections were done in HMC after delidding. The HMCs were resealed after correction and subjected to rescreening tests. This paper describes the failure analysis, HMC delidding process qualification, rework on BLDC HMCs, resealing process and rescreening test results.

Index terms: Hybrid microcircuit, Brushless DC motor, Wheel Drive Electronics

I. BLDC MOTOR DESCRIPTION

Brushless DC (BLDC) motors find wide range of applications in various industries and low-power appliances due to high-power density, ease of control and higher reliability owing to the absence of a mechanical commutator and brush assembly. These machines are often used for electric vehicular applications over wide torque and speed ranges. The BLDC machines, unlike the conventional DC machines, require an electronically switched commutator in the form of a converter circuit for its proper operation. The converter circuit which is essentially a three-phase inverter requires switching logic to drive the motor [1].

The most common circuit of brushless dc motor with permanent magnets and electronic commutator is a three phase motor with star-connected windings and electronic commutator connected into a 3-phase bridge. The connection scheme of main circuit of 3-phase PM BLDC motor with one pole pair, star-connected windings and electronic commutator connected as a 3-phase bridge [2] is shown in Figure 1.

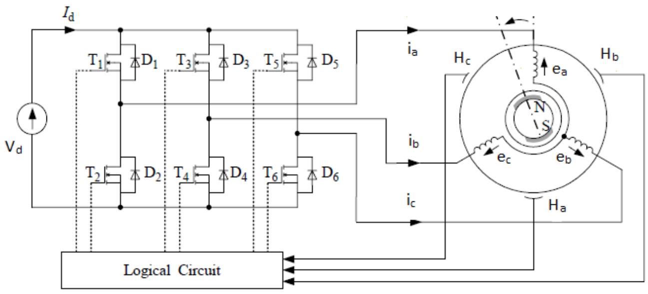

Figure 1. Electrical connections of three-phase, two-pole motor with electronic commutator

The equivalent circuit of a star-connected BLDC motor is shown in Figure 2.

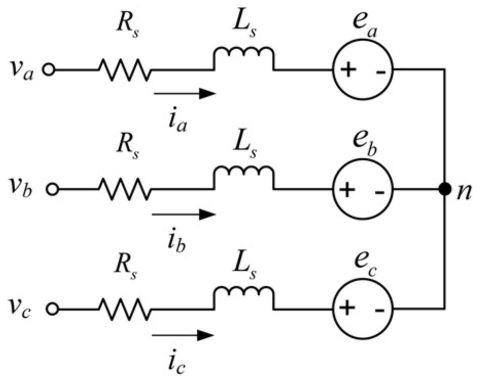

Figure 2. Equivalent circuit of a star-connected BLDC motor

The phase voltage equations from the equivalent circuit can be given as [1]

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{pmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{pmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{pmatrix} L_s & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & L_s \end{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_b \end{bmatrix} \tag{1}$$

$$L_s = L_{ss} + L_m \tag{2}$$

In (1) and (2), defining the suffixes a, b and c for three phases, v is the stator voltage, i is the stator current and e is the stator back emf all on per-phase basis. The inductance Ls is the stator inductance; Lm is the mutual inductance; and Lss is the stator leakage inductance on per-phase basis.

The dynamic torque equation for the BLDC motor can be given as [1]

$$T_{em}(t) = J\frac{d\omega(t)}{dt} + B\omega(t) + T_L(t)$$
$$= (e_a i_a + e_b i_b + e_c i_c)/\ \omega \qquad (3)$$

where T_{em} is the developed electromagnetic torque, ω is the rotor angular velocity, B is the viscous friction constant, J is the rotor moment of inertia and T_L is the load torque.

II. BLDC MOTOR DRIVE HYBRID MICROCIRCUIT

The BLDC motor is used in reaction wheel and momentum wheel for attitude control in spacecraft. The RW/ MW generates torque by driving a f lywheel connected to a brushless direct current motor [BLDC]. The BLDC motors use hall sensors for position sensing and electronic commutation. The bipolar/bidirectional switching scheme is used for driving the BLDC motor. The bipolar/bidirectional switching circuits are miniaturized as hybrid microcircuits for better reliability. This HMC has six power switches, power switch drivers, hall sensors commutation logic and current sense amplifier.

The BI-DIRECTIONAL DRIVER HMC-CTM866D481 consists of

1. Logical Circuits for Commutation
2. Top switch with PWM controller
3. Bottom switch with linear current controller
4. Differential Current Amplifier

*5 Back e.m.f filter
*6 Current Sense Resistors
*7 Reaction Wheel / Resistive Load (star)
* - Connected external to HMC

HMC DETAILS

PART NO : CTM 866 D481

Type : Bipolar Drive HMCs for WDE
Manufacturer : M/s Centum Electronics Ltd., Bengaluru

The HMC voltage/current specifications are given in table 1.

TABLE 1. SPECIFICATION OF THE BLDC HMC

Sl.No	HMC. Pin no.	Voltage Specification	Current Specification
1	15	+15V±5%	<2mA
2	14	-15V±5%	<2mA
3	24	10V±5%	<10mA
4	1/5/9	18V±5%, to 42V±5%	< 50mA No load <5 A for Full Load

Mechanical Specification

Case outline dimensions : 97 x 56.40 x 6.5mm^3
Substrate size & material
A - Al_2O_3 : 1.6''X1.25''X0.25''
B - Al_2O_3 : 0.8"X1.25''X0.025''
C1,2 - BeO : 0.8"X0.6''X0.025''
D - Al_2O_3 : 0.515''X1.87''X0.25''
E - BeO : 0.8X0.6''X0.025''
Package weight : <200 gm
No of layers
Signal Circuits : Four
Power circuits : Single with dielectric Crossover
Package style : DIL (Hermetically sealed)
No. of I/O pins : 28
Signal pin : 16
Power pin : 12
Body finish : Gold plated
Lead finish : Gold plated

The alumina and beryllia substrate are used in the HMC. The beryllia substrate provides better thermal conductivity and used for attachment of power transistors. The beryllia sunstrate is attached to the HMC header using SnPb Solder. The substrate material characteristics is given in table 2.

TABLE 2. SUBSTRATE MATERIAL CHARACTERISTICS

	Unit	96% Alumina	99.5%/ 99.6% Alumina	Beryllia (BeO)	Aluminum Nitride (AlN)
Dielectric Constant (1MHz)		9.5	9.9	6.5	8.6
Dissipation Factor (1MHz)		0.0004	0.0001	0.0004	0.001
Thermal Conductivity (100°C)	W/m-K	20	27	270	170
Coeff. Thermal Expansion	ppm/ºC	6.3-8.0	7.0-8.3	9.0	4.6

The burn-in temperature was limited to 115°C in order to limit the junction temperature < 125°C and the burn-in duration was increased to 440h. The process identification document and the list of materials used for fabrication of BLDC HMC were made and followed.

The HMC was initially developed for operating voltage of 42 V DC and the circuit type qualification was successfully completed. Later the HMC was redesigned for operating voltage of 70V DC by replacing the top switch to meet the voltage de-rating guidelines. Proto HMCs were made and after qualification tests, the flight batches were subjected to screening tests. The HMCs were integrated in the WDE and tested and found that the +10V supply voltage was dipping to +3.9V. The +10V is derived from a zen er diode through +15V, which can source current up to 50mA.

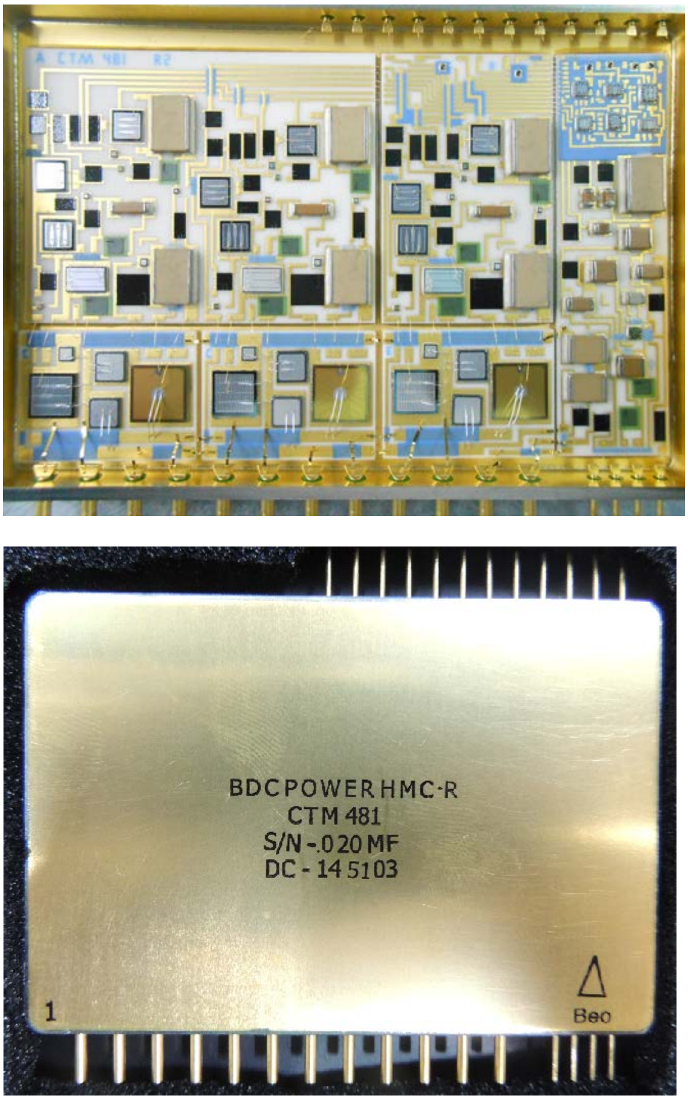

Figure 3. Internal and external view of Bipolar Drive HMC

III. Failure Analysis

The circuit was drawn in PSPICE and the probable cause for the observation was analysed. The missing of connection in the R-phase of the bottom switch driver's collector (Q5R) to base (Q6R) was suspected and it was also confirmed by inspection after delidding of the BLDC HMC. The HMC layout was changed to accommodate Q1R 2N5666 transistor die size 0.142"x0.142", while effecting this modification the connectivity between collector to Q6R to R11R was missed.

The figure 4 shows the bottom switch circuit and missing track with x-mark. In the driver, Q5R and Q7R configured as push-pull driver for the R phase bottom power switch. The current controller output (varies from 0 to +12V, during torque mode 8 to 12V expected and during breaking 3 to 6 volt is expected) is driving the base of Q5R. During the normal operation, as per the design, the Q6R transistor is ON for 240 degrees, which in-turn switches ON Q7R transistor and switches OFF MOSFET Q9R. The Q6R transistor is OFF for 120 degrees, which in-turn switches OFF Q7R transistor and switches ON MOSFET Q9R via Q5R transistor.

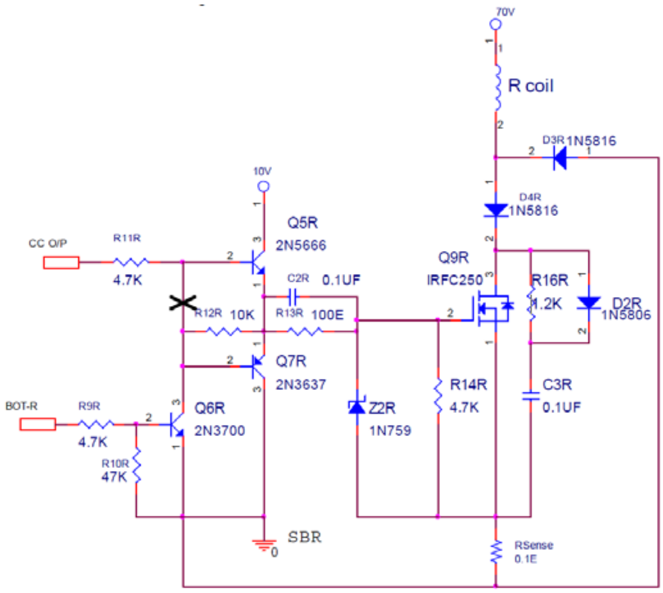

Figure 4. R-Phase bottom switch

Due to this connection missing, the Q5R transistor was always in ON state. In this condition, whenever the Q6R transistor is ON, the Q7R transistor withdraws the MOSFET Q9R gate charge as well as Q5R collector currents. This causes Q5R power dissipation exceeds the designed value. Due to this excess power, the +10V supply voltage is dipping to +3.9V.

The stress analysis was carried out Q6R ON (i.e MOSFET OFF) and Q6R OFF (i.e MOSFET ON) conditions with current controller output at +12V.

Case 1: Q6R ON

The commutation logic is working in +10V logic, when commutation logic makes Q6R ON, the Q6R transistor is fully ON with the base current of ~2 mA, which is limited by 4.7K resistor (R9). By considering the minimum hfe (Table-3 gives the device parameters) of Q6R, the collector drive of Q6R can be as high as 180mA, which is nothing but the base of Q7R. Once again considering the minimum hfe of 90, the collector current may be as high as > 1A. In this case, though the top transistor Q5R is ON permanently, the bottom transistor Q7R can reliably sink the Q5R Emitter current as well as Q9R MOSFET gate charge. If the bottom transistor is fully on, the base current of Q5R is approximately 2.5 mA (Current controller output is 12V and series resistor is 4.7K). With Q5R's maximum hfe of 120, Q5R collector current can be 300 mA. Since bottom transistor Q6R & Q7R is capable of sinking 1A, the loss in Q7R is approximately 0.3 watts only (Q7R VCE of 1V and IC of 0.3A). whereas, the power dissipation on Q5R can be 3 watts for this higher hfe

conditions. Hence by simulation as well as theoretical calculation, the Q9R MOSFET OFF is ensured by turning ON the Q6R transistor for all the environmental conditions (Table-4 gives Simulation Results). **However, due to continuous ON of Q5R, the power dissipated on the device is as high as 3 watts for 240 degrees duration**, which is exceeding the power specifications. It is also to be noted that, all the passive elements power rating also within the safer limits during this 240 degree.

Case 2: Q6R OFF **(In this case, the removal of connection Q5R base to Q6R Collector has no impact practically)**
Once the Q6R OFF (which is of 120 degree) is issued from the commutation logic, the Q6R transistor is fully OFF, which in turn switches off Q7R due to Darlington connection. Due to the self-bias arrangement of Q5R transistor, the Q5R is fully ON. This in-turn switches ON the MOSFET Q9R as per the original design. The **minimum collector current of Q5R is 80mA** (base drive of 2 mA and minimum hfe of 60). By considering the Gate capacitance of 20nF, the supplied current **is quite adequate to turn on the MOSFET reliably for all the environmental conditions**. In this case, all the passive elements power rating is also within the safer limits during this 120 degree.

TABLE 3. DEVICE PARAMETERS

Device	h_{FEMin}	h_{FEMax}	VCO_{Max}	P_{total}, T_A = 25°C
Q5R-2N5666	40	120	200 V	1.2 W
Q7R-2N3637	90	300	175 V	1 W
Q6R-2N3700	90	300	80 V	0.5 W

TABLE 4. SIMULATION RESULTS

Sl. No	Active Elements	@ +20 Deg C			@ +125 Deg C			@ -40 Deg C		
		Current (mA)	Voltage (V)	Power (W)	Current (mA)	Voltage (V)	Power (W)	Current (mA)	Voltage (V)	Power (W)
1.	Q5R-2N5666	255	9.28	2.088	351	9.36	3.28	187	9.17	1.71
2.	Q7R-2N3637	256	0.7	0.179	353	0.635	0.224	189	0.82	0.155
3.	Q6R-2N3700	2.3	0.011	~0	8	0.024	~0	2.3	0.012	~0
4.	Z2R-1N759	0	9.75	0	0	9.76	0	0	9.75	0
5.	Q9R-IRF250 – Gate current and V_{DS}	100	0.173	-	131	0.18	-	115	0.168	-

Inferences from the analysis,

1. **The power rating of Q5R is exceeding (~3watts). Hence it was recommended to replace the component**.

2. The stress analysis shows that, the power MOSFET ON and OFF cases follows the commutation signals during different environmental conditions. Hence the **MOSFET in active region during the commutation is ruled out and its dissipation is as per the derated design.**

3. All other active and passive driver component's ratings are within limits for all operating conditions.

4. The HMC layout was made in AutoCAD by drawing. The normal procedure for verifying the circuit interconnectivity is by verifying the Net list. This is not possible in AutoCAD layout and it has to be checked manually by tracing the track in the layout as per the schematics.

5. The HMC standalone test procedure was also strengthened for the 10 V measurement. The 10 V current will be measured by setting the current controller input voltage to 13 V.

IV REWORK ON BLDC HMC

The BLDC HMCs are delidded at IISU carefully and the following reworks are done inside the HMCs.

- ➢ Updated the HMC layout.
- ➢ Inspection of R phase bottom switch drive circuit for any decolouration.
- ➢ Replaced Q5R 2N5666 die in Card A.
- ➢ Additional 1mil wire bond added between Q6R collector & resistor R11R as shown in figure 5.
- ➢ NDPT for wire bonds of Q5R 2N5666 die and 1mil wire bond (between Q6R collector & resistor R11R).

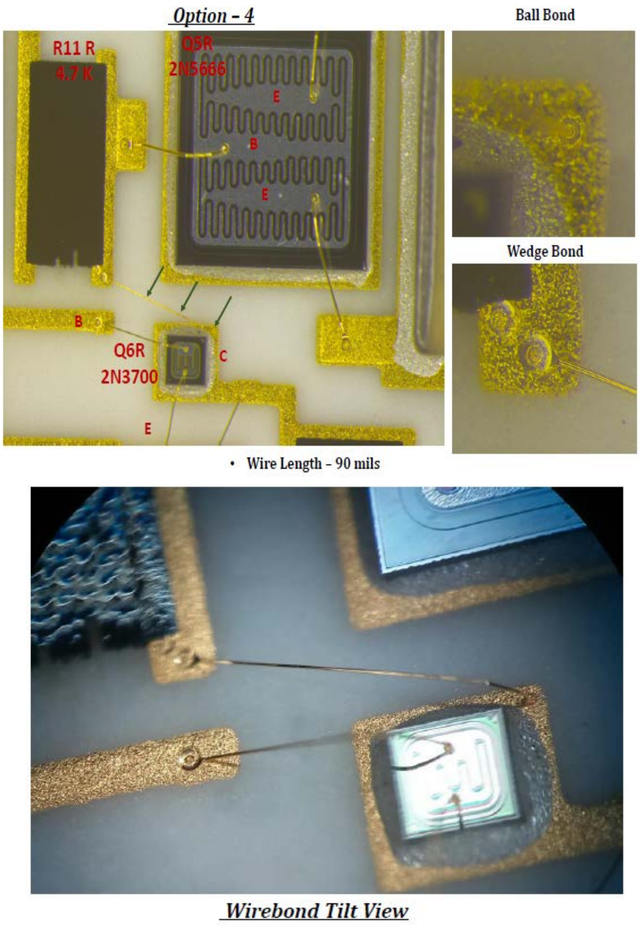

Figure 5. Additional 1mil wire bond added between Q6R collector & resistor R11R

V BLDC HMC – DELIDDING AND RESEALING QUALIFICATION PLAN

For high-reliability packages with lid areas greater than 160mm^2, welding, which achieves high yield (typically above 98 percent), welded seal is the preferred sealing process. The process generates extremely localized heat at the seal site; the active elements and attachments are

commonly subjected to no more than 50°C temperature for two to three minutes [3]. Thus, the process does not adversely affect the reliability of even the most sensitive active elements and attachments. In addition, organic vapours do not outgas during the sealing process as is the case with most glass and solder-sealing operations. Until recently, a welded joint presented delidding problems for package rework after lid sealing. However, delidding procedures for welded lids are well developed now and are routinely used in the industry, further enhancing the suitability of welded seals. Welded seals may be made by any one of a number of conventional methods, including welded seals made with energy forms such as lasers or electron beams (Messler, 1993).

The following table 5 shows the delidding and resealing process qualification adopted for repair of BLDC HMCs.

TABLE 5. HMC DELIDDING AND RESEALING PROCESS QUALIFICATION

No	Stage	Process Steps /Sequence
1	HMC delidding & Resealing	Delidding of HMC using approved procedure
2		LID removal, Visual inspection & general cleaning
3		Cleaning of HMC using E.G.IPA
4		Au 1.5 mil Wire Bonding (CTQ-02 - Post pin to chassis & Post pin to Substrate)
		Electrical Testing of the HMC as per the specifications
5		visual inspection & clearance for further activities
6		Vapor degreasing before Vacuum baking
7		PIND test
8		pre-cap visual inspection & further clearance
		H74 Epoxy application for identified substrates (C,C &E cards) & curing
9		Electrical Testing of the HMC as per the specifications
10		Vacuum Baking for 72 Hours
11	QUALIFICATION PLAN AS PER ISRO- PAS 206	Sealing of the HMCs
12		Seal leak: Fine & Gross
13		Rebranding of HMCs (identification " R")
14		Electrical Testing of the HMC as per the specifications
15		External visual inspection
16		Temperature cycling
17		Vibration test (Sine)
18		Electrical Testing of the HMC as per the specifications
19		Seal leak: Fine & Gross
20		Electrical Testing of the HMC as per the specifications
21		External visual inspection

. The process qualification was carried out on the CTQ batch HMCs and after that the flight batch HMCs were reworked using the qualified process.

VI RESCREENING TEST FOR REWORKED BLDC HMC

The following table 6 shows the rescreening tests adopted for BLDC HMCs after rework/ resealing.

Sl No	Process	Specification
1	Visual Inspection	
3	Stabilization bake	150Deg C / 24hrs
4	Temperature Cycling	150Deg C & -65deg C, 10min dwell ,10cycles
5	Constant Acceleration	3000g for 1 min ,y Axis
6	PIND test	20g @ 60hz
7	Pre Burn-in Electrical measurements	
8	Burn-in	115 Deg C /440hrs
9	Post Burn-in Electrical Measurements	
10	Fine leak	15psig / 13hrs
11	Gross leak	15psig/13hrs
12	Low / High temperature electrical	Cold -20deg C /2hrs and HOT +6odeg C /2hrs
13	Final electrical measurements	
14	Visual Inspection	

The rescreening test results were satisfactory, except for PIND test. However, the devices have undergone acceptance and qualification level random & sine vibration test in active condition after integrating in to the Wheel Drive Electronics and the performance was normal.

CONCLUSION

The commutation supply voltage dipping from 10 V to 3.9 V in BLDC HMC during integrated level testing of Wheel Drive Electronics was analysed. The missing of track/ connection inside the HMC was found to be the cause of the problem and it called for delidding and resealing of the BLDC HMCs for rework. The process qualification for rework of HMCs are carried out on CTQ samples. The BLDC HMCs were reworked after delidding and resealed after correction. The devices were subjected to rescreening tests and cleared for use.

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Study the effect of energetic electron and proton radiation on Multijunction solar cells

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Abstract — Photovoltaic Solar array system is a primary source of power generation not only for LEO, MEO, and GEO missions but also for various interplanetary and rover missions. The most critical characteristic of space solar cells is its radiation hardness. The space radiation environment degrades the long-term performance of the solar cells. Understanding of the performance degradation of solar cells due to radiation is very critical. In this paper the degradation effects caused by electron and proton are summarized based on literature survey. The results of illuminated IV measurements and quantum efficiency studies carried out on irradiated solar cells are presented.

KEY WORDS: Multijunction solar cells**,** Quantum efficiency, illuminated IV characteristics

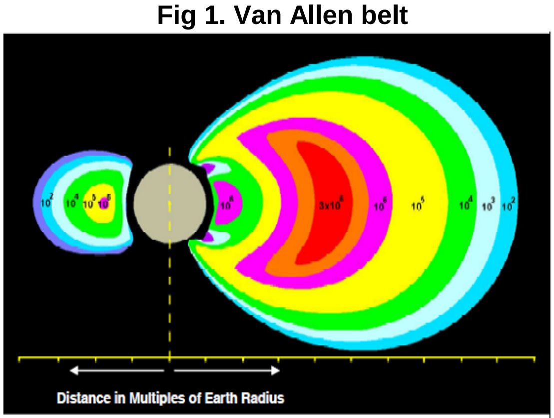
I. INTRODUCTION

Photovoltaic Solar array system is a primary source of power generation for all LEO, GEO, and MEO near earth missions as well as for various interplanetary and rover missions because of its robustness, reliability and environment friendliness. Tremendous advances in solar cell technology in the last four to five decades, starting from less than 10% efficient single-crystal silicon solar cell to the state-of-art 30 % efficient multijunction solar cells have made it possible to cater high power requirements of spacecraft loads. In a time period of less than four decades, space solar arrays have grown in size from less than 1 watt to systems over a few tens of kilowatts.

The most critical characteristic of space grade solar cells is its radiation hardness. The space radiation environment degrades the long-term performance of the solar cell. It is very essential to understand the solar cell device behavior due to radiation. The solar cell device parameters as well as electrical parameters will change when the solar cells are exposed to energetic electron and proton radiation environment

The space where the satellites traverse is abounded with energetic charged particles. These energetic particles (electrons and protons) ejected by the Sun are magnetically trapped around the Earth, forming the radiation belts, also known as the van Allen belts. The radiation belts consist principally of electrons with energies between few tens of KeV and up to few MeV,

Fig 1. Van Allen belt



protons with energies between 100 K eV and several hundred MeV. The inner zone is the

predominantly proton belt (peak intensity at about 3000 kilometers from Earth's surface) and the outer zone is the predominantly electron belt (peak intensity from about 12,000 t o 22,000 kilometers from the Earth's surface).

Understanding the behavior of the solar cells after its exposure to radiation environment is very crucial in designing of solar arrays for space crafts. The performance ratio of BOL (beginning of life) to EOL (end of life) should be minimum and it’s a performance indicator of the solar cells. Different characterization techniques are used viz. Illuminated IV measurements, external quantum efficiency in evaluating the performance of the solar cells before and after radiation exposure.

Details of the effect of different energy at different fluences of electron and proton radiation on solar cell is discussed in the following sections Also the test results of illuminated IV characteristics and external quantum efficiency before and after the irradiation is presented.

II. EFFECT OF PROTON AND ELECTRON RADIATION ON SOLAR CELLS

In solar cells electron and proton radiation usually produces atomic displacements and as a result of atomic displacements, lattice defects such as vacancies, interstitials, and complex defects are generated. Lattice defects that act as recombination centers or trapping centers causes a decrease in the output power of solar cells.

The effect of different energy protons on the multijunction solar cells is shown in the figure 2. It clearly indicates that the low energy protons (few KeV) causes damage to the top InGaP solar cell. High energy proton causes damages to middle GaAS solar cells.10MeV proton passes through the entire structure.

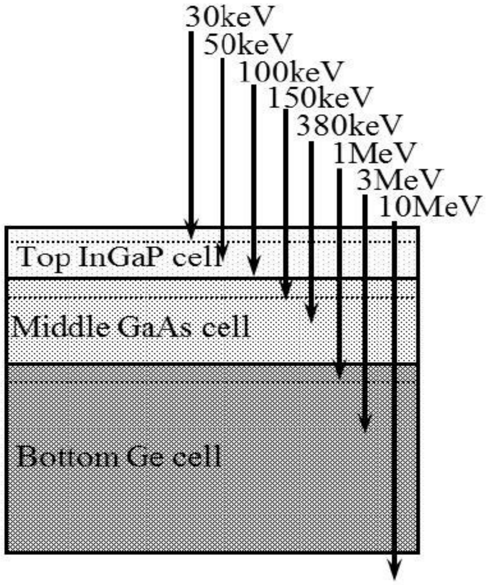


Figure2. Penetration depth of protons of various energy irradiated from the top surface

The radiation defects due to proton are more at around the depth where proton penetration stop. Thus,the radiation defect densities becomes more when the depth corresponds to the pn junction or the depletion layer depth in a solar cell. Hence the degradationt becomes more. In order to protect from proton radiation, the solar cells are covered with coverglass and hence degradation will be very less. But in case of electron radiation ,the electrons are scattered and diffused into a material. Therefore the defects created by electron do not localize at some specific reagion but are distributed in a wide area. When a electron energy is sufficient enough to go through the cell the radiation defects are created with a u niform density.

Typical example of effect of both proton and electron radiation with different energies and

doses on solar cell power output is shown in figure3.

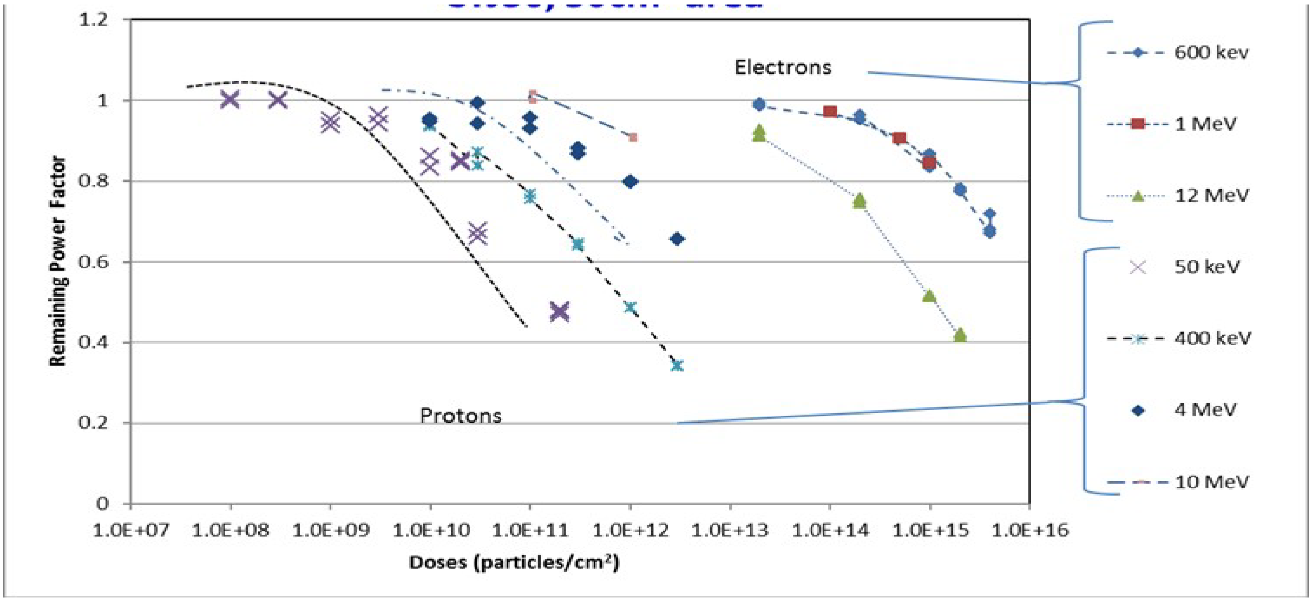


Figure3: Solar cell remaining factors after proton and electron irradiation at different energy and different dose

III. CHARACTERIZATION TECHNIQUES RESULTS AND ANALYSIS

1.1. External quantum efficiency (EQE):

External QE measurements are essential for the design and performance evaluation of multijunction solar cells. The EQE measurement give direct & fast result of radiation effect on MJSCs by showing the reduction in the EQE spectrum. From the EQE graphs, one can find out the important solar cell performance parameter, the short circuit current density (Jsc). Figure 4 and 5 shown below are external quantum efficiency measurement of top and middle cells before and after irradiation.EQE measurements shows up to 20% degradation in the top cell and up to 10% in the middle cell with 50keV proton.

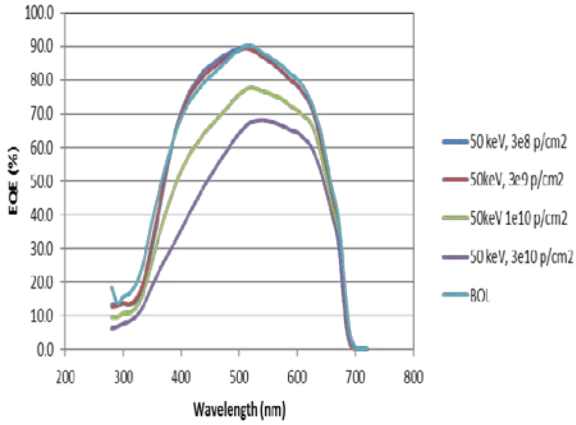


Figure4: EQE TOP cell degradation after proton test

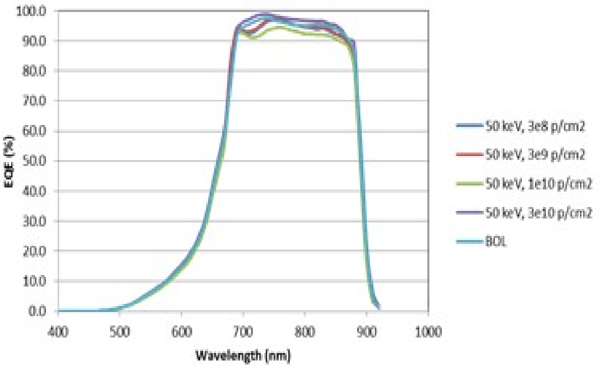


Figure5: EQE Mid cell degradation after proton test

3.2 Solar cell IV characteristics:

Solar cell Illuminated IV characteristic is essential to determine the electrical performance of the solar cells. Also from IV we can determine the solar cell device parameters like series and shunt resistances. The solar cell IV characteristics will show a degraded performance due to radiation. Figure 6 shows the typical IV characteristics of multijunction solar cell before and after radiation

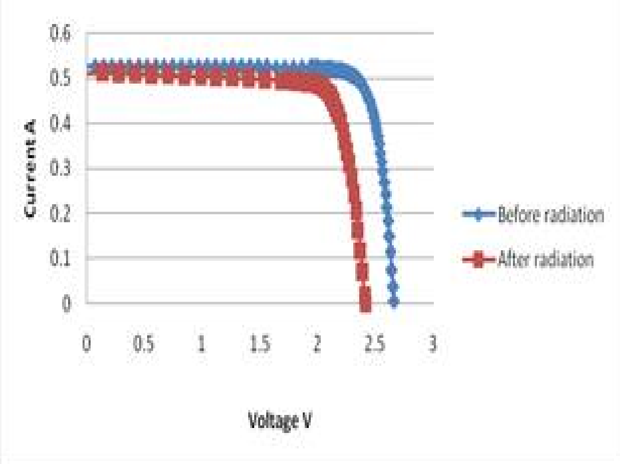


Figure6. Solar cell IV characteristic before and after radiation

The solar cells were irradiated at different energies and doses for both proton and electron.

Figures 7 to 10 shows the performance degradation of solar cell's voltage, current and power after it is exposed to proton and electron radiation at different energies and fluences.

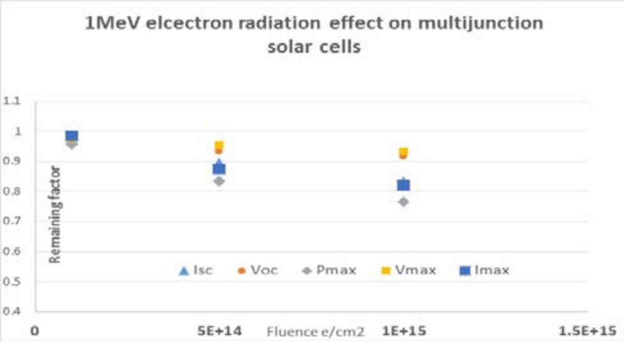


Figure7: 1MeV electron radiation effect on MJ solar cells

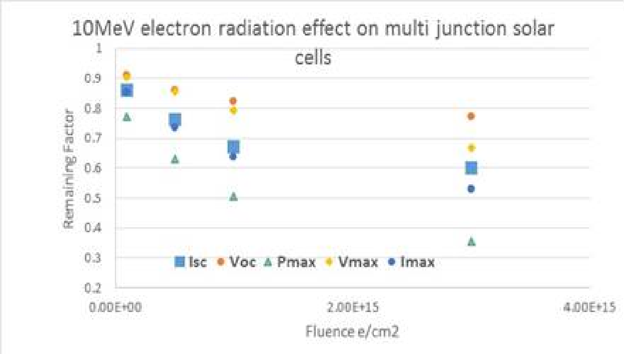


Figure8: 10MeV electron radiation effect on MJ solar cells

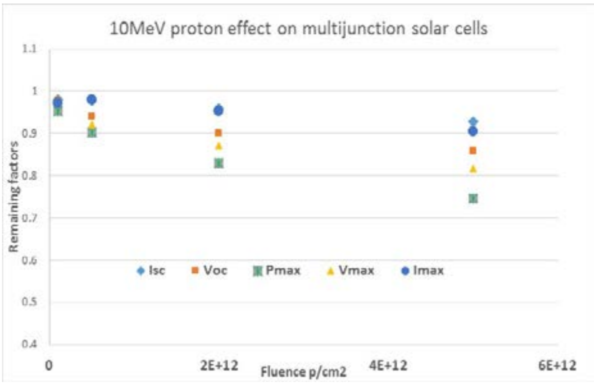


Figure9: 10MeV Proton radiation effect on MJ solar cells

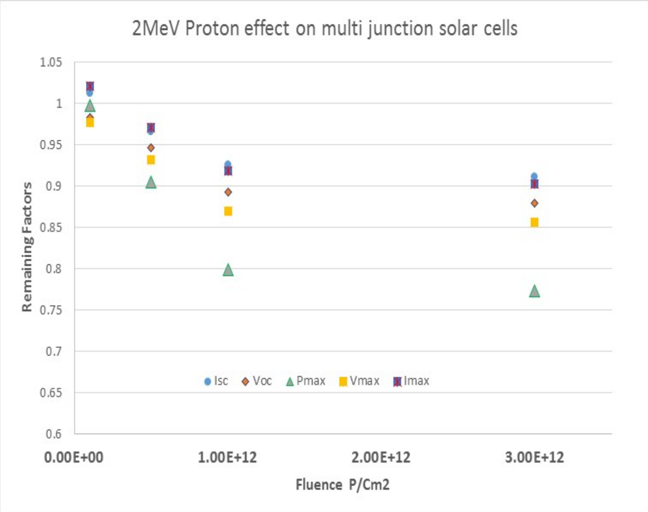


Figure10: 2MeV Proton radiation effect on MJ solar cells

IV. CONCLUSIONS

The effect of proton and electron radiation on multijunction solar cell is studied. To understand the behavior of the solar cells, different characterization techniques are used viz. solar cell dark and illuminated IV measurements, external quantum efficiency. The results of proton and electron radiation on multijunction solar cells are presented in this paper. Further study is under progress to develop suitable degradation model.

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EOS and ESD phenomenon in Semiconductor Devices

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ABSTRACT

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) combining are the major source of failure in the semiconductor industry. As both EOS and ESD are driven by same failure mechanism i.e. Joule's heating effect, failure signature generated by them is similar. Hence it is very difficult to distinguish between ESD and EOS phenomenon in semiconductor device.A systematic physical failure analysis methodology can beapplied to distinguish the damages induced by EOS and ESDin semiconductor devices. Eventhough the electricalfailure modes observed are identical, a t horough analysis byknowing the differences in failure signatures **as** well **as**employing specific methods, it is found possible todistinguish between EOS and ESD failures to a g reat extent.

Both field failed and simulated failed cases have beenstudied to establish the difference in failure signatures.

Keywords: ESD, EOS, SEM, PEM,Latent Damage, HBM ESD Tester

I. INTRODUCTION

The boundary between Electrostatic Discharge (ESD) and Electrical Overstress (EOS) in semiconductor devices is very fuzzy. Electrical failure modes due to EOS and ESD are similar. ESD is actually a subset of a broad spectrum of EOS, where the EOS family includes lightning and electromagnetic pulses [1]. The main concern for the microelectronic chips is ESD, which is in the time scale of the 100 ns range. EOS, on the other hand, commonly refers to events other than ESD that encompass time scales in the microsecond and millisecond ranges. These events can occur due to electrical transients at the board level or the system level. They can also occur during device product engineering characterization or during the bum-in test. The primary difference between ESD and EOS events is their time duration. ESD events are generally between 500V and 8000V, and last for less than 300nS. During an ESD event, the peak current can reach many amps of current, but because the event is so short, a w ell designed ESD protection circuit can shunt this energy to ground which causes no damage. While voltage and current levels can be similar, an EOS event has a much longer duration, typically from 1 μSto few minutes [1].Due to the observed striking similarities in the EOS and ESD failure modes andsimilar failure signatures, it is very difficult to distinguish between them [2-5]. In many of the field failureanalysis cases, where the failure cause is hard or impossibleto identify, the device failure will be generically attributed toEOS. Further, there were a number of previous reportshighlighting that with careful methods it i s possible todistinguish failures arising out of EOS and ESD [6-9].However, with rapid miniaturization and newer ESD/EOSthreat scenarios, there is a definite need to constantly updatethe analysis procedures to achieve accurate failure causedetermination. The purpose of this paper is to highlight thenewer/improved analysis methods that are available foranalyzing the ESD failures, along with a discussion on theidentified failure mechanisms.

The present study is focused to understand the difference between EOS and ESD, based on their physical failuresignatures/damages caused in the device structures. Various sophisticated analytical equipments such as Scanning Electron Microscope (SEM), Photon Emission Microscope (PEM) and Human Body Model (HBM) ESD simulators were used substantiate the difference between ESD and EOS. Thestudy also highlights the need for a systematic and structuredphysical analysis, which is the key to identify the failurecause. In the subsequent sections, details of the device analyses andthe experimental methods used are briefly explained followed by the ESD failures and EOS failures respectively.

II. EXPERIMENTAL DETAILS

In this investigation, field failed devices were analyzedalong with lab-simulated-devices. The field-

faileddevices are initially categorized as EOS/ESD failureswithout clear distinction. In the case of lab ESD simulateddevices, good deviceswere subjected to controlled ESDstress using Human Body ModelESD Simulator as per MIL-STD-883G method 3015. Since there are no standard test methodsavailable for EOS simulation study, DC voltage/current step stress method was employed until failure occurred.Though standard failure analysis techniques using SEM andPEM were applied to identify the failure locations, specificimprovised physical failure analysis methods were employedto identify the failure mechanism, which require carefulplanning and focused methodology. Bulk CMOS IC analog multiplexer CD4051 and Pulse width modulator IC SG1524 were chosen for EOS/ESD field failure and EOS/ESD simulation study.

III. RESULTS AND DISCUSSION

A. EOS FAILURES:

In a s emiconductor environment, Electrical Overstress (EOS) is a term used to describe the phenomenon that may occur when an electronic device is subjected to a current or voltage that is beyond the specification limits of the device. Field failures due to thermal damage can occur when the excessive heat generated during an EOS-ESD event melts themetal interconnects of conductors or resistors. The excessive heat generated during an EOS/ESD event can melt the metalinterconnects of conductors or resistors. The metal line that acts as a fuse may become completely open after melting in thick conductor films. Even partial melting of the metal line mayimpact the functionality of the device. If the metal line has resistance R and I is the current flowing, then the powergenerated will be $P = I^2R$. This phenomenon is also called as joules heating effect.When temperature due to localized heat is raised to the melting point of the metal line, melting will occur.The Electrical Overstress may result in thermal damage to the entire device or a p ortion of the device. The thermal damage is the result of the excessive heat generated during the EOS event. When a device is subjected to high voltage or current, resistive heating in the connections within the device generates excessive temperatures. Typically, the excessive heat is localized around the area where the electrical stress is exerted. This result in damage to the device, and most of the time, this damage is visible to the naked eye. EOS can be the result of a single non-recurring event or the result of ongoing periodic or non-periodic events. An EOS event can be a momentary event, lasting only milliseconds, or can last as long as the conditions persist. After the EOS energy is dissipated, the device may be permanently damaged and may become non-functionalor partially functional.The following is a list of causes for EOS[10]:

1. Power supply voltage surge beyond the absolute maximum voltage range.
2. Switching circuits on the board may cause highvoltagespikes internal to the board, propagatedto other devices on the board.
3. External connections, such as capacitive chargeon an external cable, antenna pick-up of externalswitching noise and inductive loads can createvoltage spikes.
4. Excessive noise on the ground plane due topoor grounding.
5. I/O switching creating voltage overshoots orundershoots.
6. EMI (Electromagnetic Interference) due to poor shielding in an electrically noisy environment.
7. Improper power-up sequences can applyunintended voltage levels or polarities to thedevice.
8. ESD events that cause damage, or weaken thedevice, making it more susceptible to futureEOS events.

An EOS failure is identified by the following damage conditions:

1. Large areas of damage are seen
2. Characterized by a large amount of melted metal
3. Can be localized to an I/O pad or internal to the die in the case of an EOS event on a supply pin
4. Damage can encompass many devices
5. Can have many different simultaneous damage types

B. EOS CASE STUDY

During satellite level integration testing,few ICs CD4051 (Analog Multiplexers) failed with output floating. Failure Analysis on the above ICs revealed charring and open of one input pin (refer figures 1 & 2).

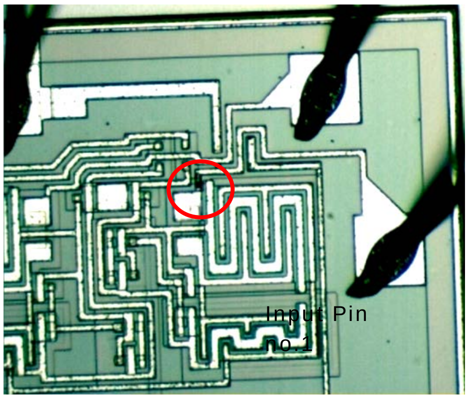


Fig.1: Optical photograph shows Charring & Opening of metallization connecting I/P pin no.14 of the IC CD4051.

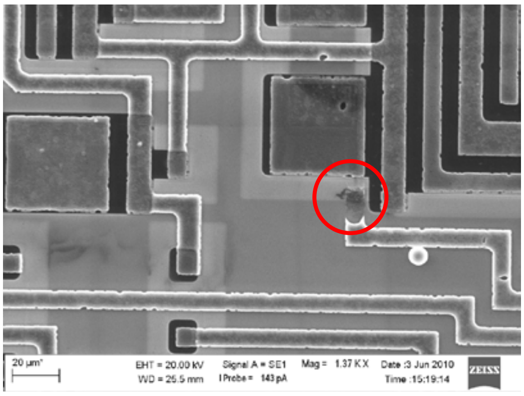
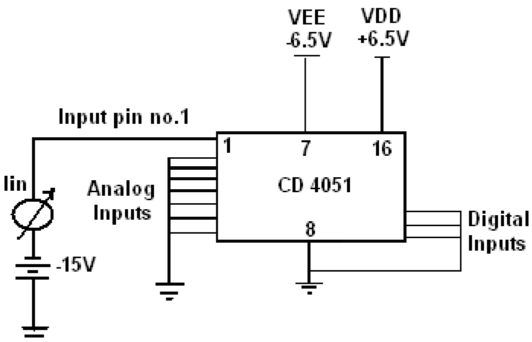


Fig.2: SEM photograph shows Charring & Opening of metallization connecting I/Ppin no.14 of the IC CD4051.

It is assumed that input pins no 13 a nd 14 of ICs CD4051, which are grounded during spacecraft level integration testing, might have accidentally shorted to negative supply line (-15V) as the ground and the supply point are adjacent to each other in the OLM test point. In order to verify this assumption, EOS simulation study was carried out on CD 4051 by momentarily shorting an input pin directly to -15V, where other inputs pins grounded and V_{DD} and V_{EE} are at +6.5V and -6.5V respectively.Test circuit, test condition and results are shown below.

Test Circuit



Test Results

Test Pin	Supply Voltages (VCC & VEE)	Voltage applied at pin no.1	Input Current	Result
I/P Pin no.1	VCC = 6.5V VEE = -6.5V	-15 V	~200mA (Current limit was kept at 500mA)	Input pin no.1 failed at open mode.

Post-decapping internal visual examination revealed using optical microscope (refer figure-3) and SEM (refer figure-4) revealed charring and opening metallization connecting input pin no.1. This signature is matching to that of the field failure IC CD4051.

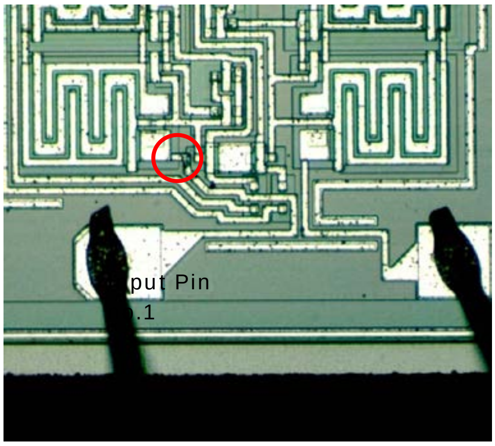


Fig.3: Optical photograph shows charring &opening of metallization connecting I/P pin 1 of simulated IC CD4051.

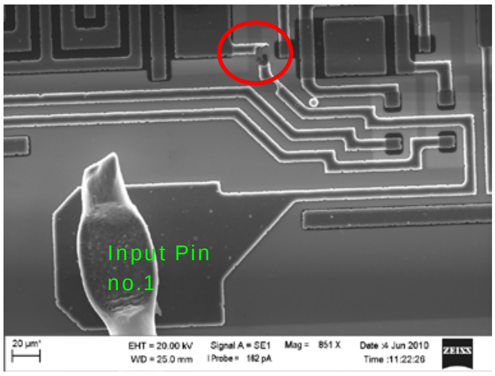


Fig.4: SEM photograph shows Charring & Opening of metallization connecting I/P pin 1 of simulated IC CD4051.

Above discussion revealed that signature duo to Electrical Overstress are clearly visible on the surface of the IC diewith help of optical microscope and SEM. On the contrary, when the same device (CD4051) failed with output latched to high, failure analysis followed by failure simulation study indicates ESD induced failure. Internal visual examination (Optical/SEM) revealed no visual damage on the die surface (refer figure-5)

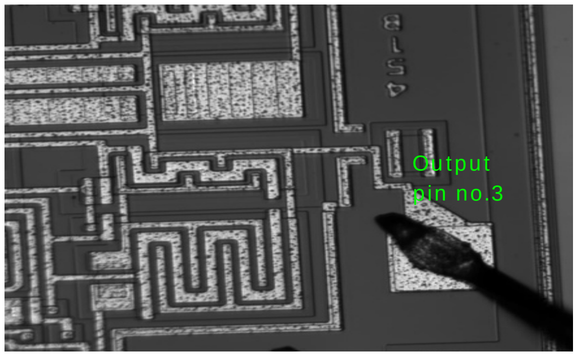


Fig.5: Optical photograph shows no visual anomalies on the metallization/contact window connecting to O/P pin no.3.

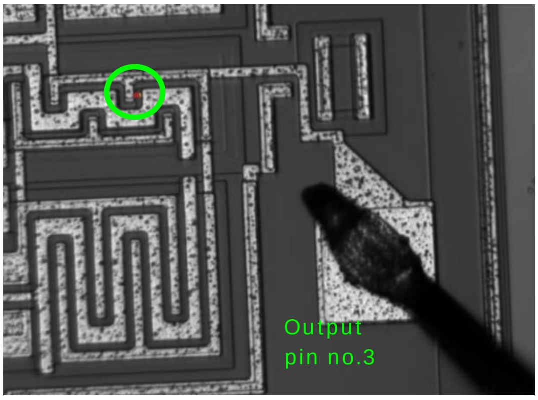


Fig.6: Optical photograph shows no visual anomalies on the metallization/contact window connecting to O/P pin no.3.

Photon Emission Microscope (PEM) analysis of the failed IC revealed hot spot near the contact window O/P pin no.3 (refer figure 6). Usually hot spots are artifacts of ESD, which represents gate oxide damage/oxide puncturing area where emission of heat/light occurs due to current crowding.

C. ESD FAILURES:

The Electrostatic Discharge (ESD) is the most common phenomena of Electro-Magnetic Compliance (EMC). The word, electrostatic, indicates static electricity accumulated by specific materials that come into contact with one another, such as rubbing your feet on a wool carpet. ESD is a miniature lightning bolt of charge that moves between two surfaces that have different potentials. It can occur only when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When a s tatic charge moves, it becomes a current that damages or destroys gate oxide, metallization, and junctions. ESD can occur in any one of four ways: a charged body can touch an IC, a charged IC can touch a groundedsurface, acharged machine can touch an IC, or an electrostatic field can induce a voltage across a dielectric sufficient to break it down. The amount of electric discharge depends upon the material and environment, including humidity. ESD discharge not only happens when a human comes in contact with a statically charged material.Machines and furniture, such as lab tables, can also accumulate static electricity, and discharge when electrical components come in contact with them.

An ESD failure is identified by the following damageconditions:

1. Small focused area of failures
2. Typically focused around an I/O pad and associatedcircuitry.
3. Characterized by melt filaments between junctionsof transistors, causing a short.
4. Can be very small and difficult to find
5. Only a single device is damaged
6. There is only one type of damage mode

Gate oxide damage is the most common and prone to ESD events. Gate oxide breakdown depends upon the thickness ofoxide, biasing voltage, breakdown voltage of oxide material, uniformity, and roughness of oxide film. If the oxide film hassharp edges, the induced electric field will be highly concentrated to those edges and highly prone to breakdown.The averageelectric field across the oxide layer then can be calculated from the equation $E = V/T_{OX}$

Considering the oxide layer to have a thickness (T_{OX}) of 100 Å with applied voltage (V) across the oxide layer of 3.3V, $E=3.3V/(100 \times 10^{-8}$ cm) $= 3.3 \times 10^{6}$ V/cm. Silicon dioxide (SiO_2), a d ielectric material, has a b reakdown electric field of 11×10^{6} V/cm. If the oxide thickness isreduced to 50 Å, then, electric field increases to $E = 6.6 \times 10^{6}$ V/cm. There will be an increase in the electric field across the dielectric if breakdown voltage increases or dielectric thickness decreases.

D. ESD CASE STUDY:

During package level Thermal vacuum testing, few pulse with modulator ICs SG1524 failed with variation of output with temperature excursion of -25°C to +55°C. Failure analysis was carried out on these ICs, where in optical microscopic analysis and SEM analysis did not reveal any visual anomalies on the surface of IC die (refer figure-7) but PEM analysis revealed low intensity hot spot(blue colour) towards the center of the IC (refer figure-8). This hot spotdo not have top layer metallization connection to contact window of any input pins.Usually hot spot is an artifact of oxide zapping/silicon punch-through resulting due to ESD.

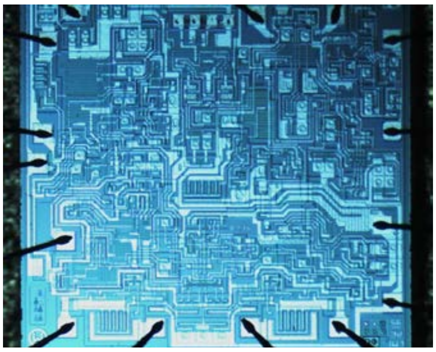


Figure-7: Optical photograph shows no visual anomalies on the die surface of IC SG1524.

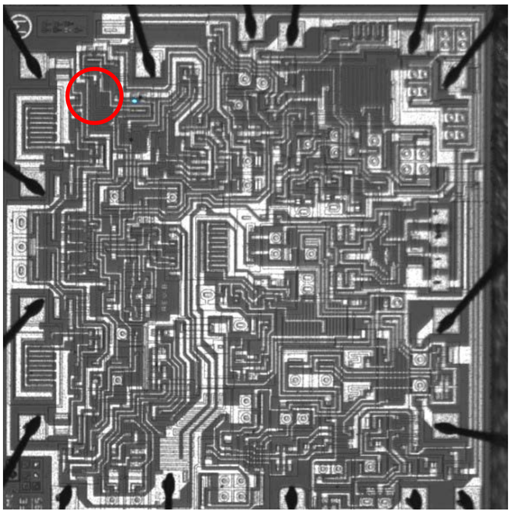


Fig.8:PEM photograph shows low intensity hot spot (blue colour) on the die surface of IC SG1524.

As the observed hot spot on t he die surface do n ot connect contact window of any I/O pin hence it is difficult to presume that such damage is due to ESD or EOS.As IC SG1524 is sensitive to ESD and is classified under class-1 ESD sensitivity level, hence ESD simulation study was conducted as per MIL-STD-883G method 3015, on IC SG1524 followed by PEM Analysis to detect hot spot, if any, on the die surface. As per the internal layout diagram of the device obtained from manufacturer's data sheet, there is an error amplifier within the IC, which is most ESD sensitive part. Input pins of this error amplifier i.e. pin no.1/2 of IC SG1524 were simulated with respect to ground pin no.8 with help of Human Body Model (HMB) ESD simulator. To compare the electrical characteristics of the good and ESD simulated IC, offset voltage parameter was chosen, because this parameter is most sensitive to ESD.The results are tabulated below.

Pre-ESD offset voltage of the IC	Applied ESD pulses	Post-ESD Offset voltage of the IC	PEM analysis Result
0.61mV	500V, 5 pulses	0.62mV	No visual defects observed
0.62mV	1000V, 5 pulses	0.59mV	No visual defects observed
0.59mV	1200V, 5 pulses	1.12mV	No visual defects observed
1.12mV	1400V, 5 pulses	1.06mV	No visual defects observed
1.06mV	1500V, 5 pulses	**7.89mV (specified limit (±5mV)**	Hot spot observed at the same location as that of failed IC (refer figure-9)
7.89mV	1700V, 5 pulses	**10.1mV**	Hot spot observed at the same location as that of failed IC (refer figure-10)

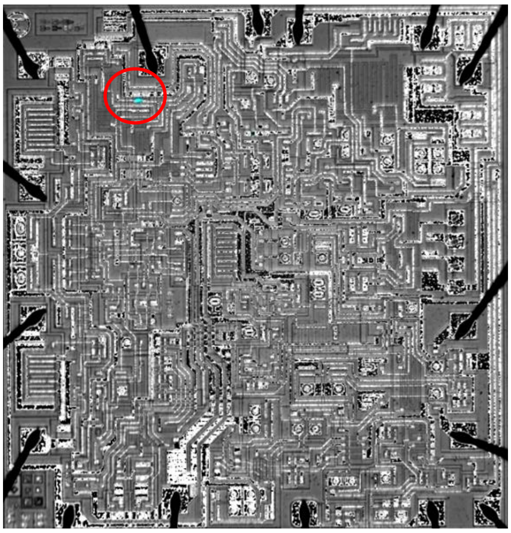


Fig.9: PEM photograph shows low intensity hot spot (blue colour) on the die surface of IC SG1524.

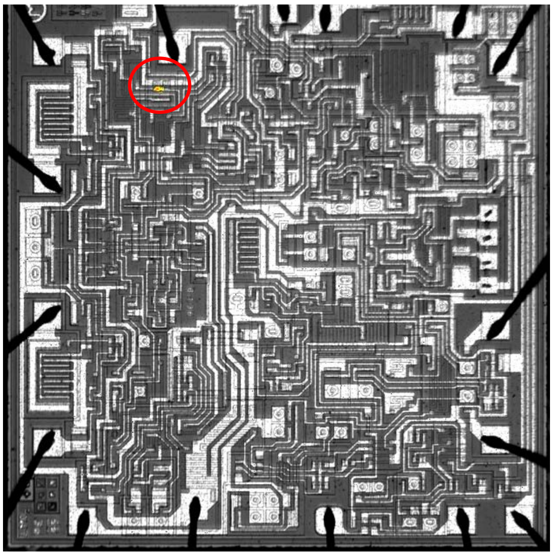
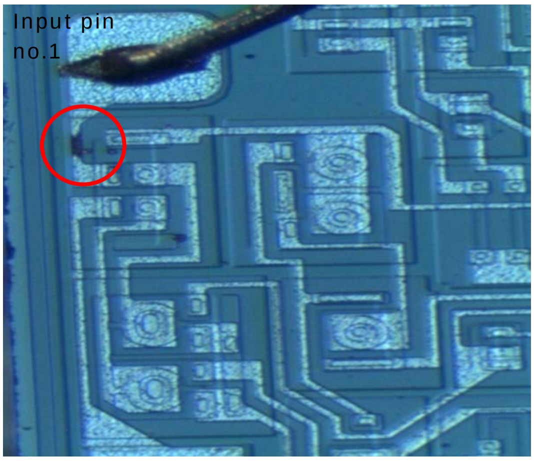


Fig.10: PEM photograph shows high intensity hot spot (red colour) on the die surface of IC SG1524.

Post-ESD PEM analysis revealed that hot spot on the ESD simulated IC is at same location of that of the field failure IC. This study also revealed that with increasing discharged voltage the ESD induced damage gets accumulated as reflected from the increased intensity of hot spots. Usually in a PEM

photograph, blue colour represents low intensity hot spots and red colour represents high intensity hotspot. Above discussion revealed that signature duo to ESD induced damage are surface and are not visible on the surface of the IC die with help of optical microscope and SEM. Only with help of photon emission technique these surface damages revealed their presence in term of hot spots. On the contrary, when the same device (SG1524) failed with reported failure "no output for a given input", failure analysis indicates EOS induced failure. Internal visual examination (Optical/SEM) revealed charring and opening of metallization connecting to input pin no.1 of the IC (refer figure-11).



IV. CONCLUSION

The failure modes observed between the devices suffering from EOS and ESD induced damages look alike and thus the two are normally regarded as one single failure category. However, physical analysis examples illustrated here demonstrate the subtle differences between the two. The main differences observed between EOS and ESD failure defects/signatures in devices from the failure analysis can be summarized as:

EOS

- usually with single damage spot
- concentrated failure site
- can be traced back to one starting point/interface where melting, fusing, etc. are initiated.

ESD

- usually with multiple discharge damage spots,
- discrete hit points **as** fail sites,
- follows certain discharge current flow pattern - most of the time towards the ground points
- cannot be traced back to a single starting point unless the overall discharge path is derived.

The study has clearly demonstrated the potential of a careful physical analysis to reveal the subtle yet often distinctive differences in failure signatures of EOS and ESD left behindin failed devices. Even though it is difficult to make a clear distinction between EOS and ESD failures based on theelectrical failure modes and signatures, careful physicalanalysis approaches, such as the one used in this investigation, can lead to accurate root cause identification in almost all cases. Further, using the physical failure analysis results, a discharge current path can be reconstructed to provide a better insight into the failure mechanisms.

ACKNOWLEDGEMENT

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Development of an In-house Software for Radiation Shielding Estimation of Spacecraft Electronic

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Abstract— **Estimation of optimum radiation shielding for spacecraft electronics is a challenging task considering the multiplicity of factors which influence this decision. It requires predicting environment radiation levels during mission life, modelling the spacecraft's mass shield configuration, applying dose computation algorithms and optimizing the shielding. The existing estimation tools are either proprietary or have the limitation that their source code is inaccessible and hence cannot be modified to meet project specific Radiation Hardness Assurance (RHA) guidelines. This paper presents an in-house developed simulation software 'DOSEMAP' for estimating local/package level shielding on flight electronic components for protection against Total Ionizing Dose (TID). The flow control of this software is presented with a discussion on each of its modules. The spacecraft modelling platform of DOSEMAP is based on a hierarchical approach - primary structure level, subsystem package level and component package level. As opposed to 3D Monte Carlo and NOVICE algorithms for total dose computation which require many hours of execution time, by using ray tracing technique DOSEMAP achieves an execution time of 5 to 15 seconds with high accuracy. DOSEMAP results have been validated by Total Radiation Dose Monitor (TRDM) payload in GSAT-2 and cross-validated with ASTRIUM's software DOSRAD.**

Keywords— **Total Ionizing Dose (TID), radiation shielding, DOSEMAP, Radiation Hardness Assurance (RHA), Total Radiation Dose Monitor (TRDM), ray tracing**

I. INTRODUCTION

Space radiation environment severely affects the performance of on board electronic components. With the accumulation of ionizing dose deposited by space radiation, device parameters drift from their normal values and the devices may even fail functionally [1]. These parametric drifts and functional failure of components can lead to degradation in circuit, subsystem and mission performance. Protection of spacecraft electronics from space radiation effects is an important activity for the success of a s pace mission.

One of the techniques to protect spacecraft electronics from ionizing effects of radiation is local/package level shielding of components so that the radiations are attenuated before they reach the sensitive component [2]. As the amount of shielding depends on the total dose received by a component over its mission life, the most important step in determining shielding for a component is estimating this total dose. An inaccurate estimation of total dose may result in under-shielding or over-shielding of the components. Under-shielding leads to decrease in component lifetime and hence is a threat to mission objectives. Over-shielding leads to weight penalty which limits mission capabilities and causes increased launch cost besides posing vibration problems. An accurate total dose determination can also justify the usage of rad-tolerant parts in place of rad-hard parts thus saving cost and component management efforts.

As the total dose deposited on a component depends on the spacecraft structure, subsystem package enclosure and component package, the process of estimating the dose received on a component requires 3D modelling of spacecraft. This calls for a software platform where the spacecraft can be modelled and dose calculation techniques can be applied. The already existing software are either proprietary or have the limitation that their source code is inaccessible and hence cannot be modified to keep pace with the ever evolving field of Radiation Hardness Assurance (RHA) and meet the project specific RHA guidelines. The software DOSEMAP addresses these limitations. Given the mission specific dose depth curve, this software provides an end to end solution for determining the shielding for electronic components.

The software DOSEMAP can be used by radiation hardness assurance engineers to map the total dose deposited at any component location inside the spacecraft. It is standalone software with its source code in C++ programming language. It runs on Windows operating systems and requires at least 512Mb RAM.

II. DOSEMAP FLOW CONTROL

As shown in Fig. 1, DOSEMAP consists of three modules. The first module consists of modelling the spacecraft 'built in' mass shielding configuration in terms of simple geometrical objects. The second module is the computation module where ray tracing algorithm is run on the spacecraft model. For estimating the total dose on a component, this algorithm takes mission specific dose vs. depth curve as an

input from a separate source. The output module gives the total dose received by the component over its mission life.

DOSEMAP provides an easy to use platform where the spacecraft structure, equipments, PCBs and component packages around the component chip can be modelled. The incorporation of modelling facility and dose calculation algorithm in the same software saves the efforts of users to import the models from third parties and hence provides an integrated usage environment.

The total dose received by a component depends on the spacecraft orbit and mission life. This information is contained in the mission specific dose vs. depth curve. Fig. 2 shows typical dose vs. depth curves for a GEO 15 year mission and a LEO 5 year mission. These curves give the dose deposited in silicon behind an aluminium spherical shield as a function of its mass thickness for a s pecific mission. This curve is obtained by simulating environment models for trapped protons and trapped electrons viz. AP-8 and AE-8 respectively and JPL 91 for solar proton events. SPENVIS (Space Environment Information Systems) is a convenient software to obtain such dose vs. depth curves for space missions [3].

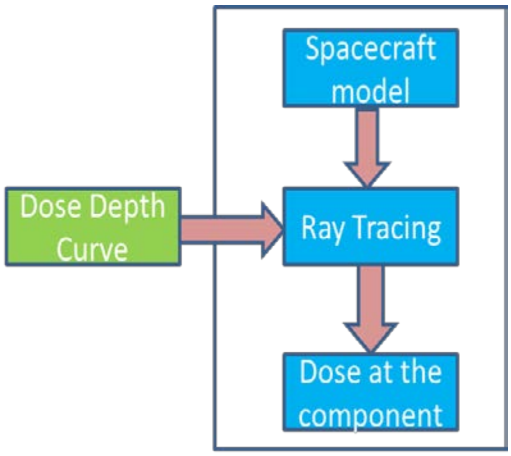

Fig. 1 DOSEMAP flow control

Based on the spacecraft mass model and mission specific dose depth curve, the dose deposited at component can be computed by a number of techniques like ray tracing, 3D Monte Carlo or NOVICE simulations. 3D Monte Carlo simulation is considered to be the most accurate but suffer from extremely large and impractical computation time. Even NOVICE simulations take between 1 to 9 hours for computing dose for a component [4]. As there are thousands of components used for a mission coupled with the fact that the process of dose calculation for a component is repeated many times for determining optimum shielding, it i s impractical to use such an algorithm. Hence the in-house developed software DOSEMAP incorporates ray tracing technique which gives a run time of 5 to 15 seconds. The computational error with this technique has been experimentally found to be only 5.68% by Total Radiation Dose Monitor (TRDM) payload in GSAT-2 [5]. Such small errors are taken care of by including Radiation Design

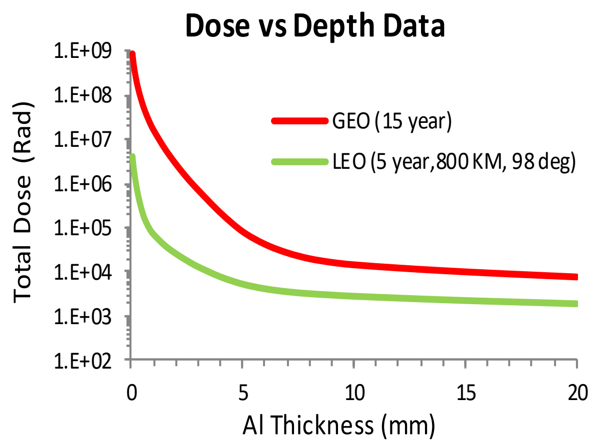

Fig. 2 Dose vs. Depth curve for GEO and LEO missions

Margin (RDM) in the shielding recommendation for any component.

III. SPACECRAFT MODELLING

It is known that constructing a spacecraft mass model with its subsystems, fuel tanks, oxidiser tanks, load cylinder, shear web, etc. using standard tools like CAD requires a large number of man-hours. DOSEMAP provides a platform where for radiation shielding estimation a spacecraft can be modelled with simple 3D geometrical objects like rectangular planes, circular planes, cylinders and spheres. Such a feature reduces the efforts and time that is spent on modelling complex geometries. DOSEMAP allows the use of right handed Cartesian co-ordinate system to define these geometrical objects. The thickness of representative objects is defined as mass thickness (g/cm^2) because dose attenuation by an object depends upon its thickness and density of its material.

The construction of spacecraft mass model can be considered as a three step process. As shown in Fig. 3, first the primary structural configuration of the spacecraft consisting of panels, shear webs, fuel tank, oxidiser tank, central CRPF structure is defined in terms of simple geometrical objects. The mass thickness of these objects is kept same as the in the spacecraft structure.

The second step is the construction of electronic subsystem package mass model. This includes defining package enclosure and PCBs of the package. Fig. 4 shows the modelling of an electronic package in DOSEMAP.

Thirdly the component package around the component chip is modelled. This is done using the same basic geometric objects as for spacecraft and subsystem package and is shown in Fig. 5. As component package contributes significantly to dose attenuation, an accurate definition of package can reduce the subsequent shielding weight and justify the usage of non rad-hard and COTS components

It is to be noted that the RHA guidelines may require considering the worst case scenario for estimating total dose so as to accommodate design changes and have the flexibility of mounting packages anywhere in the spacecraft. For this purpose, while preparing the mass model, the

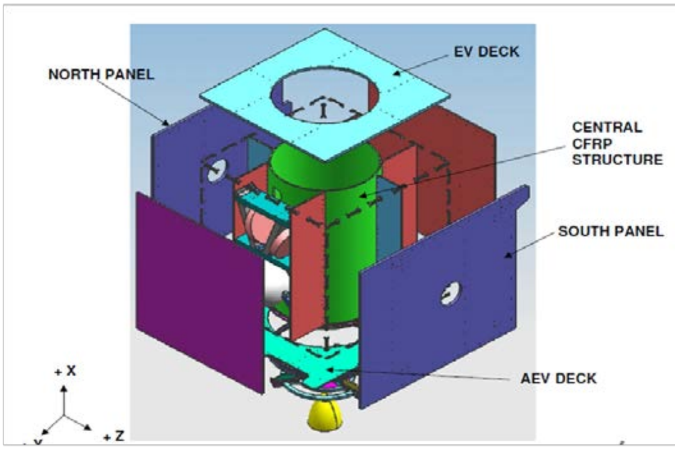

Fig. 3 (a) Candidate spacecraft primary configuration

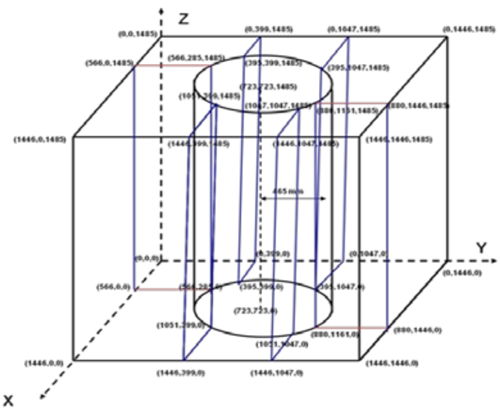

Fig. 3 (b) Equivalent model in DOSEMAP

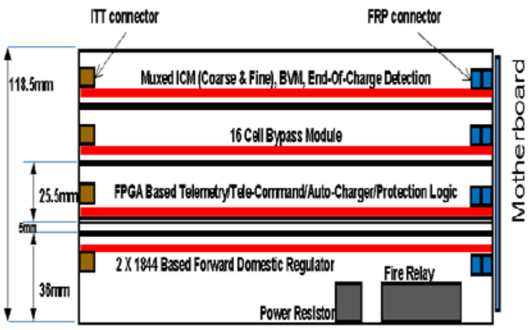

Fig. 4 (a) Subsystem electronic package

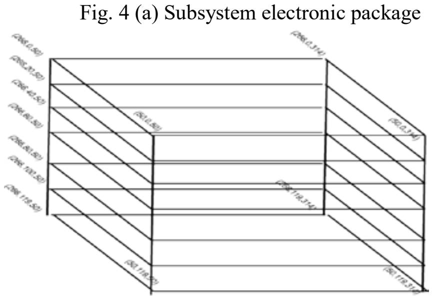

Fig. 4 (b) Equivalent model in DOSEMAP

package is considered to be mounted at a location which receives maximum dose (if known). And the location of the chip is considered to be on a PCB which receives maximum dose in the package. Although other components on same

PCB and on adjoining PCBs also shield the dose, for worst case estimation, they can be neglected.

As other components on the PCB surrounding the target component also attenuate the dose, this becomes significant if the density of components on the PCB is very large. As modelling each and every component requires a lot of modelling efforts, an approximation can be used [6]. An aluminium shield of thickness 2mm and height 5mm is placed at a distance of 25mm. This is supposed to simulate the adjacent component. If the projection of this shield at

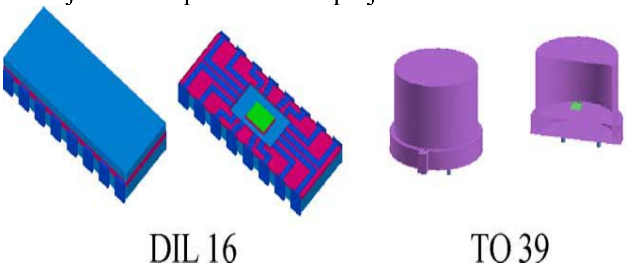

Fig. 5 (a) Electronic Component Package [4]

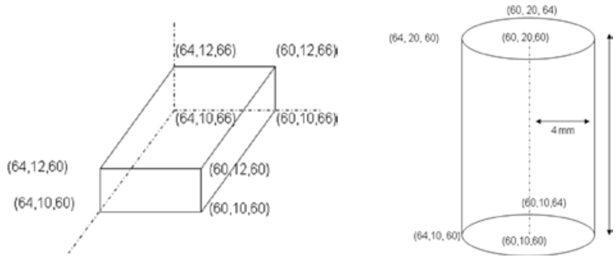

Fig. 5 (b) Equivalent model in DOSEMAP

panel is greater than perpendicular distance of the centre point of a sector from target chip, its shielding effect is to be considered and neglected otherwise.

IV. GRAPHICAL USER INTERFACE AND SYNTAX FOR CONSTRUCTING MASS MODELS

As shown in Fig. 6, DOSEMAP has a very friendly graphical user interface where user can easily define geometrical shapes representing spacecraft structure, subsystems, electronic packages, PCBs and component packages. Spacecraft model and dose depth data has to be submitted on a single page thus keeping the user free from unnecessary navigation. For new users, the steps to be followed are displayed on this page itself. Any spacecraft mass configuration change can be easily incorporated by making changes in the definition of objects. And from the viewpoint of production where satellite design remains more or less the same, changes can be made only in the dose depth curve before executing DOSEMAP. As shown in Table I, the syntax for defining these geometries is extremely simple in

DOSEMAP so that human error while defining objects is minimized.

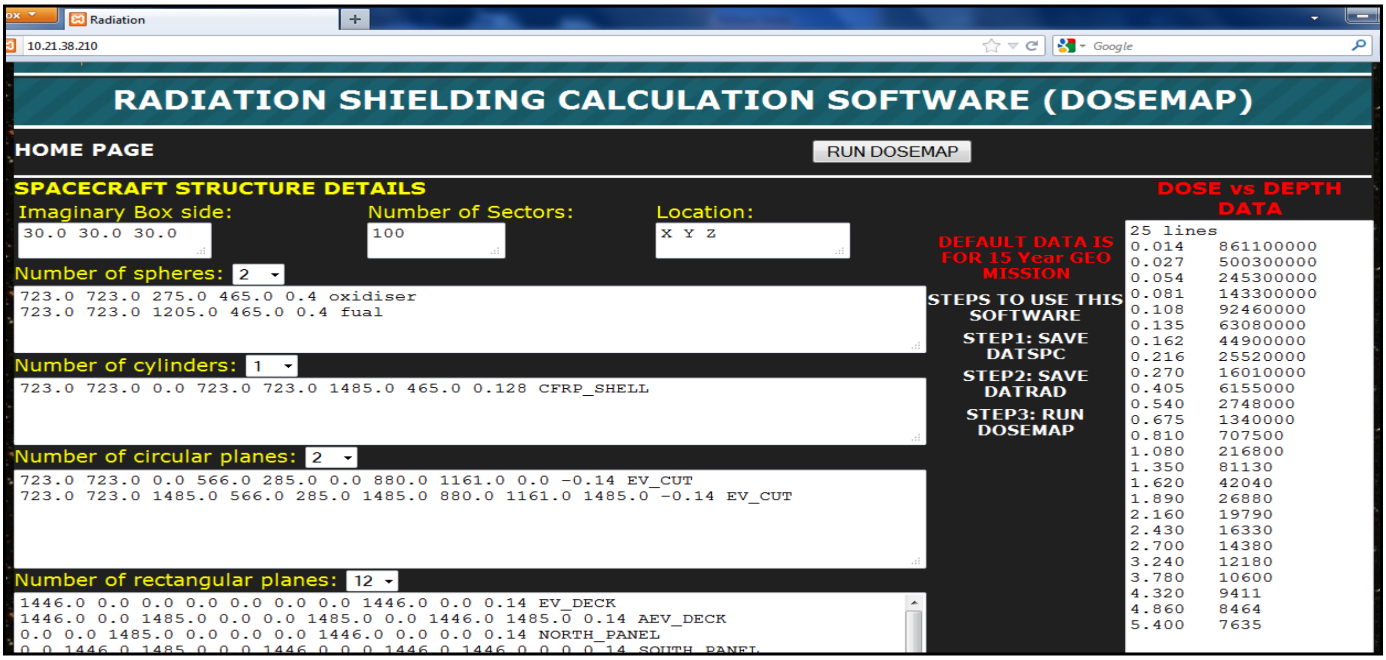

Fig. 6 Graphical User Interface in DOSEMAP

TABLE I
SYNTAX FOR DEFINING GEOMETRICAL OBJECTS

Object	Syntax	Remark
Rectangular plane	X1 Y1 Z1 X2 Y2 Z2 X3 Y3 Z3 T comment	(X1,Y1,Z1), (X2,Y2,Z2), (X3,Y3,Z3) are any three corners of rectangular plane. T is mass thickness.
Circular Plane	X1 Y1 Z1 X2 Y2 Z2 X3 Y3 Z3 T comment	(X1,Y1,Z1) is centre, (X2,Y2,Z2) and (X3,Y3,Z3) are any two points on boundary of circular plane. T is mass thickness
Cylinder	X1 Y1 Z1 X2 Y2 Z2 R T comment	(X1,Y1,Z1) and (X2,Y2,Z2) are top centre and bottom centre coordinates respectively. R is radius and T is mass thickness
Sphere	X1 Y1 Z1 R T comment	(X1,Y1,Z1) is centre of sphere. R is radius and T is mass thickness

V. RAY TRACING

Ray tracing technique finds applications in many fields including heat transfer, fluid flow calculations and computer graphics [8]. DOSEMAP uses this technique to estimate the dose received on the sensitive component. This algorithm is based on straight ahead approximation i.e. radiation penetrates in straight lines. The steps followed in this algorithm are as follows:

1. A detector point is selected on the component chip where total dose is to be calculated.
2. An imaginary cubic box is placed around detector point.
3. Each face of the imaginary box is divided into 10,000 sectors.
4. For computing dose received from one sector, a ray is launched from the detector point to the centre of sector as shown in Fig. 7. The mass thickness of objects intercepted by this ray on its way is added. Let it be T.
5. The dose received through this sector is determined from dose-depth curve. If Ω is the solid angle subtended by the sector on the detector point and D is the dose corresponding to thickness T in the dose depth curve, then dose received through this sector is given by ‘d’:

$$d = \frac{\Omega}{4\pi} D$$

6. The dose received through a face of imaginary box is

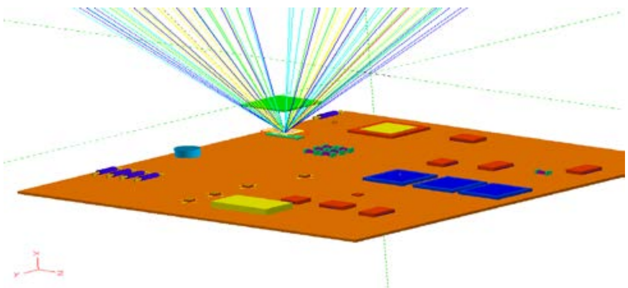

Fig. 7 Demonstration of ray tracing through one face of imaginary box [7]

```
==========================================================================
                       RAY TRACING SOFTWARE DOSEMAP
==========================================================================
              COPY RIGHT: ISRO SATELLITE CENTER, BANGALORE-560075
==========================================================================
        SIDE OF IMAGINARY BOX      SOLID ANGLE          TOTAL DOSE
==========================================================================
              XY0                    2.0944           7196.0913 KRAD
              XY1                    2.0944           2355.5073 KRAD
              XZ0                    2.0944           7196.0913 KRAD
              XZ1                    2.0944           1995.3009 KRAD
              YZ0                    2.0944          10779.4863 KRAD
              YZ1                    2.0944           1886.1024 KRAD
==========================================================================
            RESULTS                 12.5667          31408.5801 KRAD
==========================================================================
 TOTAL IONISING RADIATION DOSE AT (25.0,25.0,25.0) is:31408.6KRAD
==========================================================================
```

obtained by adding dose received through each sector on the face.

Fig. 8 Output from DOSEMAP

7. The total dose received at the detector location is the sum of dose received through each of the six faces.

It is to be noted that by increasing the number of sectors into which the face of the imaginary box is divided, better accuracy in total dose estimation is achieved. However as a trade-off it requires more execution time. 10,000 sectors per face find middle ground with acceptable accuracy and execution time.

VI. TOTAL DOSE AT DETECTOR POINT

DOSEMAP estimates the total dose received at the detector point from six faces of the imaginary box and displays the same in output as shown in Fig. 8. This gives the radiation analyst an indication of the “weak sides” from where the dose received is comparatively higher. This forms a useful input to select the best line of attack (shielding on top or side of component). The total dose received at the detector point from all sides shown in the output window is an indispensible parameter in radiation shielding analysis.

VII. RADIATION SHIELDING ANALYSIS BASED ON DOSEMAP OUTPUT

Radiation Design Margin (RDM) is defined as the ratio of component radiation hardness to the total dose received by it over mission life. As shown in Fig. 9, based on the dose estimated by maiden run of DOSEMAP, it can be known if device can survive the mission total dose level (i.e. component hardness > total dose) and RDM is met. If it is not so, the shielding option which is feasible (depending on the component package structure) and looks most optimum is included in the geometry profile of spacecraft model. The DOSEMAP is re-run with this new model. This process is repeated until RDM requirement is satisfied. Thus it is seen that in estimating the radiation shielding for any component DOSEMAP is executed a large number of times. This justifies the use of ray tracing technique in DOSEMAP over 3D Monte Carlo and NOVICE simulations which take hours of execution time

VIII. VALIDATION OF DOSEMAP SOFTWARE

DOSEMAP has been experimentally validated by its close estimation of total dose on dosimeters of Total Radiation Dose Monitor (TRDM) payload of GSAT-2 satellite. To further validate results of DOSEMAP, a comparison is made between DOSEMAP and contemporary software DOSRAD for a hypothetical model [9]. DOSRAD has been used by ASTRIUM for total dose estimation for over a decade now and is claimed to be cross validated with NOVICE simulations [10]. The hypothetical model used for this comparison is shown in Fig. 10. It consists of:

1. Aluminium sphere: hollow, diameter 1000mm, thickness 1mm, centered on the origin
2. Aluminium box: dimensions X=500mm, Y=-300mm, Z=200mm , thickness 2mm, centre at the origin
3. PCB: dimensions X=400mm, Y=250mm, Z=1.6mm, thickness 1.6mm, centre at the origin
4. Kovar Cube: side = 10mm, thickness = 0.25mm, centre at X = -150mm, Y= 100mm, Z = 7.8mm
5. Ceramic Box: dimensions X =20mm, Y=40mm, Z=20mm, thickness 2mm, centre at X=150mm, Y=100mm, Z=12.8mm
6. Steel cylinder: diameter 10mm, height 20mm (Z direction), thickness 1.5mm, centre at X=150mm, Y=-100mm, Z=12.8mm

Considering an imaginary cube of side 2mm, total dose was computed by using DOSEMAP and DOSRAD separately at the following four locations:

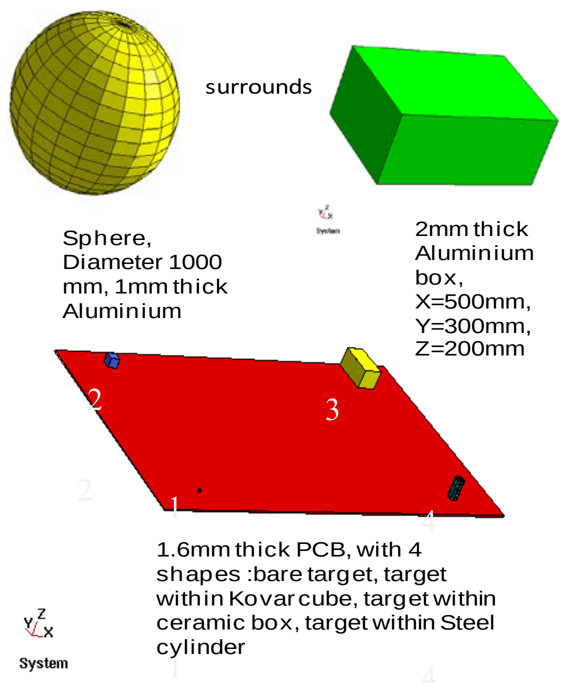

Fig. 10 Model for cross-validation of DOSEMAP with ASTRIUM’s DOSRAD

1. X= -150mm, Y= -100mm, Z= 3.8mm

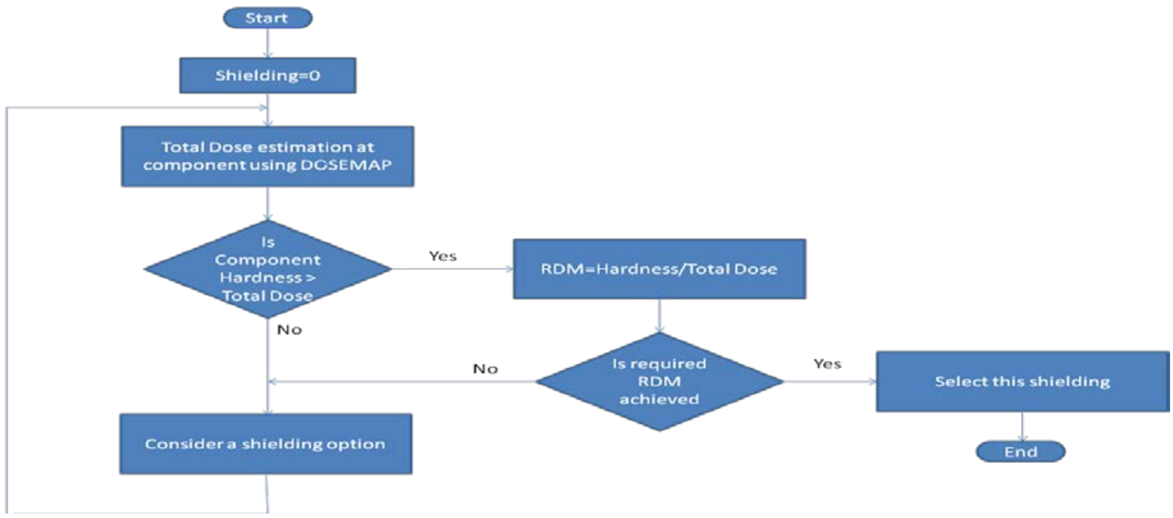

Fig. 9 Radiation shielding analysis flow

X= -150mm, Y= 100mm, Z= 7.8mm
2. X= 150mm, Y= 100mm, Z= 12.8mm
3. X= 150mm, Y= -100mm, Z= 12.8mm

TABLE II
COMPARISON OF DOSRAD AND DOSEMAP RESULTS FOR THE HYPOTHETICAL MODEL

Location	DOSRAD	DOSEMAP	Delta (%) Between DOSEMAP & DOSRAD
1	280 krad	328.0 krad	17.14 %
2	122 krad	145.9 krad	19.59 %
3	42.5 krad	49.4 krad	16.23 %
4	14.6 krad	14.8 krad	1.4 %

Table II shows that the total dose predicted by DOSEMAP is higher as compared to DOSRAD. This is because of a conservative approach followed in DOSEMAP which interpolates the dose vs. depth data points linearly as opposed to curve fitting in DOSRAD. This has been done to provide additional factor of safety. Hence the shielding estimation by DOSEMAP will always be more protective.

IX. CONCLUSION

Estimation of total dose received on electronic component over the mission life is an indispensible activity in radiation hardness assurance of any space mission. The software DOSEMAP stands as a good tool to carry out this activity. Being in-house developed it takes away the need to look to proprietary software and allows the modification of its source code in accordance with project requirements. It provides a good platform to model spacecraft with simple geometrical figures. Good graphical user interface along with simple syntax for defining objects make it very user friendly. As opposed to 3D Monte Carlo and NOVICE simulations, the incorporation of ray tracing technique in DOSEMAP reduces the execution time to a few seconds and makes it useful for practical estimations. The output format of DOSEMAP gives a hint of "weak sides" which is an important input to consider the merit of a shielding option. The validation of DOSEMAP is established by TRDM payload of GSAT-2 satellite and cross validation with ASTRIUM's software DOSRAD. DOSEMAP has established itself as a powerful and reliable tool for shielding estimation of spacecraft electronics. To enhance the capability of this software, the geometrical object database can be expanded in future by including figures like prism, cone and pyramid. Also stopping power correction factor of shielding materials can be implemented for better shielding estimation of extremely sensitive components.

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Radiation Environment Analysis for Electronic Components On-board Spacecraft in Low Earth Orbits

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***Abstract*— Radiation Hardness Assurance for EEE components in Low Earth Orbit (LEO) spacecraft missions is indispensible to ensure that on-board electronic systems render their designed reliable performance. The variability in LEO orbital parameters such as altitude and inclination coupled with varying solar activity conditions during the mission lifetime necessitates the need for conducting a top-down analysis to evaluate the damaging effects of LEO space radiation environment on electronic components. In the present paper, radiation environment has been analyzed for an orbital parameter matrix consisting of i) altitudes ranging from 500 km to 1000 km & ii) inclinations ranging from 0° to 98°. The analysis shows that charged particle flux varies by orders of magnitude with altitude and inclination. The results obtained in this work reveal that i) electronic components on-board spacecraft in low inclination orbits experience lesser Total Ionizing Dose (TID) than polar orbits ii) the geomagnetic shielding has a profound effect on protecting low earth orbits with inclination less than 50° from the lethal solar radiation particles emitted during Solar Flares & Coronal Mass Ejections. The conclusions drawn from this work can be used by LEO spacecraft system designers for making informed decisions regarding selection of electronic components and appropriate mitigation techniques.**

***Index Terms*— Van-Allen Belt, Solar Particle Event, Galactic Cosmic Rays, Total Ionizing Dose, LET, Single Event Effects, South Atlantic Anomaly.**

I. INTRODUCTION

Low Earth Orbit (LEO) radiation environment presents harsh operating conditions for on-board electronic systems. It leads to cumulative effects like Total Ionizing Dose (TID) effects and Displacement Damage (DD) effects & a host of transient effects like Single Event Upset (SEU), Multiple Bit Upset (MBU), Single Event Latch-up (SEL), Single Event Gate Rupture (SEGR), Single Event Burnout (SEB), Single Event Function Interrupts (SEFI) and Single Event Snap-Back (SESB). These effects lead to performance degradation of electronic components and eventually their failure leading to system anomalies.

Conventionally the approach to deal with radiation environment starts at subsystem design stage after the mission orbital parameters are frozen. This approach leads to several radiation reliability issues, shielding weight penalties and poses limitations for using high performance components with lesser radiation thresholds. The emergence of advanced electronic components with increased sensitivity to space radiation effects has led to evolution of new mission design approaches.

One such approach is to consider radiation environment effects on electronic components before freezing the orbital parameters such as altitude, inclination, etc. This approach would address the reliability issues associated with space radiation effects on electronic components thereby leading to higher system design robustness. However such an approach requires an extensive analysis of LEO radiation environment because of the possible variations in LEO orbital parameters such as altitude and inclination. Accounting for these factors is an integral part of radiation environment analysis for LEO missions.

The present study focuses on radiation environment analysis for different representative LEO altitudes and inclinations which forms the foundation for the emerging mission design approach described above. The results obtained in this analysis give a comprehensive view of Solar Particle Events (SPE) and Galactic Cosmic Rays (GCR) environment for low inclination orbits, effectiveness of geomagnetic shielding on LEO radiation environment and better understanding of South Atlantic Anomaly (SAA) impact on electronic components. The results can be used by system designers to make informed decisions while selecting electronic components for LEO missions and apply appropriate mitigation techniques to deal with radiation effects.

II. LEO RADIATION ENVIRONMENT

Wherever Times is specified, Times Roman or Times New Roman may be used. If neither is available on your word processor, please use the font closest in appearance to Times. Avoid using bit-mapped fonts. True Type 1 or Open Type fonts are required. Please embed all fonts, in particular symbol fonts, as well, for math, etc.

A. Van Allen Belts

Electrons and protons are “trapped” in earth’s magnetic field. These particles are trapped because the earth’s magnetic field constrains their motion perpendicular to the magnetic field. The electromagnetic Lorentz force is directly responsible for restraining a trapped charge particle and keeping it well within a defined region around earth. This region is called Van Allen Belts. As a result of the forces

acting on the particles, they spiral around magnetic field lines, oscillating back and forth between the northern and southern hemispheres.

The population of charged particles trapped by the earth's magnetic field consists mainly of protons with energies between 100 keV and several hundred MeV and electrons with energies between a few tens of keV and 10 MeV. Population of trapped particles is very dynamic and gets affected by solar cycle, secular changes in the geomagnetic field, magnetosphere conditions and low altitude atmosphere interaction. The separation of the geographic magnetic dipole centre from the earth's centre and the inclination of the magnetic axis with respect to the rotation axis produce a local depression of magnetic field in the South Atlantic region. It leads to penetration of trapped particles to altitude as low as 300 km. The charged particles trapped in this region pose a hazard to operation of spacecraft electronics which is commonly known as 'South Atlantic Anomaly' [1].

B. Solar Particle Events (SPE)

The charged particle environment in near-earth region is dominated by the activity of the sun, which acts as both a source of charged particles and a modulator of trapped particle flux in Van Allen Belts. It is for example a source of protons and heavy ions via the periodic high-energy solar events that increase the number of particles. The two storm phenomena occurring on the sun (likely during its maximum activity phase) that affect particle levels are Solar Flares and Coronal Mass Ejections (CMEs). These events lead to changes in solar wind density and velocity and the interactions between these disturbances and earth magnetosphere causing perturbations known as magnetic storms and substorms.

Solar activity is identified by the sunspot numbers. The solar activity is divided in two main phases: one maximum activity phase lasting approximately seven years and one low activity period lasting about four years. The high activity phase is generally illustrated by exceptional events lasting several days emitting mainly high-energy protons; but at the same time, this intense activity enhances solar wind emission acting as a shield against Galactic Cosmic Rays [2].

C. Galactic Cosmic Rays (GCR)

The earth's magnetosphere is bombarded by Galactic Cosmic Rays having nearly isotropic flux of energetic charged particles, primarily the nuclei of atoms stripped of all electrons. These comprise of 85% protons (hydrogen nuclei), 14% α-particles or helium nuclei, and 1% heavier ions covering the full range of elements. They are partly kept out by the earth's magnetic field and have easier access at the poles compared to the equator. Solar cycle provides modulation to GCR flux as it is in antiphase with the sunspot cycle [3].

III. SELECTION OF REPRESENTATIVE LEO MISSIONS FOR ANALYSIS

Earth has its own magnetic field which traps charged particles close to the earth and also acts as shield for particles coming from outside (GCR and SPE). Therefore the radiation environment for LEO missions depend upon altitude and inclination of orbit. Representative LEO missions were chosen with orbital altitude varying from 500 km to 1000 km and inclination from 0° to 90°. Table 1 shows the matrix of altitude and inclination included for analysis in the present work.

TABLE I. INCLINATION AND ALTITUDE OF ORBITS CONSIDERED FOR ANALYSIS.

		Altitude (km)					
		500	**600**	**700**	**800**	**900**	**1000**
Angle of Inclination	**0°**	√	√	√	√	√	√
	10°	√	√	√	√	√	√
	20°	√	√	√	√	√	√
	30°	√	√	√	√	√	√
	40°	√	√	√	√	√	√
	50°	√	√	√	√	√	√
	60°	√	√	√	√	√	√
	70°	√	√	√	√	√	√
	80°	√	√	√	√	√	√
	90°	√	√	√	√	√	√
	98°	√	√	√	√	√	√

IV. RESULTS AND ANALYSIS

The analysis has been carried out considering a representative case of a mission with 1 January 2017 as the launch date and a life of 5 years. Various space radiation environment models have been used to obtain particle spectrums such as AP-8 (trapped protons), AE-8 (trapped electrons), JPL-91 (solar proton fluence), and CRÈME 96 (heavy ion and solar proton integral flux). To account for the interaction of space radiation charged particles with spacecraft materials, various charge transport codes have been used such as SHIELDOSE-2 (Dose Depth Data) and JPL Si (Displacement Damage). Radiation environment for orbits mentioned in Table 1 is analyzed using ESA's SPACE ENVIRONMENT INFORMATION SYSTEM (SPENVIS) software.

A. Integral Average Trapped Proton Flux

Variation of Integral Average Trapped Proton Flux for Energy > 30 MeV with altitude (varying from 500 km to 1000 km) and inclination (varying from 0° to 98°) is shown in Figure 1. It can be seen that proton flux increases with increase in altitude. The figure shows that proton flux is the highest for orbits with inclination close to 30°. The possible reason for this observation is the more number of spacecraft passages through South Atlantic Anomaly (SAA) region. It is also noted that for 900 km and 1000 km orbits, there is slight dip in the proton flux at 10° inclination. This observation can be attributed to the fact that at such high altitudes and 0° inclination, the spacecraft starts passing

through inner Van-Allen Belt and hence experiences greater proton flux.

B. Integral Average Trapped Electron Flux

Variation of Integral Average Trapped Electron Flux for E>0.5 MeV with altitude (varying from 500 km to 1000 km) and inclination (varying from 0° to 98°) is presented in Figure 2. A general trend can be seen that electron flux increases with increase in altitude. The figure suggests that for all the altitudes, the electron flux is the highest for inclinations between 60° and 70°. This is due to passages of satellite through Van-Allen belts. A very interesting observation can be made from Figure. 1 which shows spikes in electron flux for 900 km and 1000 km orbits with inclinations close to 30°. This increased flux is most likely to result from the passage of the spacecraft from South Atlantic Anomaly (SAA) region.

C. Integral Solar Proton Fluence

Variation of Integral Solar Proton Fluence for E>30 MeV with altitude (varying from 500 km to 1000 km) and inclination (varying from 0° to 98°) is provided in Figure 3. It is seen that Solar protons are not available in the representative low earth orbits with inclination less than 50°. Such an observation points to the profound effect of geomagnetic shielding for inclinations below 50°. The continuous decrease in geomagnetic field strength beyond 50° leads to increase in solar proton fluence and it attains peak at 90° inclination. It is noted that dependence of Solar proton fluence on altitude of orbits is very less. The underlying reason behind this observation is that the geomagnetic field strength is a much stronger function of inclination than altitude.

D. Total Ionising Dose (TID) for LEO On-board Electronic Components

For estimation of TID at chip level using ray tracing technique, dose-depth curve applicable for the mission is required. Dose-depth curves provide the TID levels deposited behind a given shielding thickness (or mass thickness) in a target (or detector). Currently, the shielding shape used for dose-depth curve determination is an aluminium solid sphere with the detector located at the center of the sphere. In order to best represent the die material of an electronic device, the material of the target is considered to be silicon. Typical shielding provided by device package style, electronic housing and spacecraft is equivalent to 3 mm Aluminium or more. Figure 4. presents the dose-depth curves obtained for orbit altitudes ranging from 500 km to 1000 km and inclinations ranging from from 0° to 98°. It can be seen that TID for LEO missions increases with increase in altitude of orbit. Two peaks are observed-one at around 30° inclination and the other at inclination close to 70°. The first peak close to 30° is due to South Atlantic Anomaly region and second peak close to 70° is due to higher spacecraft dwell duration in inner Van-Allen Belt.

In this paper, TID estimation was carried out for the electronic components using total mission dose and thickness data given in Figure. 4. a nd using ray tracing based in-house developed software 'DOSEMAP'. EV, AEV, north and south panel thickness considered is equivalent to 0.6 mm Al. East and west panel thickness considered is equivalent to 0.4 mm Al. For total dose estimation 1 mm thick Al package housing with dimension 200 mm X 200 mm X 200 mm and 4 PCBs mounted inside package is considered. Total dose received by component die has been calculated for different package styles such as DIP14. For DIP14 components mounted inside the spacecraft, such calculated TID levels are presented in Figure 5 while Figure 6 shows the TID levels for such components when mounted outside the spacecraft. It may be noted that the data presented in these figures does not consider any spot shielding over the component die.

E. Displacement Damage Dose

In LEO orbits, Displacement Damage in optical components is caused by trapped proton and solar protons. Figures 7 and 8 show the Displacement Damage Dose (DDD) vs Depth and Displacement Damage Equivalent Fluence (DDEF) vs Depth data respectively for typical 3 mm Al equivalent shielding. The graphs show that DDD and DDEF increase with increase in altitude of low earth orbit. For altitudes more than 700 km, both DDD and DDEF are maximum at 30° inclination while for altitudes less than 700 km, DDD and DDEF are maximum for 98° inclination orbits. This is because of the higher proton flux encountered in the South Atlantic Anomaly region at around 30° and weaker geomagnetic shielding for solar protons at polar orbits.

F. Integral Peak Tapped Proton Flux

Variation of Integral Peak Trapped Proton Flux for Energy>30 MeV with altitude (varying from 500 km to 1000 km) and inclination (varying from 0° to 98°) is given in Figure 9. It is observed that the Integral peak trapped proton flux increases with increase in altitude of orbit for a given inclination. The Integral peak trapped proton flux increases with inclination upto 30°. However for inclinations above 30° very small variation in peak flux has been observed. This is because orbits with inclination less than 30° will never enter into the peak flux region of South Atlantic Anomaly (SAA). All orbits with inclination more than 30 ° will pass through high flux region of SAA. So highest error rate in low SEE threshold devices is same for all orbits with inclination more than 30° but total number of errors during mission will depend upon the total number of passes through SAA.

G. Integral GCR Proton Flux

Figures 10, 11 and 12 show the variation in Integral GCR Proton Flux for inclinations 10°, 20° and 98° respectively for altitudes ranging from 500 km to 1000 km. It is observed that GCR protons are available for all inclinations therby re-affirming the high energy nature of GCR protons. The figures clearly show that the GCR proton flux is maximum for polar orbits but dependence on altitude is very less.

H. Integral Worst Day Solar Proton Flux

The Integral Worst Day Solar Proton Flux was analyzed for low earth orbits with altitudes ranging from 500 km to 1000 km and inclinations ranging from 0° to 98°. It was observed that solar protons are not available for orbits with inclination less than 50°. This observation is attributed to the geomagnetic shielding. For the remaining inclinations, the Integral Worst day solar proton spectra for 98° inclination orbits was found to be having the maximum flux. As for SEE rate determination, maximum flux is the quantity of interest, the same is presented in Figure 13. It can be seen from the figure that Solar proton flux is maximum for polar orbit and there is a less dependence on altitude of orbit.

I. Integral Worst Day Heavy Ion Flux

Integral Worst Day Heavy Ion Flux is analyzed for representative missions of Table 1. A stark contrast in flux levels was observed for low inclinations and high inclinations. Figures 14, 15 and 16 present the data for inclinations of 10°, 20° and 98° respectively. From the figures it is clear that heavy ions flux is almost independent of altitude of orbit but it s trongly depends upon angle of inclination. As can be seen from the figures, the flux is many orders of magnitude higher for polar orbits. This observation can be attributed to the absence of geomagnetic shielding in polar orbits.

At this stage, a need was felt to compare the flux with other missions such as GEO and interplanetary. Figure 17 shows the Integral Heavy ion Spectra under worst day condition for LEO (800km, 20°), LEO (800km, 98°), GEO and interplanetary Mission. From the figure, it is clear that heavy ions flux for GEO and interplanetary missions are almost same but the flux is less for LEO.

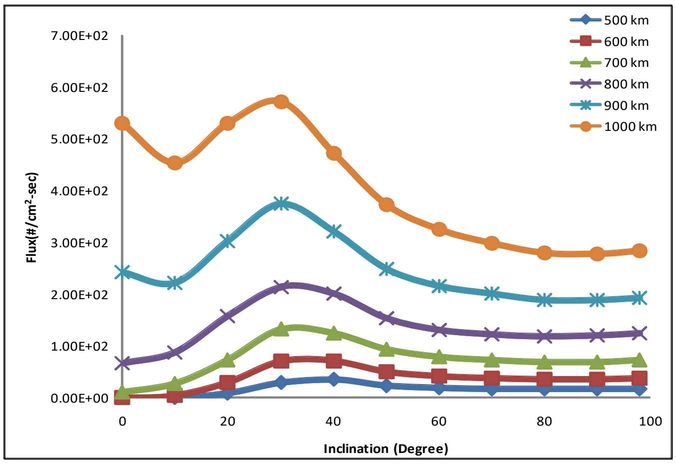

Figure 1. Integral Average Trapped Proton Flux for E>30 MeV

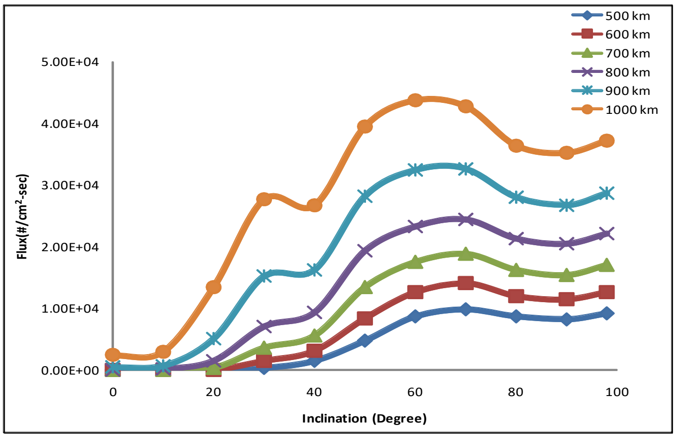

Figure 2. Integral Average Electron Flux for E>0.5 MeV

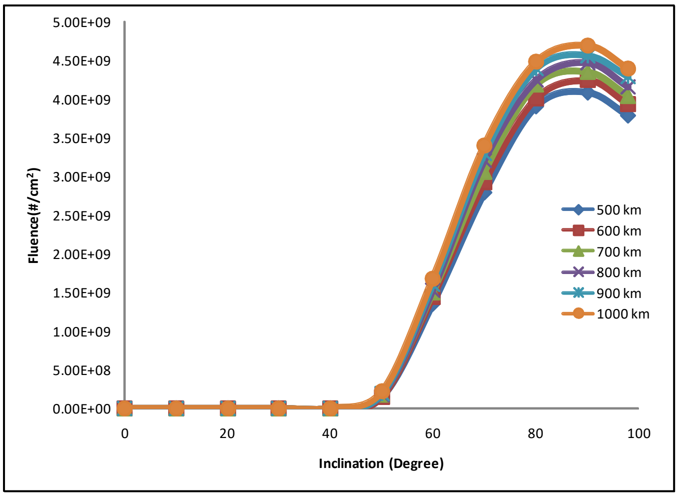

Figure 3. Integral Solar Proton Fluence for E>32 MeV

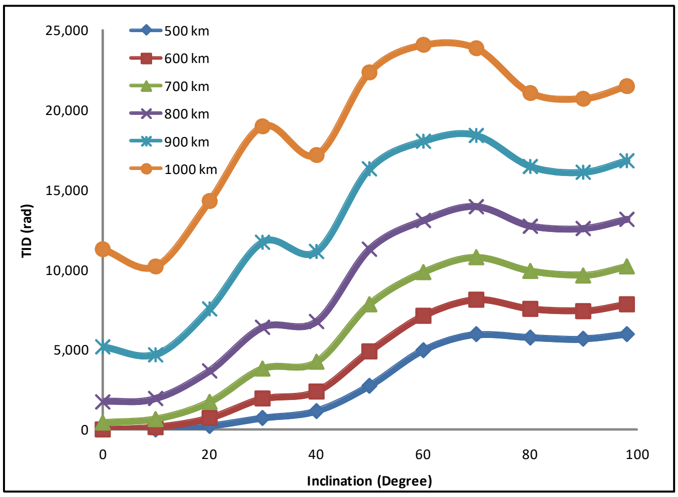

Figure 4 Total Ionising Dose for 3 mm Equivalent Spherical Aluminum shield

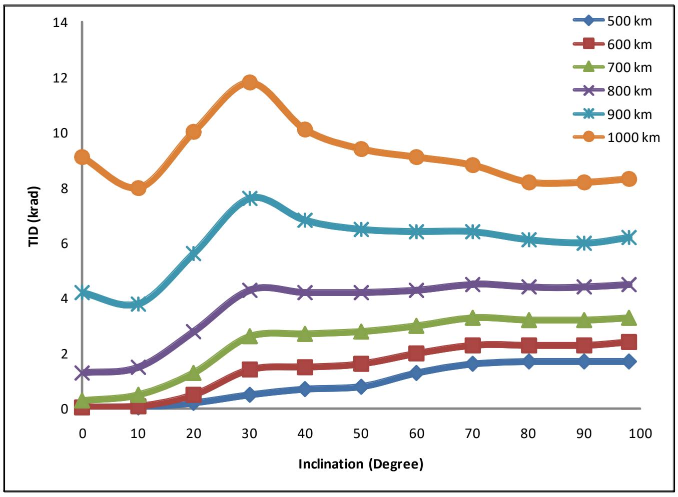

Figure 5. TID for DIP14 Component in an Electronic Package Mounted Inside Spacecraft

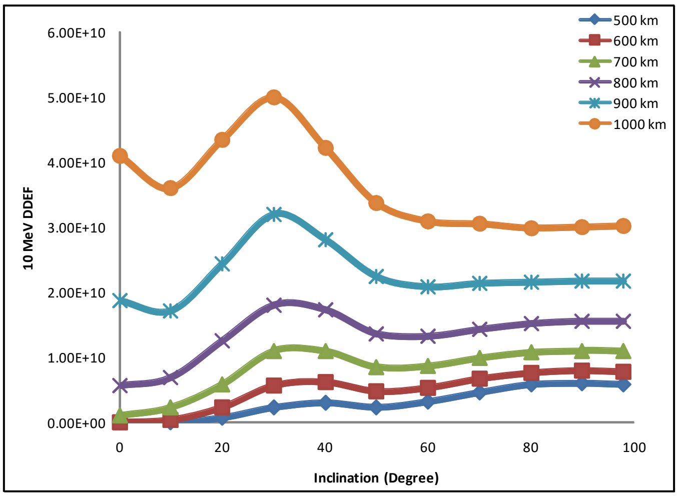

Figure 8. Displacement Damage Equivalent Fluence (DDEF) for 3 mm Equivalent Spherical Aluminum shield

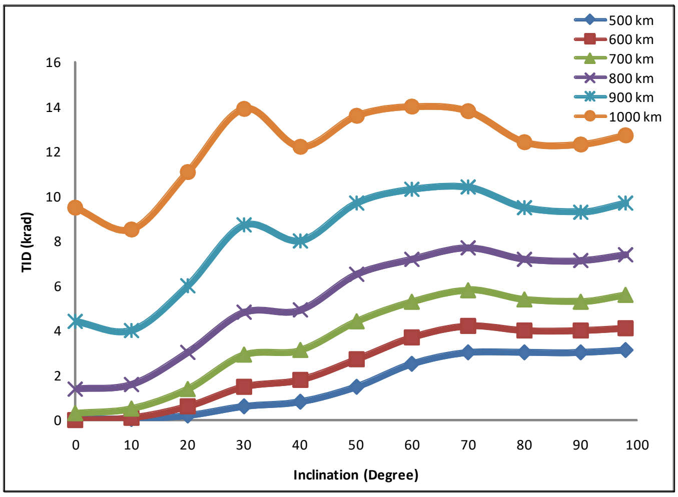

Figure 6. TID for DIP14 Component in an Electronic Package Mounted Outside Spacecraft

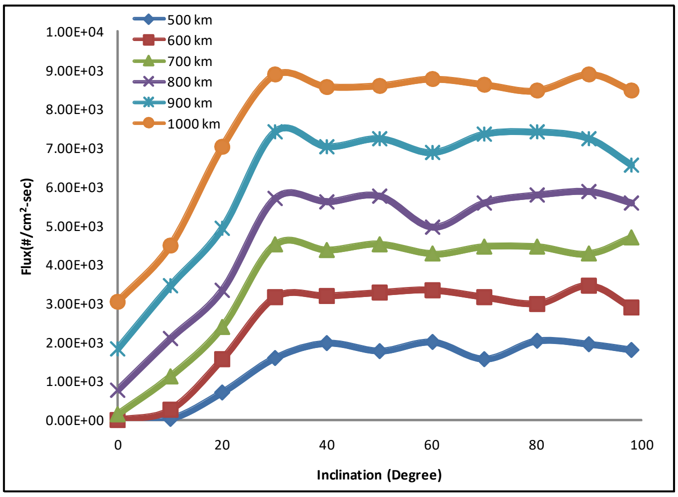

Figure 9. Integral Peak Trapped Proton Flux for E>30 MeV

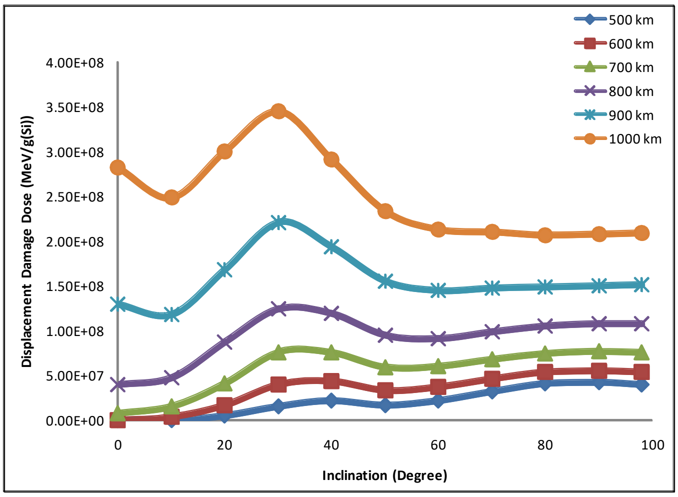

Figure 7 Displacement Damage Dose for 3 mm Equivalent Spherical Aluminum shield

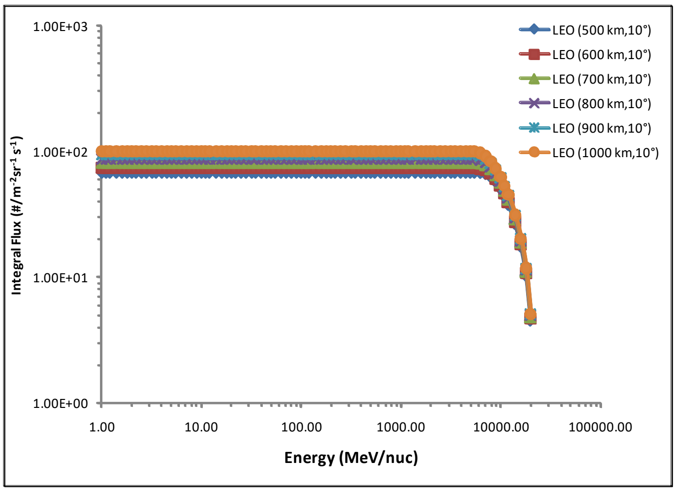

Figure 10. Integral GCR proton spectra for 10° inclination orbits

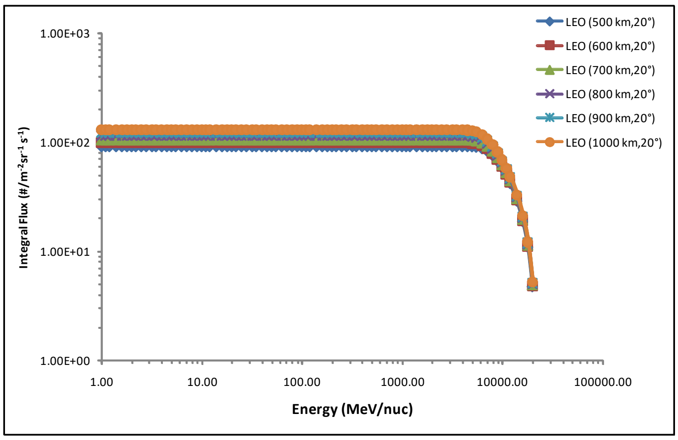

Figure 11. Integral GCR proton spectra for 20° inclination orbits

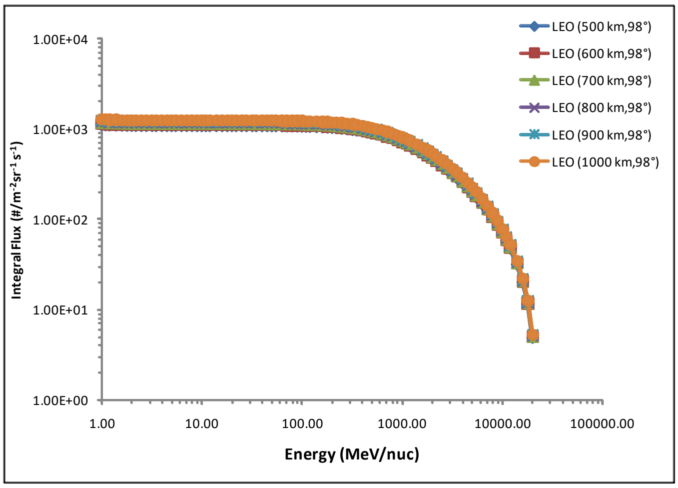

Figure 12. Integral GCR proton spectra for 98° inclination orbits

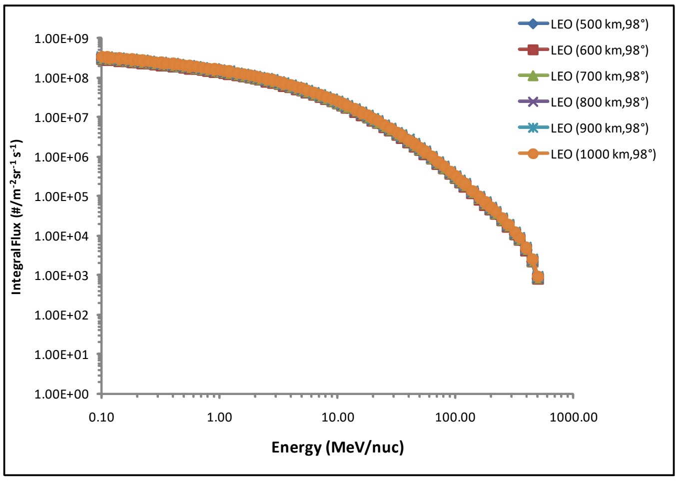

Figure 13. Integral worst day solar proton spectra for 98° inclination orbits

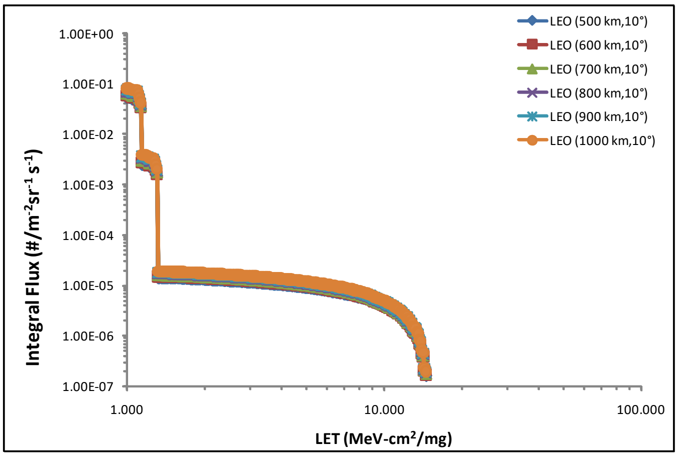

Figure 14 Integral Heavy ion Spectra under worst day condition for a component shielded by 100 mil shielding for 10° inclination orbits. The predication is for 1 AU.

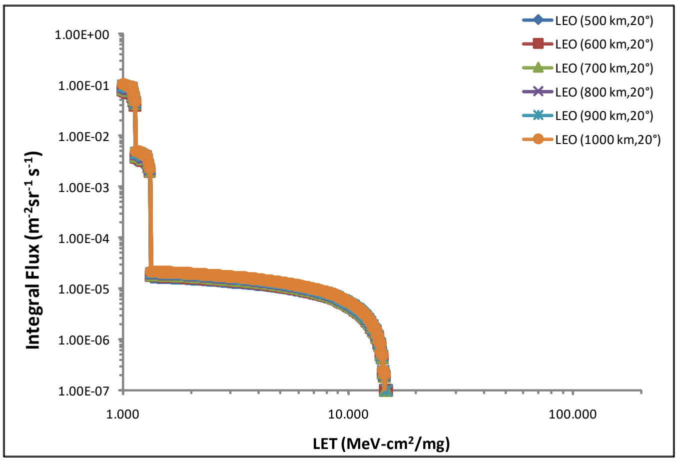

Figure 15. Integral Heavy ion Spectra under worst day condition for a component shielded by 100 mil shielding for 20° inclination orbits. The predication is for 1 AU.

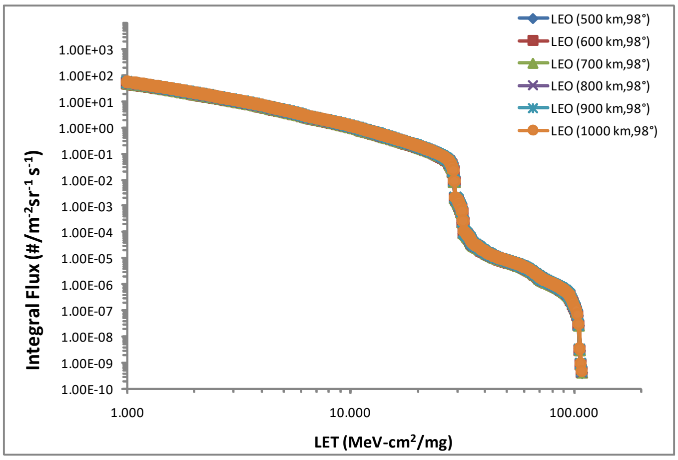

Figure 16. Integral Heavy ion Spectra under worst day condition for a component shielded by 100 mil shielding for 98° inclination orbits. The predication is for 1 AU

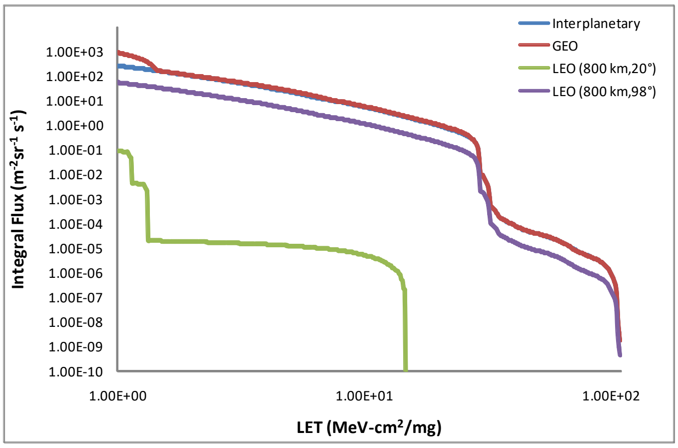

Figure 17. Integral Heavy ion Spectra under worst day condition for a component shielded by 100 mil shielding for LEO (800,20º), LEO (800,98º), GEO and Interplanetary Mission. The predication is for 1 AU.

V. CONCLUSION

Integral Average Trapped Proton & Electron Flux in low earth orbits show strong dependence on orbit inclination and altitude. However Solar protons vary little with low earth orbit altitude but exhibit a strong dependence on angle of inclination beyond 50°. As a result the TID, DDD and DDEF variations are observed with altitude and inclination variations in LEO. From the point of view of TID hardness assurance, low inclination and low altitude orbits are better than polar and high altitude orbits. Although DDD and DDEF varies with altitude and inclination but the maximum value of these quantities obtained in the analysis presented in this work is less than the radiation hardness of most of electronic components.

The Integral GCR Proton Flux and Integral Worst Day Solar Proton Flux show strong dependence on LEO angle of inclination such that polar orbits present an increased risk of proton flux for LEO spacecraft. It has been also shown that due to South Atlantic Anomaly, the Integral Peak Trapped Proton flux is high for 30° inclination orbit. These results lead to an important conclusion that appropriate mitigation techniques are required if devices with LET threshold less than 15 MeV-cm2/mg are used for such orbits. The analysis also shows that the Integral Worst Day Heavy Ions Flux is dependent on the angle of inclination but does not vary significantly with orbit altitude. The high LET particles are not available for low inclination orbits, hence devices with low SEU LET threshold can be used for orbits with low inclination.

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Internal Electrostatic Discharge Risk Assessment for Electronic Components On-board Spacecraft

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Abstract: **Damage of spacecraft on-board electronic components due to electrostatic discharge from build-up of high electrostatic potential in spacecraft dielectrics and metal conductors has been reported to be one of the key reasons for major spacecraft anomalies and failures. The build-up of electrostatic potential is known to be caused by the penetration of high energy space radiation electrons through the spacecraft structure and their deposition on surfaces or interiors of dielectric materials such as wire insulation, PCBs, etc & surfaces of ungrounded conductors such as component metal lids, floating radiation shields, etc. This paper presents risk assessment for on-board electronic components to internal electrostatic discharge by estimating the electron current density for different representative orbits such as LEO, GEO and GTO. The integral electron flux for these missions is estimated using the FLUMIC model for worst case electron environment and CRRESELE model for conditions prevailing during geomagnetic storms. In house developed ray tracing tool 'IESDMAP' has been used to determine the built in shielding provided by spacecraft structure to incoming electrons and hence estimate the internal charging current density. As electronic package enclosure thickness and location of mounting the packages influence the internal charging current, an analysis has been carried out that shows the dependence of internal charging current on these factors. The internal electrostatic discharge risk assessment presented in this paper can aid system designers to take appropriate measures and ensure in-orbit reliable performance of electronic components.**

Index Terms – Deep dielectric charging, internal charging, FLUMIC, CRRESELE, SPENVIS

I. INTRODUCTION

Space radiation electrons with energy > 0.1 MeV in the Geostationary Orbit (GEO), Medium Earth Orbits (MEOs) and Polar Earth Orbits (PEOs) are a major threat to spacecraft on-board electronic components. It is because such electrons can penetrate the satellite structure and get deposited on surfaces or interiors of dielectrics and surfaces of ungrounded conductor leading to a gradual build-up of electrostatic potential. If the electrostatic potential between two surfaces exceeds the breakdown strength, electrostatic discharge (fast transfer of charge leading to transient currents) takes place [1]. The electrostatic discharge leads to serious damage of electronic components. Trapped protons generally do not have enough penetrating flux to cause a significant charge build-up and hence electrons solely contribute to the threat of Internal Electrostatic Discharge (IESD) Anomalies observed in ANIK E1, ANIK E2, DRAS and CRRES satellites have been attributed to IESD by electrons [7]. Susceptibility of electronic components to IESD depends upon the current density or flux of electrons in the interior of spacecraft. Computer codes that use electron spectra and spacecraft geometry as inputs can be used to determine internal electron current density.

This paper considers different representative orbits such as LEO, GEO and GTO and assesses the risk associated with IESD for on-board electronic components. The unshielded integral electron spectrum is obtained by using electron environment models – FLUMIC and CRRESELE. The internal charging current density is determined by using electron range vs energy data obtained from software ESTAR and taking into consideration the attenuation offered by the spacecraft 'built in' shielding by using the in-house ray tracing tool 'IESDMAP'. The reduction in IESD risk by increasing the thickness of electronic package housing and changing the location of package mounting is presented in this paper.

II. ELECTRON ENVIRONMENT FOR INTERNAL CHARGING

Low energy electrons (<0.1 MeV) cannot penetrate spacecraft structure and hence contribute only to spacecraft surface charging. However internal charging occurs due to penetrating electrons, generally over 0.1 MeV. The electrons trapped in Van-Allen radiation belts possess energies large enough to cause the internal charging. The Van-Allen belt electrons are trapped in two regions. Under normal conditions of the magnetosphere, the two zones of electron distribution are the inner zone ($1.0 < L < 2.8$) and outer zone ($2.8 < L < 12.0$), where L is Dipole Shell Parameter [4]. The outer belt is highly dynamic and electron fluxes higher than 2 MeV can rise by two or three orders of magnitude over a period of hours. Such enhancements can persist for several days. There is a solar cycle effect, which means that peak fluxes are usually an order of magnitude higher during the declining phase of the solar cycle than at solar maximum. Although satellites in geostationary orbit are far from the peak of the outer belt, they are subject to continuous exposure and experience a significant risk of internal charging effects. Earth regimes of concern for on-orbit internal charging hazard for spacecraft with circular orbit are shown in Figure 1.

III. MECHANISM OF INTERNAL CHARGING

Electrons incident on a material lose kinetic energy continuously during the course of their transit through the

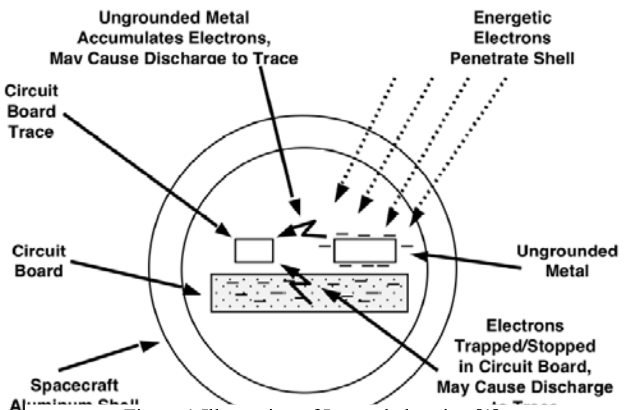


Figure 1 Illustration of Internal charging [1]

material. Eventually the kinetic energy becomes zero and electrons are deposited in the material medium. By virtue of this mechanism, high energy electrons penetrate spacecraft surface and get deposited in internal dielectric materials such as wire insulation, PCBs, etc. or on the surface of ungrounded conductors such as component metal lids and floating radiation shields. The distance traversed by the electron before coming to rest depends upon electron energy and material density. The timescale for charging is often days or longer and is usually determined by the capacitative time-constant across the material [5].

IV. ELECTRON ENVIRONMENT MODELS

1.1 FLUMIC (Flux Model for Internal Charging)

The FLUMIC model is considered as worst case for internal charging caused by trapped electrons. The FLUMIC model gives integral electron spectra for $3 \leq L \leq 8$. The model consists of fits to the upper boundary envelope of daily averaged fluxes during the most intense electron enhancements from 1987 to 1998. Data from GOES-7, the LANL Energetic Spectrometer for Particles (ESP) on a number of geostationary spacecraft and the REM instrument on STRV-1b have been used in this model. FLUMIC describes the electron flux, which has an exponential dependence on energy 'E' and varies with 'L', time of year and phase of the solar cycle.

This model is not valid below 200 keV, hence it is not appropriate for totally unshielded structures. The reason for this lower energy limit to the model is that, below 200 keV, the electron population is dominated by the ring current rather than the radiation belts. The ring current is highly variable on a shorter time scale than is characteristic of internal charging [2].

FLUMIC version 1 and 2 covered L - shells above 2.8, i.e. the outer belt only. Recently, version 3 has been created. This is broadly similar to FLUMIC version 2 in the outer belt because it is based on the same data. However, it also models electron fluxes in the inner belt [5].

Figure 2 Earth Regimes of concern for on-orbit internal charging hazard for spacecraft with circular orbit [1].

1.2 CRRESELE (Combined Radiation and Release Effects Satellite Electron Flux) Model

The dynamic nature of the outer electron radiation belt, together with its diurnal variations mean that statistical description is required while assessing risk from internal charging. No standard models for the variability are yet available, but for engineering purposes the CRRESELE model has been constructed from data measured by the High Energy Electron Fluxmeter (HEEF) flown on the Combined Release and Radiation Effects Satellite (CRRES). CRRES flew in a geosynchronous transfer orbit for 14 months during solar maximum. While the model is based on data collected over a short 14 month period starting in July 1990 and during solar maximum conditions only, they give the most comprehensive picture available of the environment resulting from a geomagnetic storm [3].

The CRRESELE model maps trapped electrons for L values of 2.5 to 6.5. It calculates electron omni-directional fluences (differential and integral) for 10 energy intervals (0.5-6.60 MeV). It gives electron levels for six ranges of magnetic activity, the average for the CRRES mission, and the worst case encountered during the mission. The model also predicts the 27-day recurring, intense outer zone electron "episodes" which provides an improvement over the average values provided by AE-8.

V. INTERNAL CHARGING FLUX AND CURRENT DENSITY ESTIMATION

The electron flux encountered by a spacecraft is a function of orbit parameters such as perigee, apogee, angle of inclination, mission life and timing of the mission. As shown in Table 1, four representative spacecraft missions were selected. For each representative mission, the integral electron flux was obtained by using FLUMIC and CRRESELE electron models integrated in the SPENVIS software. Figure 3 and 4 show the obtained integral flux spectra for representative missions based on FLUMIC and CRRESSELE models respectively.

Table 1: Representative missions for IESD Risk Assessment

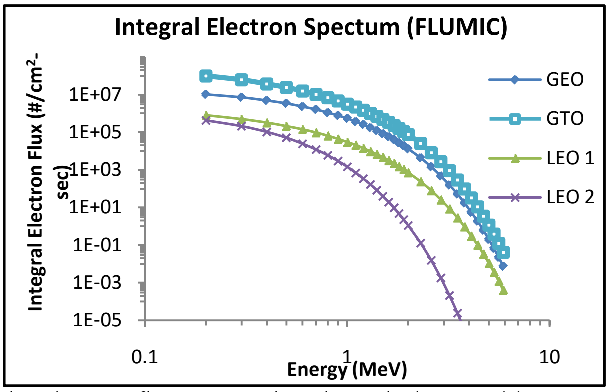
Mission	Perigee	Apogee	Incli-nation	Life (Years)
GEO	35870	35870	0	15
GTO	250	36000	0	15

LEO1	800	800	98	5
LEO2	800	800	20	5

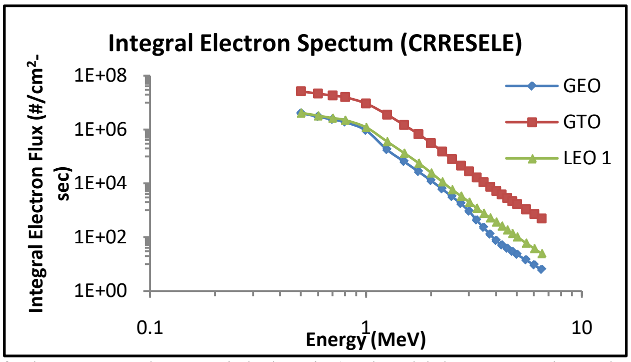
Figure 3. Integral electron spectrum from FLUMIC

Figure 4. Integral electron spectrum from CRRESELE

The spacecraft cuboid, fuel tanks, oxidiser tanks, load cylinder, shear web and electronics packages attenuate



the electron flux penetrating through them and hence act as 'built in' shielding. In order for an electron to reach a collecting surface, its penetration range (depends on energy



of electron and material density) should be more than the 'built in' shielding offered by the spacecraft.

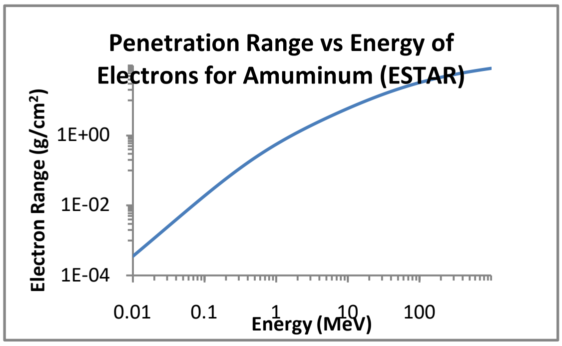
Estimating this shielding is an important process in the estimation of internal charging current density. In-house built ray tracing tool 'IESDMAP' has been used for this estimation. This tool uses a straight ahead approximation i.e. radiation penetrates in straight lines. A detector point is selected at the center of electronics package where electron deposition is to be estimated. An imaginary cubic box is placed around detector point. Each face of the imaginary box is divided into 10,000 sectors. For computing electron deposition from one sector, a ray is launched from the detector point to the centre of sector. The mass thickness of objects intercepted by this ray on its way is added.

The mass thickness obtained from this algorithm gives the estimation of 'built in' shielding that would be encountered by an electron following the path of the ray. The shielding so obtained is the minimum penetrating range that an electron should possess in order to get deposited.

Figure 5. Penetration range of electron in aluminum.

This minimum penetrating range is translated to minimum energy required to be possessed by an electron by using electron range v/s energy data. Figure 5 shows the data obtained from software ESTAR that was used for the present work [6].

Corresponding to the minimum electron energy required to penetrate the 'built in' shielding along the direction of launched ray, integral electron flux are obtained from Figure 3 and 4. If 'Ω' is the solid angle subtended by the sector on the detector point and 'F' is the flux corresponding to minimum electron energy, then flux received through this sector is given by 'f' as



$$f = \frac{\Omega}{4\pi} F$$

The internal charging current density ,ΔJ, contributed by electrons passing through the sector is obtained as follows:

$$\Delta J = 1.6\, X 10^{-19} X\, f$$

The total internal charging current density is the summation of current densities obtained from each sector as:

$$J = \sum_{all\ sectors} \Delta J$$

VI. Electronic Package Thickness and Location Effects

The tool 'IESDMAP' provides a platform where for 'built in' shielding estimation, a spacecraft can be modeled with simple 3D geometrical objects like rectangular planes, circular planes, cylinders and spheres. The modeling of spacecraft 'built in' shielding is a two step process. First, the primary structural configuration of the spacecraft consisting of panels, shear webs, fuel tank, oxidiser tank, central CRPF structure is defined in terms of simple geometrical objects. The second step is modeling the electronic subsystem housing package in which the component resides. This includes defining package enclosure and PCBs inside the package. As the thickness of an electronic package and its mounting location determine the spacecraft 'built in' shielding, modifying the package thickness and location can lead to change in internal charging current density. This presents an opportunity for

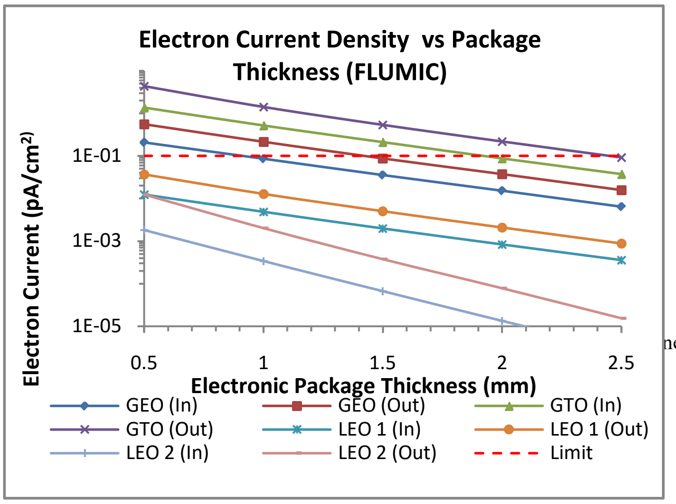
the system engineers to prevent internal charging by controlling these factors.

An assessment has been carried out to determine the extent to which these factors can contribute in lowering the internal charging current density. NASA handbook [8] puts 0.1 pA/cm^2 as the maximum internal charging current density that can be considered safe for device operation. For this assessment, ten different spacecraft mass shield models were defined in 'IESDMAP'. The primary structural configuration consists of typical I-1K spacecraft bus and is kept same for all the spacecraft mass shield models. However the package housing thickness and mounting location have been varied. The package thicknesses considered are 0.5 mm, 1mm, 1.5 mm, 2mm and 2.5 mm equivalent aluminium. Corresponding to each package thickness, the two mounting locations are considered – inside spacecraft and outside spacecraft. Ray tracing code of 'IESDMAP is run through the spacecraft mass models so generated for integral electron flux obtained from FLUMIC and CRRESELE models for the representative missions of Table 1. The electron current densities so obtained are presented in Figure 6 and 7.

Figure 6 shows the dependence of internal charging current density on package thickness for different representative missions and locations as obtained by the integral electron spectrum from FLUMIC model. It is seen that for any package thickness, the internal charging current density is considerably less if the package is mounted inside the spacecraft. Furthermore, by increasing the package thickness, the internal charging current density can be reduced. Internal charging current density estimation base upon FLUMIC model show that spacecraft charging is not a major concern for spacecraft in LEO orbits. For GEO spacecraft, electronic packages mounted outside spacecraft should have a minimum 1.5 mm Al equivalent thickness and for packages mounted inside spacecraft should have a minimum 1.0 mm Al equivalent thickness.

Figure 7 shows the dependence of internal charging current density on package thickness for different representative missions and locations as obtained by the integral electron spectrum from CRRESELE model It can be seen from the figure that for the worst case of GTO mission & outside mounting, by increasing the thickness from 0.5mm to 2.5mm, more than 40 times reduction in the charging current density is achieved. As the CRESSELE model gives integral electron spectrum for conditions prevailing under geomagnetic storms, it can be seen from Figure 7. that during geomagnetic storms, even the LEO orbits are not safe from internal charging. In such situations, as shown in Figure 7, the system engineers can consider the options of increasing the package housing thickness or changing the location of the package so as to ensure that the risk of IESD is reduced.

VII. CONCLUSION



Risk assessment of IESD caused by high energy electrons in the trapped Van-Allen belts is indispensible to assure on-orbit performance of electronic components. This paper estimates the internal charging current density for different representative orbits such as LEO, GEO and GTO. For each representative orbit, integral electron spectrum is obtained from FLUMIC and CRRESELE environment models. The 'built in' spacecraft shielding is estimated using the in-

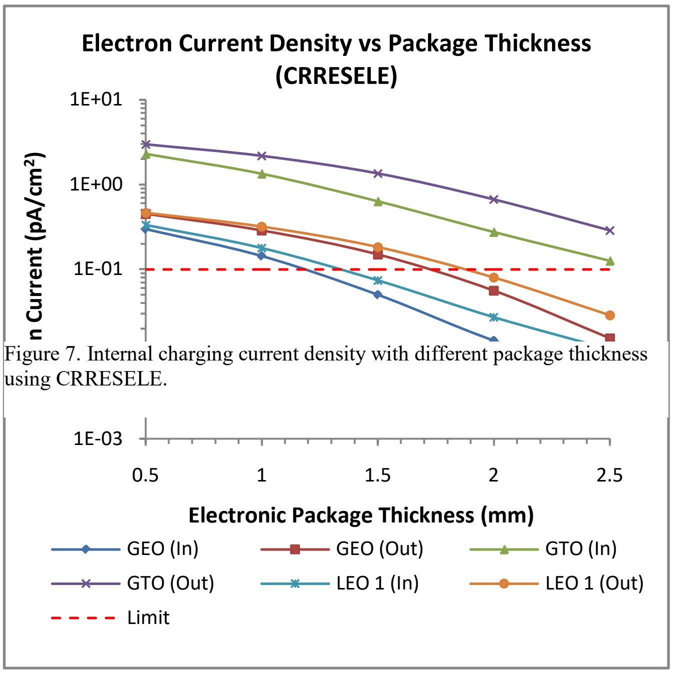


Figure 7. Internal charging current density with different package thickness using CRRESELE.

house developed software tool based on the technique of ray tracing. Risk assessment has been carried out for different spacecraft mass shield models with varying thickness of electronic package housing and its mounting locations. The results show that electronic components in LEO orbits are safe from the threat of IESD. However under geomagnetic storms, IESD can be avoided by mounting the package inside spacecraft and increasing the package housing thickness. The GEO and GTO missions are at higher risk for IESD as compared to LEO but the risk can reduced by mounting the packages inside the spacecraft and increasing the thickness of electronic package housing.

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INDIGENISATION,SUPPLY CHAIN MANAGEMENT,STORAGE AND HANDLING OF EEE COMPONENTS

Components Management for Off-The Shelf Avionics

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Abstract : Space services / spacecraft have become an integral part of the society. Thousands of components are involved in the realization of sub-systems of a major operational spacecraft which is an achievement in terms of procurement, fabrication and supply chain management. The paradigm shift in recent times has been scaling up from the earlier 4-5 spacecraft realization per year with large cycle time realization to the present 12 spacecraft (S/C) per year and towards the futuristic goal of 18 spacecraft per year with reducing cycle times. The success of this goal depends on the availability of Off-the-shelf-Avionics so that they can be fine-tuned to meet the specific mission requirements and assembled quickly to realize the spacecraft. Already, global trends as seen at SSTL, UK have shown the success of the Off-the-shelf-avionics concept for faster realization of spacecraft. It is also leading to the Order to Orbit concept as the Spacecraft is increasingly seen from a Manufacturing point of view.

Presently, fabrication of sub-systems is initiated generally after sanction of Project followed by sub-system reviews / interface meetings. Hence, the cycle time involved is significantly long. To save time and to move towards the goal of off-the shelf avionics, we need to realize pre-fabricated cards. A card level database needs to be prepared and identified with sub-systems programmatically. Many cards are common across Projects. Accordingly, the possible PCBs that can be pre-fabricated need to be identified programmatically and stored in a controlled environment. They can be subsequently used as part of Just in Time (JIT) philosophy on sanction of project in future. Such an approach will lead to fabrication ahead of the Project which will save time and effort. The cycle time is optimized in sub-system / spacecraft realization.

To achieve the same, a Programmatic approach is needed to provide components for PRE-FABRICATION. Based on past experience, the core configuration which can support many projects can be identified and the project specific requirements as enhancements can be done later. For example, we have I-3K S/C power systems for GSAT-8 / GSAT-10 / GSAT-15 / GSAT-16 / GSAT-17 / GSAT-18. As the realization of these S/C are known in advance, a major portion of the Power Systems can in principle be realized in advance in terms of pre-fabricated cards. Similarly common elements like DC-DC converters can be realized and stored to save TIME for all Projects where they are needed in large numbers.

Currently ICSDBS is used for components requirement projection and their issue for fabrication. Hence, Component Management via ICSDBS needs to be augmented to support PRE-FABRICATION. ICSDBS can be augmented suitably to identify the card / subsystem which can be used in multiple projects. This will also help to improve schedules and also ramp up production when needed especially in case of replacement satellites which are needed to sustain continued space services. Fabrication needs to be organized along the lines of a series / programme -- Small Satellites / IRS Satellites / IRNSS satellites / GEO satellites (I-2k/ I-3K) etc., Cards that can be PRE-FABRICATED need to be identified and realized accordingly in each programme and they can be shown in PDR of the Project on its sanction. This will also help R & D as lot of TIME will be made available for focusing on future developments in Spacecraft Technology as seen by the success story of SSTL, UK which has integrated R & D with Off-the-shelf Avionics.

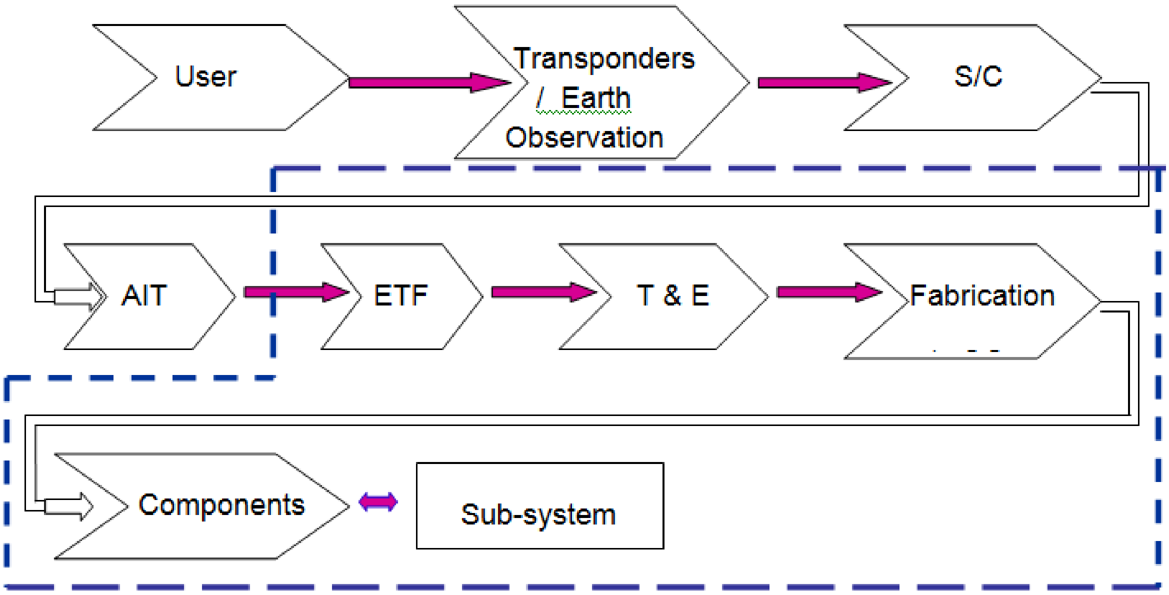
In a space programme driven by services, replacement satellites also form a major portion of the work load and sometimes, there is an unexpected emergency to replace a satellite which is down or in case of an unexpected launch failure. Such a situation normally leads to hiring of a foreign satellite to tide over the crisis. The Off-the-Shelf Avionics will help in such a scenario to quickly assemble the replacement satellite and launch it. This will also help to save valuable foreign exchange as the temporary hiring of a foreign satellite will be of short duration This paper will address an Integrated Component Management approach required to realize Pre-Fabricated Cards towards the goal of Off-the-shelf-Avionics to save cycle time in sub-system / spacecraft realization. A manufacturing perspective is needed for the goal of 12 to 18 S/C per annum

Key words: Avionics, ICSDBS, components, off-the shelf , just in time

I. INTRODUCTION

ISRO Satellite Programme provides space services for Communication, Navigation, Earth observation, Applications of Remote Sensing, Disaster Management, Distance Education, Tele-medicine etc., The supply-chain framework needs to be traced from USER SERVICES to Spacecrafts / sub-systems as shown in Fig 1.0 The present goal of 12 to 18 S/C per annum and the reducing cycle times for realization of sub-systems and spacecraft realization highlights the need for innovative strategies to realize the same. The concept of Off-the-shelf sub-systems especially Avionics has ga ined importance and it calls for innovative component management practices to achieve the same. The historical

achievement of IRS-P2 was a great milestone in the history of IRS / PSLV. The reason for the realization of IRS-P2 in less than a year was because it was largely realized with Off-the-Shelf-Avionics. For example, the AOCE of INSAT-IITS was taken and refurbished as AOCE for IRS-P2 i.e, the changes were essentially w.r.t software. Although it was an exceptional event, it only proves the basic principle that Off-the-Shelf Avionics will help in faster realization of heritage elements (Cards / Sub-Systems) wherever possible to save TIME to achieve THROUGHPUT of 12 to 18 S/C per annum as focus can be given to new elements and software to meet the mission requirements.



Section 2 describes the traditional scenario of an R & D environment with low volume work execution and large cycle times for Projects. Section 3 describes the present component management which is linked to Projects. Section 4 gives the need for a programmatic approach for sub-system realization. Section 5 describes component management in a programmatic manner for Pre-Fabricated Cards / Off-the-Shelf Avionics. It should also be noted that in a space programme driven by services, replacement satellites form a major portion of the work load and sometimes, there is an unexpected emergency to replace a satellite which is down or in case of an unexpected launch failure. The Off-the-Shelf Avionics will help in such a scenario to quickly assemble the replacement satellite and launch it. It will help to overcome the dependency on the foreign satellite which is hired temporarily at great cost to tide over the crisis. This will also help to save valuable foreign exchange as the temporary hiring of a foreign satellite will be of short duration. SSTL, UK ha s successfully integrated R & D with Off-the-shelf Avionics.

II. 2.0 TRADITIONAL SCENARIO : SINGLE PROJECT ENVIRONMENT & A MULTI-PROJECT ENVIRONMENT

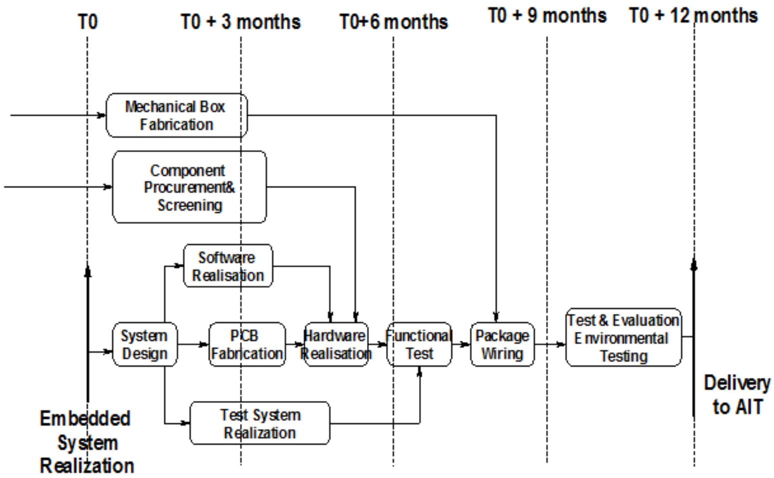


Fig. 1 Realization of a typical sub-system in a typical R & D environment for single spacecraft

The realization of an embedded system in a single project environment and a multi-project environment after the approval of projects is briefly discussed. Typically, the realization of a sub-system in a traditional single project R & D environment is shown in Fig 1. Assuming that there are

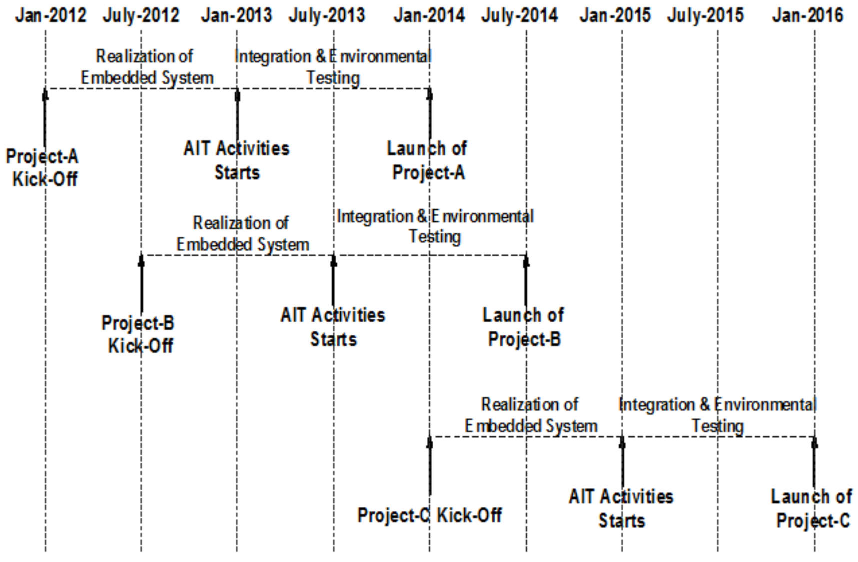


Fig 2 a multi-project environment involving 3 spacecraft and their sub-systems

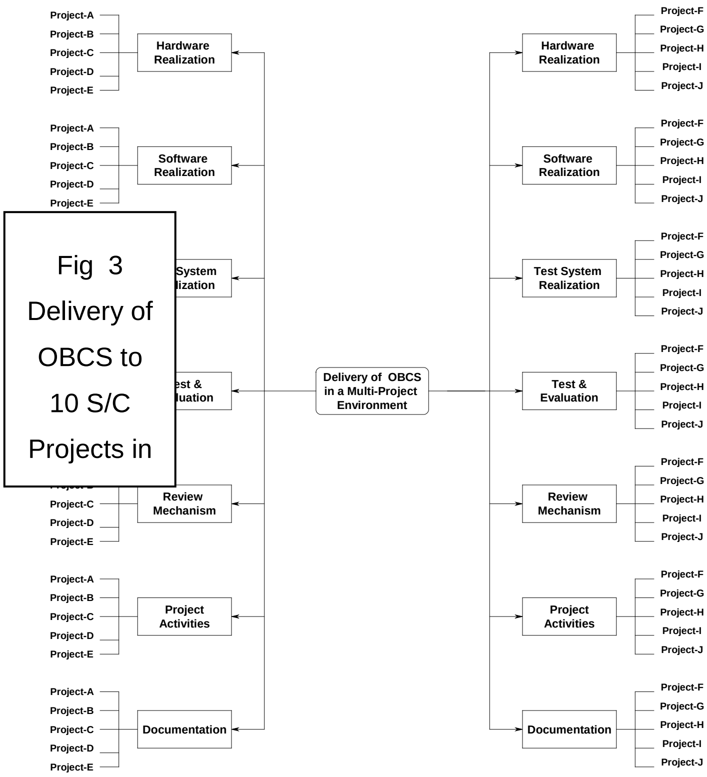


Fig 3 Delivery of OBCS to 10 S/C Projects in

a typically 10 to 20 sub-systems in a spacecraft, the same principle applies to all sub-systems which are realized in parallel.

Let us consider a multi-project environment (only 3 satellites) as shown in Fig 2 by taking 18, 24 and 36 months as time-lines for the realization of the projects depending on the technical complexities involved. The realization of various embedded systems in a multi-project environment calls for optimal utilization of resources – infrastructure and HR. Assuming that more than 30 sub-systems need to be realized for the 3 S/C, any delay in one sub-system can affect the schedule of remaining sub-systems and projects in the pipeline. The typical constraints in a multi-project environment are

- Limited human resources: Human resources are the scarce resources of the organization and should be used efficiently. In multi-project environment, one person is responsible for multiple project activities due to matrix management structure.
- Limited Facility / Downtime of facility: In any organization facility plays the major role for realizing the electronics system. The electronics hardware consists of PCB (printed circuit board), components, mechanical housing, Testing Facility and qualification. Downtime in any dimension slows down the overall throughput.

Fig 3 gives the pictorial representation for delivery of a Sub-system (OBC) for 10 S/C per annum. Each of the steps have to be repeated for all the OBCSs. which will be in different stages of realization --> initial fabrication to mission level operation. A similar situation is present for the remaining sub-systems of the spacecrafts which only highlights the importance of PRE-FABRICATED Cards in delivery of sub-systems to AIT to optimize CYCLE TIME for realization of a Spacecraft. Imagine the situation for 12 to 18 S/C per annum with reducing cycle times of spacecraft realization (3 to 4 weeks only in pipe-line mode for sub-system delivery). The basic steps in High-Volume / High-speed work-execution associated with sub-systems of the 12 to 18 Spacecraft Projects remain essentially the same as in the case of Low-Volume work execution of 1 spacecraft per annum. Hence, if fabrication is started after approval of Project, the delay in one project has cumulative affect down the line on other Projects as resources are shared. The review mechanism is also part of the overall cycle time of the sub-system realization in Matrix Management. As number of Projects increase and are expected to increase further, it also puts more load on the review and delivery mechanism i.e., on the TIME of the staff for review, fabrication and Test & Evaluation, Qualification, AIT-GC, Launch and post-Launch activities. Any anomaly at any stage takes away further time down the line. Hence, the urgency and need for Pre-

Fabricated Cards to save TIME in the early stages of a Project and give buffer TIME down the line.

III. PRESENT COMPONENT MANAGEMENT FOR FABRICATION : PROJECT BASED

The present component management for fabrication has evolved in the R & D era of limited Projects (3 to 4 S/C per annum) with long cycle times (6 to 8 years) for their realization. After finalization and sanction of each project, the component requirements are collected from different subsystems and consolidated. The available stock is checked and the balance components to be procured are identified. Then the procurement action is initiated and components are procured which take the standard lead time. This, in case of custom built space qualified component procurement may take upto one year after placement of order. The received components are inward inspected and posted to stock after the defined tests and verifications including test reports and documentation. An in-house software ICSDBS is used to approve the cards at the design stage and to subsequently issue the components for fabrication according to different project requirements.

To meet the requirements of enhanced Throughput, lot of effort has been put to increase standardization in sub-system designs and also in advance procurement of components for 10 S/C at a time. For example, ASIC AOCE was designed to meet the core requirements of both IRS / INSAT missions and the minor upgradations / technological developments in hardware were taken care suitably (a new card would be realized specific to the mission). The basic package assembly configuration was maintained. As and when the new Project was approved, the realization of the ASIC AOCE was initiated. The fabrication details were given and components were issued for fabrication, development of software and its delivery as PROM, Test and Evaluation (card level / package level) and delivery to the Project took place. The software was programmed as per the mission requirements. Similarly, even in case of BMU-OBC, many cards were standard across different projects. The same principle applies to other sub-systems like Power / RF / SSR / Data Handling etc., The realization of packages is initiated after the sanction of the Project. It is important to note that the realization of the Sub-systems has an impact even on realization of Test Setups / Test Systems etc., and their lock in period increases if the fabrication starts after the initiation of the Project which has an overall impact on Sub-System Life-Cycle. Package assembly can be quickly done if PRE-FABRICATED cards are available. In the next section, the need for a paradigm shift to a programmatic approach for sub-system realization based on Pre-Fabricated Cards is highlighted as we need to realize 12 to 18 S/C per annum.

IV. PROGRAMMATIC APPROACH FOR SUB-SYSTEM REALIZATION

The ISRO Satellite programme has evolved over the years and is organized along the lines of

- Communication (I-3K / I-4K etc.,)
- Remote Sensing (Cartosat series / Resourcesat series / Oceansat series)
- Small Satellites (IMS-1 / IMS-2)
- Scientific Satellites (Inter-planetary / Deep space missions etc.,)

Essentially, the time-line from AIT-GC at Spacecraft level to Launch is practically optimized and the need is to optimize the sub-system realization in the PRE-AIT phase. Over the years the spacecraft configurations have stabilized and the sub-systems have also reached a stage of considerable maturity in each track. Fig 4 shows the typical sub-systems being used in different spacecraft. The incremental changes that take place in sub-systems from mission to mission are added to the core base-line of the sub-system configuration.

Fig 4 Typical sub-systems being used in different spacecraft.

Hence, it is possible to prepare the Card-Level Data base and identify them programmatically. It is feasible to realize PRE-FABRICATED cards which are common to many Projects in a Programme in advance, store them in a controlled environment and deliver them as and when the Project is sanctioned in future. This can be achieve by integrating component management and fabrication / T & E in a programmatic manner ahead of a Project. Pre-Fabricated Cards (Off-the-Shelf Avionics) will help to save TIME and they can be given to the Project after its approval. Project can give more focus to mission planning & management, spacecraft configuration, realization of new elements, package qualification, and software development as major portion of hardware elements (especially cards of the core configuration) are realized in advance. Buffer time will be available for both Sub-System / Spacecraft testing which is vital for the goal of 12 to 18 S/C per annum. It will also help us to move faster towards global trends of Order to Orbit to meet customer expectations on demand especially for replacement satellites. Pre-Fabricated Cards are used extensively in the PC industry and it was pioneered by DELL Computer Systems and adopted by others subsequently.

V. SUGGESTED COMPONENT MANAGEMENT FOR PRE-FABRICATION : PROGRAMME BASED

We have now entered the RFD era and contemporary manufacturing practices need to be adopted for the goal of 12 to 18 S/C per annum with reducing cycle times for spacecraft realization. It is suggested to issue components in a Programmatic manner so that standard cards in a package / DC-DC converters are realized in advance and stored in a controlled environment and hence available to Projects on their sanction.

Case study 1 : Power Packages of I-3K GEO S/C :. The components for 5 models can be issued to realize the standard cards of the I-3K GEO S/C Power System configuration and these PRE-Fabricated cards will form the bulk of the hardware being realized. On sanction of the corresponding project, the new elements can be realized and integrated with the Pre-Fabricated cards. It will very quickly take us to package level realization / testing and delivery to spacecraft.

Case Study 2 : DC-DC Converters : The DC-DC converter requirements of IRS and GEOSAT programmes are fairly well known. Hence, DC-DC converters in each series (I-3K / IMS-1 / IMS-2 / Resourcesat / Oceansat / Cartosat-2 etc.,) can be realized in advance to save Project TIME in each Programme. Spare DC-DC converters also can be realized as they are needed in large quantities.

Case study 3 : AOCE / OBC packages : The AOCE / OBC packages are used extensively in GEOSAT / IRS Projects and the requirements are well known in advance. Many of the cards are standard cards and are common across Projects and can be realized in a programmatic manner.

Case Study 3 : SMT based packages : A typical card has both SMT and through hole components. All on-board cards have to be realized in 2 phases - SMT assembly line and regular labs for through hole components. As a major portion of the components are SMT components, a dedicated SMT component stores (capacitors / resistors / dioded / transistors) can be considered as they form a major share of the components and these components can be released in a programmatic manner ahead of Projects. The SMT cards can then be routed via conventional labs also to complete the fabrication and stored in a controlled environment. In this method more cards can be realized as the set up (stencil) can be maintained for many cards (e.g. 10 cards). For every new card, the set up (stencil / thermal profile / pick and place machine data etc.,) has to be changed in the SMT Assembly Line and it has bearing on Throughput. R & QA also improves as the process is same for the cards which are realized in bulk mode. Automatically, schedule is improved and cost comes down as set up time is optimized. Man power is also optimized and consumables (e.g. solder paste) are also minimized.

The following illustrates a standard card across different Projects to highlight the feasibility of Pre-Fabricated Cards in a programmatic manner and the need for a card level database.
RISSR10103 (6#) in SSR-10 and RISSR10103 (6#) in SSR-20 of Cartosat-2D.
RISSR10103 (6#) in SSR-10 and RISSR10103 (6#) in SSR-20 of Cartosat-2E.
RISSR10103 (3#) in SSR-10 of EMISAT.
The TS components can be mounted after Project requirements are finalized on approval i.e, even partial fabrication can be done for some packages / cards if more than 80% components are known. NA list also gets minimized and saves time. This approach towards Pre-Fabricated Cards saves Time considerably. As Procurement is anyway being done for 10 projects in advance in a Programmatic manner, along similar lines PRE-Fabrication can also be done in programmatic lines for 3 to 5 models so that Just in Time philosophy can be suitably adopted.

VI. CONCLUSION

Large amount of Space Quality/ Hi-Rel components (Electronic / Electrical / Electro-mechanical) are used in cards & packages on-board in a spacecraft. Timely availability of components ensures deliverables and project schedules. Apart from the advance planning for procurement of components, standardization of components in terms of models, packages and availability in PPL, improvements in the standardisation of sub-system designs, much more needs to be done to achieve PRE-FABRICATED Cards / Off-the-Shelf Avionics. The key lies in issue of components in a Programmatic manner ahead of the Project sanction. A paradigm shift in component management for fabrication from Project to Programme can help to realize Pre-fabricated cards and they can be given to the project on its approval.

A Card level database needs to be prepared so that common PCBs across projects are identified and pre-fabricated, tested and stored in controlled environment for Just-in-time usage as and when the project is sanctioned. This approach leads to project independent fabrication, saves time and effort. The cycle time is optimized in subsystem realization. Appropriate budgetary, procedural and production support must be provided in the Programme to support components procurement for Pre-fabrication with component bank concepts. This will also help to improve schedules and also ramp up production when needed especially in case of replacement satellites which are needed to sustain continued space services.

Along with realization of Pre-Fabricated Cards in a Programmatic Mode, heritage components need to be replaced quickly. Towards this, optimization and synchronization of the procurement aspects also need to be addressed. A dedicated component procurement team at Purchase to process the estimated 500 to 600 purchase files

per annum for Components on an end-to-end basis will save time significantly as procurement Time is also intimately linked to shrinking Project cycle times which is the driving force for Pre-Fabricated Cards / Off-the-shelf Avionics. This is as important as saving time in component flow for fabrication i.e., Integrated Component Management (ICM) is needed for the goal of 12 to 18 S/C per annum with reducing cycle times. As ICM will save TIME, it has the potential to help in realizing Spacecraft / Sub-systems for global markets as part of Make in India initiative in continuation of earlier efforts of HYLAS / W2M / / Youthsat / SARAL (I-2K / I-3K / IMS-1 / IMS-2) with reduced cycle times.

Thus, issue of components for fabrication needs to be organized along programmatic lines -- Small Satellites (IMS-1 & IMS-2) / IRS Satellites / IRNSS satellites / GEO satellites (I-1K, I-2K, I-3K) etc., so that pre-fabricated cards can be shown in PDR of the Project. Even review time is a major portion of Project cycle time and it will get optimized with PRE-Fabricated cards. This will also help R & D as lot of TIME will be made available for focusing on developments in future Spacecraft Technologies as seen by the success story of SSTL, UK [1.2.3].

Acknowledgements

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Robustness in design, fabrication, testing of indigenous connectors and induction in to launch vehicle application

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Abstract – Connector per se is a very critical component for electronic packages used in launch vehicles. Its performance and reliability matter significantly for the success of launch mission. Indigenisation effort in indentifying connectors as a key EEE part plays a vital role in achieving self reliance, mitigating obsolescence and counterfeit issues. In this discussion various indigenous connectors used in the successful PSLVs and other launch vehicles of ISRO has been presented. Focussed attention is given to the generation of PID, facility evaluation, design, selection of materials, methods of fabrication process, engineering model evaluation, screening and qualification test, field evaluation, modification, if required after field trials and finally induction into LV System. The methodologies followed in the realisation, testing and induction of high reliable connectors used in launch vehicles has been presented. It was seen that the steps followed in the realisation and induction of indigenous connectors proved to be highly successful with the consecutive successful launches of PSLVs and other launch vehicles.

Keywords –EEE parts, PID, indigenisation, de-rating, out-gassing, R&QA, SCISC, mil stds, LV

I. INTRODUCTION

An electrical connector is an electro mechanical EEE component used to join electrical termination and create an electrical circuit. Electrical Connectors consists of plugs (male-ended) and sockets (female ended). The connection may be temporary, as for portable equipment, require a tool for assembly and removal or serve as a permanent electrical joint between two wires or devices.

There are hundreds of types of electrical connectors. In computing, electrical connectors can also be known as a physical interface (ie., physical layer in OSI model of networking)

In military and aerospace requirement, the connector used must be high reliable version and conforming to the military Standards defined by NASA and ESA Quality guidelines and requirements. VSSC (R&QA) reliability and quality Assurance requirements govern the guidelines for selection and use of EEE components for launch vehicle application. E EE-INST-002: instructions for EEE parts selection, screening, qualification and de-rating VSSC PPL are the applicable document for VSSC (R&QA) requirements. Mil Stds namely 24308, D38999, 1344, 202 and 39029 for contacts are the guidelines taken for the material selection, process guidelines, fabrication, screening and qualification programme for connectors. Positronics, Glenair, Tyco, Souriau and Amphenol are the major manufacturers and suppliers of imported connectors. Indigenisation of EEE components have been a vital part in space program under the overall indigenization effort initiated by VSSC/ISRO in early 1980s. Major activity initiated by VSSC was the programme of indigenization pertaining to connectors and started inducting from 1996 onwards. This became necessary to mitigate the issues with regard to obsolescence, availability and subsequently counterfeit related issues. Today more than 95% of connectors are indigenized and used in launch vehicle. The range of connectors comprises all variants of D-sub connectors, D38999 circular connectors, Push-pull connectors and umbilical connectors. A close look at the complexity of electronic packages sitting in PSLV class of vehicle reveals that there are about 250 packages with 70,000 components, 63 Km of harnessing, 28000 crimp joints, a lakh of solder joints and 1500 connectors. The reliability of the connectors going into the system attribute to the methodology followed in the design, fabrication, testing and induction in to the LV system.

The reliability of EEE parts depends mainly on the selection of materials, design going into the system, process control, testing (screening & qualification) and finally modification carried out based on the feedback from the field trials. As per EEE-INST-002 NASA guidelines, following are the materials identified for connectors for aerospace application.

II. MATERIAL

Materials are a primary consideration in selecting connectors for space flight application and the following requirements and guidelines are provided.

1. Base materials for metal shell connectors shall demonstrate low permeability (ie., resist

establishment of magnetism in the material), machined aluminum alloy, corrosion resist steel or brass are the preferred material

2. Preferred finishes for Metal Shell Connectors and Contacts: Electro less nickel plating is the preferred finish for circular, general purpose D-subminiature and micro miniature metal shell connectors. Gold over copper flash is required finish for D-subminiature connectors when residual magnetism is a consideration. Passivated stainless steel or gold is the required finish for coaxial connector. Gold plating in accordance with ASTM-B488, Type II, Grade C, class 1.25 micron is the preferred finish for the contacts over the entire contact including the engagement area.

3. Prohibited finishes for metal shell connectors, contacts, Terminals and Terminal lugs.
   Cadmium, Zinc, chemically coated cadmium or Zinc, or silver shall not to be used as a connector or contact finish. Silver shall also not to be used as an under plate and shall not be used as finish due to corrosion concern when exposed to atomic oxygen in lower earth orbits. Due to the risk of the whisker growth, which can lead to short circuit conditions pure tin finishes are prohibited.

4 Preferred Dielectric Materials

The following are preferred dielectric insulating materials for multi-contact connector (colour is optional)
Molding compound
Diallyl phthalate (DAP), type SDG-F or type GDI-30F of ASTM-D5948
Themoplastics
Polyester, glass reinforced, MIL-M-24519 type GPT-30F or type TPES013G-30A0000per ASTM-D5927
Polyphenylene sulphide (PPS), glass reinforced Mil-M-24519 type GST-40F or type PPS 000G 40A0000 per AST-D4067.
Liquid crystalline Polyster, glass reinforced MIL-M-24519 type GLCP-30F
Diallyl phthalate (DAP) is the preferred material for solder application; PTFE (Teflon) is the preferred material for radio frequency and Data Bus Connectors. In general, the non-metallic material used in connectors shall be non combustible or self extinguishing.

III. OUTGASSING

Outgassing occurs in vacuum environment when unreacted additives, contaminants, absorbed gasses or moisture can evaporate from molding materials and ink. These outgassed materials can condense on cold surfaces causing performance degradation. Outgassed materials can also become more rigid or brittle. Non-metallic materials shall not exceed 1% total Mass Loss (TLM) or 0.1% Collected Volatile Condensable Material (CVCM) when tested in accordance with ASTM-E595 (Test Method Outgassing). Acceptable material should be selected from NASA Reference Publication 1124.

Materials and process Technical Information service, PML, VSSC are the documents available for reference. However, materials listed as acceptable in the documents may have been baked out prior to evaluation in order to reduce outgassing and the users need to be aware that they have performed similar processing in order to achieve acceptable levels of outgassing. Testing shall be performed as per ASTM-E595 for materials that are not traceable to the above reference. Processing generally consists of bake out at 125°c and 10^{-6} Torr for 24 hrs.

IV. CRYOGENIC APPLICATION

The only connectors that are officially rated for use in low temperature cryogenic application are procured to MSFC spec. 40M38294 (connector, cryogenic circular,

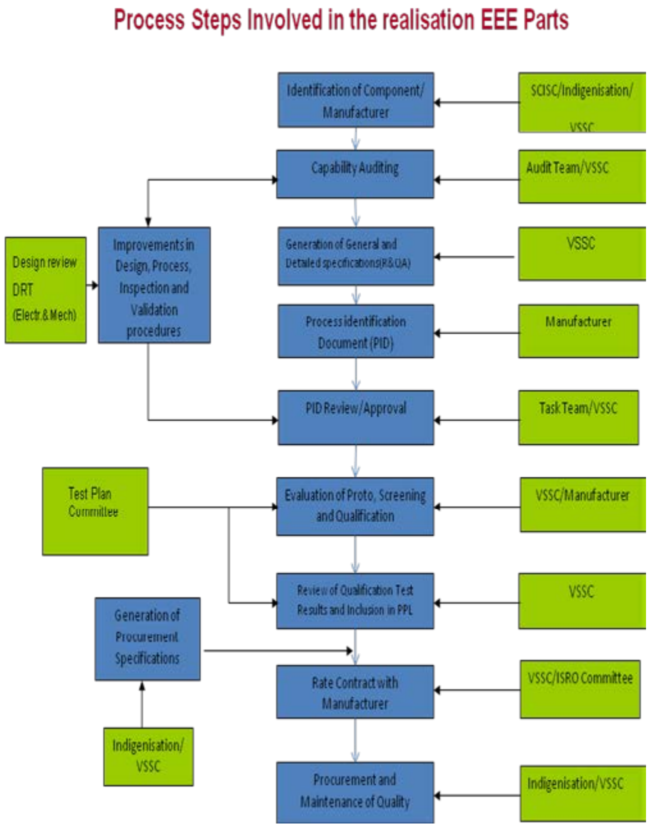


Figure -1

-269°C). However, experience has proven it is possible for other connector types to be used successfully at cryogenic temperature. It is recommended that connector samples should be subjected to five cycle of cryogenic temperature cycling using sufficient low temperature to qualify for the intended application. Perform post temperature cycle inspection at room ambient condition for cracks and DWV.

The following chart depicts the process involved in the realization and induction of components into the LV system. Process steps involved in the realisation of indigenous EEE parts are given in Fig.1.

V. CASE STUDIES

Case I - D-sub Connector

High reliability connectors utilize female closed entry contacts that provide an unl

Figure -2

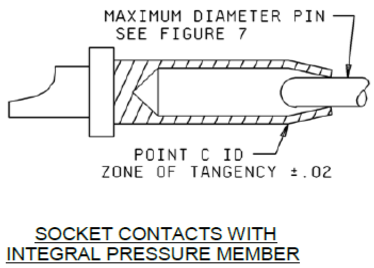


Figure 2

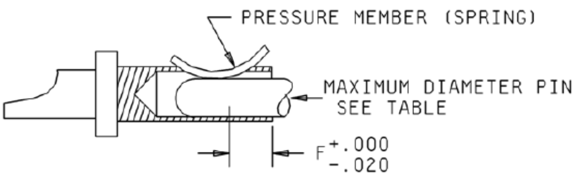
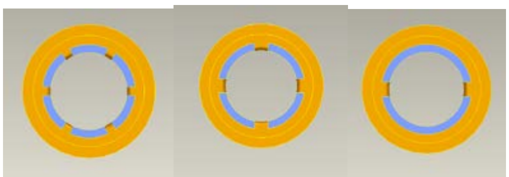


Figure 3



TWO TINES FOUR TINES SIX TINES

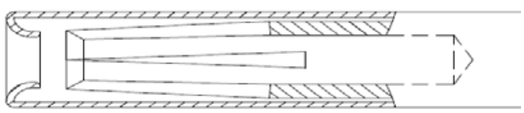


Figure 6 Sectional view

material at the face of the contact. The closed entry feature is crucial in preventing damage to female contact used in harsh environment, repeated mating cycles, blind mate application and application requiring highest reliability.

A common closed entry design utilized by connector manufacturer is a split tine and sleeve concept. The main part of the contact has split tine to provide normal force on male contact when connectors are mated. A sleeve is placed over the main part of the contact to provide a closed entry. The sleeve surrounding the split tine offer greater contact reliability when compared to a similar contact without closed entry feature the sleeve serves to limit the distance the contact tines can open. If female contact tines open too far, they may not return to their original position. This may cause diminished normal forces and can result in intermittent or open electrical circuits.

Female contact tines can open too far if an over-size pin is inserted in to the contact. The most common cause for damages can occur if a male contact is inserted in a female contact at an angle. Rocking the connectors back and forth during mating and demating can pry the female contacts open. Utilizing a sleeve to provide a closed entry feature does allow split tine contact greater reliability. This design has been used for decades because it provided a degree of reliability at an affordable price. However split tine contacts are still susceptible to being pried open if care is not taken when cable connectors are mated and unmated to other cable or board mount connectors.

The split tine design has other inherent weakness. One weakness is the need to anneal the crimp barrel. The material used to manufacture split tine female contact must have elasticity to allow the tine to open when receiving the male contact and then to return to their original position after the male contact is disengaged. Unfortunately, elasticity is not a characteristic that is desirable for the crimp barrel. When crimping a wire into a contact, the material must be ductile to allow a permanent set after the crimping operation.
Split tine contacts are manufactured using a material with elastic properties. The crimp barrel is annealed to soften the material so a proper crimp can be achieved. If the annealing process is not carefully controlled, the mating portion of the contact may unintentionally be annealed. This will result in diminished normal forces and potential electrical failures.

Other weakness of split tine contacts revolves around the fact that the tines must be depressed to provide normal force. The depressed tines slope inward and form a 'point' at the mating end of the contact. If the forming operation is not carefully executed, proper normal force will not be achieved. Also, since the tine slope toward a point, there is a reduced area of contact between male and female contact interface. The interface consists of a small ring at the tip of the female contact. Electrical contact depends solely on this small area between the male and female interface.

New approach for contact eliminating many of this weakness of the split tine design is the socket contact with clip type design. It utilizes a two piece contact design. Each piece serves separate function. The main body of the contact provides the mechanized platform for the contact system. This include a true closed entry contact opening. The spring clip provide normal force on the male contact shown in Fig 3 & 4. It uses spring clip which is very robust

and less susceptible to damages. The system is much more rugged than traditional female contact design.

Another important feature is the use of brass to manufacture the base contact. B rass has excellent properties for crimping wire on to contacts, eliminating the need for annealing, thus avoiding the potential for intermittent or open electrical circuits due to improper heat treatment. The base contact can be made of brass because the spring clip provides contact normal force. The spring clip is made of spring tempered beryllium copper.

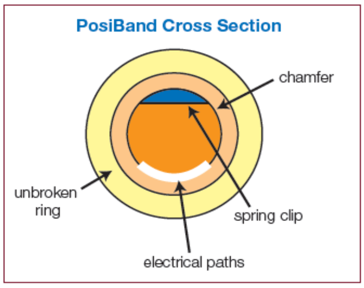


Figure 7

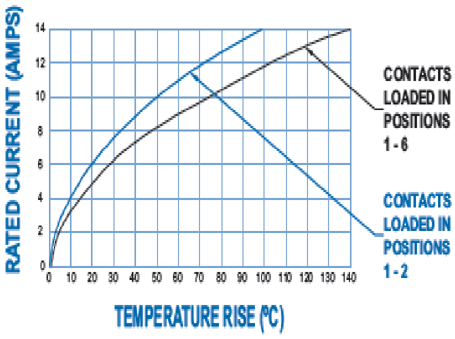


Figure 8
12amp @ 2contacts ; 10amp @ 6 contacts
Contact resistance 0.005 ohm. max.

The clip system increases the interface area between male and female contact when compared to the sloped design of split tine contacts. The greater contact area provides more reliable integrity. On a micro level, there are a greater number of electrical paths through the contact interface. T he greater contact area provides better resistance to discontinuity during vibration. T he greater contact area may also minimize the effects to electrical performance due to corrosion over time.

Greater contact area provided by the chip system does not increase insertion forces. In fact the design provides a more consistent insertion force value, which results in a lower average insertion force when compared to the split tine design. H owever, due to non idealities in the clip design there are deviations observed in the continuity of connectors. *This resulted in adopting hooded split tines with more than 4 tines typically 4 tines or 6 tines for indigenous connectors shown in Fig 5&6. The contact separation force has been revised to min. 50 gm and max.* 150gm.

Case II – Push-pull connector

PTDS series push-pull connectors are used in the inter-stage interface areas where these connectors are to be separated during the separation of stages. The vehicle half after separation will act as a dead face. T he separation force is an important parameter for the smooth separation of the push-pull connector. These connectors are processed as per the process identification document (PID) and tested as per test plan document before inducting into flight application. T he deviations observed during field trials have been corrected with minor design changes, material changes and tightening the tolerance specification.

Figure 9

Figure 10

Following are the changes made to make it a robust design to improve reliability

I. Dimensions have been toleranced to suit reliable operation. The tolerance has been specified to 0.01 mm wherever necessary.
II. Retainer ring spring force measurement has been added as part of acceptance
III. Load spring material has been changed to stainless steel 304 from phosphor bronze.
IV. Coupling nut and coupling bush material have been changed to Al alloy 7075 (T6) from Al alloy 6061(T6) because Al 7075 has got excellent tensile strength. T his

improved wear resistance of coining and travel of retainer ring.

V. Insert retainer strip material has been changed from plastic to metal (BeCu). The bonding of rear insert and front insert has been changed to rear side so that retainer ring will hold the bonding area together even if extra force Is applied on the insert through harness.

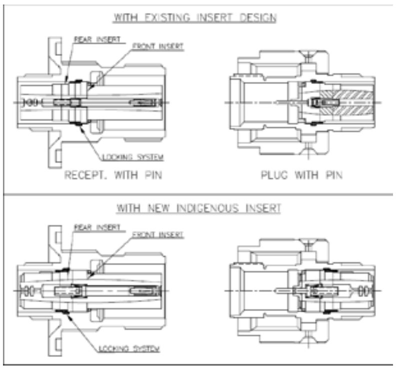


Figure 11

Case III - D38999 connector

The connectors are mainly used in the vehicle harness interface with avionic packages. This was qualified to mil Std D38999 requirements. The connectors are processed as per approved PID and tested to VSSC test plan. Modifications have been effected after field trial to improve reliability.

Main modifications are

1. Pin retention clip has been changed to metal from plastic retention clip.

2. Just as in push-pull insert bonding configuration, the bonding area between front insert and rear insert has been change to location such that retainer ring will hold the bonding area to improve reliability.

Case IV - 317 Umbilical Connector

The design, fabrication and qualification of 317pin electrical umbilical connector was taken up as an indigenization activity for use in GSLV MK3. The connector configuration was made to meet the increased measurement envisaged for GSLV MK3 class of vehicle. The 317pin configuration resulted in the selection of high density 128pin D38999 circular connector inside the main umbilical connector. This configuration was realized and qualified in 2008 through Indian Industry. The first batch of connector was put to use in various tests including hot test of L110 stage and EB proto model testing. Considering the criticality of dimensional tolerance for the umbilical connectors in the usage of high density D38999 connector and reduced measurement requirement of GSLV MK3, it was decided to change over to 282pin umbilical connector configuration avoiding 128pin D38999 connector inside. The issues seen with 317pin version during trials were addressed and additional improvements required were incorporated. However, the basic mechanisms, shell size, overall size of the connector etc. are not altered. The new version is qualified for the derived vibration levels from acoustic tests. A separate qualification model was subjected to all tests including vibration test to qualification level.

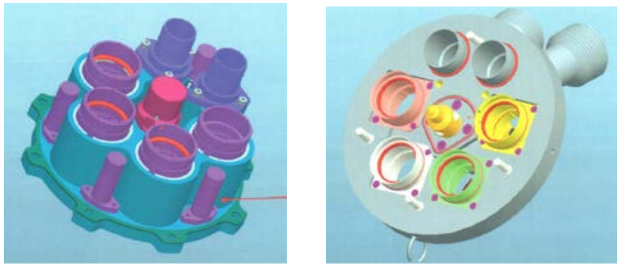


Figure 12

Following improvements/modifications were implemented in 282pin connector.

Misalignment of the ground half and vehicle half shown in Fig 13. The tolerance and clearance of the subassembly parts were redefined based on tolerance analysis and implemented

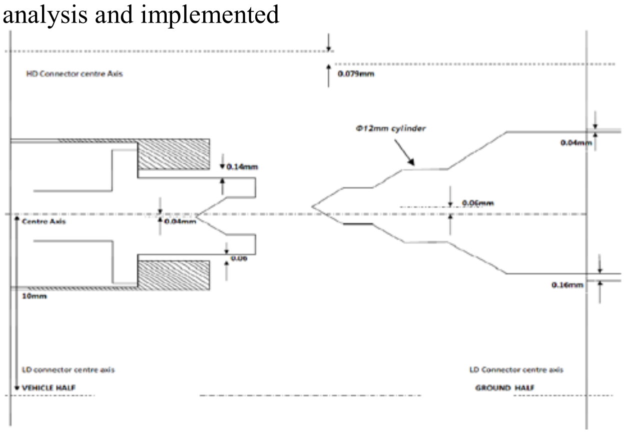


Figure 13

Retention of the ground half - Even though alignment has improved, retention of the ground half with the high density connectors inside during de-mating with tool was observed. The force provided by the main spring was not sufficient to overcome the contact retention caused due to friction and misalignment and the force imbalance of the non symmetrical layout of the connectors and also due to space constraint. This was observed when the ground half was at 3-4 mm from complete disengagement from vehicle half. Three additional spring systems were introduced at 138° angle sector to provide additional ejection force to the ground half for the existing layout of

the connector. This has also aided for the better engagement with uniform gap between umbilical (0.8-1.5mm) and the coupling torque has also reduced. Since each spring will impart a force of 15 kg on the ground half, the shear washer for the emergency release will be loaded with 45 kg and the shearing of the washer will be around 300kg release and is acceptable. Adequate margin exist in the shear washer capability for the increased spring load as the minimum shear capacity of washer is increased to 570 kg minimum.

Deformation in stainless steel balls and disconnection pin in the pin-collar contact edge was solved by changing the hardness of the material to the range 45 to 60 shore hardness.

Secondary release separation force was found to be higher than the specified range of 40-80 kg. The radius of curvature of rocker arm was increased to optimize the separation force.

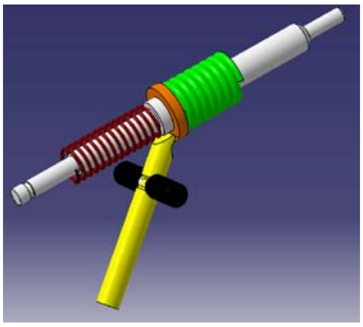


Figure 14

Spring loaded ball plunger-grub screw shown in Fig.14 is used to lock the disconnection pin in its position after engagement. The problem was due to poor quality of spring loaded ball screw. Black anodized coated hardened SS ball screws of LPS Bossard make EH 2205 balls with dia. 4.5 mm were used and found to be satisfactory.

Qualification tests were carried out on the modified connector and found to be satisfactory. Modified connector is now used in GSLV MK3 flight.

VI. CONCLUSION

Focused attention is given to the generation of PID, facility evaluation, design, selection of materials, methods of fabrication process, engg. model evaluation, screening and qualification test, field evaluation, modifications, if required after field trials and finally induction into launch vehicle. System approach for the realization, testing and induction of connectors as an indigenized component into LV is robust and proved by the reliable operation of electronic system in Launch Vehicle meeting all military and VSSC standards.

ACKNOWLEDGMENT

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5) ASTM Standards

Indigenization of Light up transformer for ISRO LASER Gyroscope

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Abstract—The design and development of ISRO LASER Gyroscope (ILG) is in progress and the light up transformer is critical part of the sensor which initiates LASER. The light up transformer is a pulse transformer with custom made design and was imported during initial development phase and latter efforts were put for indigenising the light up transformer in order to be self-reliant in ILG production. The pulse transformer proto models were realized and evaluated for its electrical performance. This paper depicts about the qualification test plan, test results and decap assessment of the pulse transformer of qualified samples. The pulse transformers were cleared for flight and included in Preferred Parts List (PPL) based on the satisfactory qualification test results.

Index terms:Pulse transformer, rise time, transformer topology, LASER, ISRO Laser Gyro.

I. PULSE TRANSFORMER

Pulse transformers are electrical devices used to increase or decrease the voltageprovided by an external pulsed source. In most ways their appearanceand function are closely related to those of conventional transformers. Howeversteep flanks of the pulses are typically associated with high frequencycomponents, making pulse transformers and their design process partiallysimilar to high frequency transformers. The design considerations thereforeinclude concerns regarding saturation behavior and oscillations during thepulse, efficiency at different load points as well as enhancement of rise time.

In literature, numerous electrical equivalent circuits considering LF and HF properties of pulse transformers have been proposed and IEEE standardized the equivalent circuit of pulse transformers [1] as shown in Figure 1. In order to simplify the analysis of the transient behavior for operation with rectangular pulse voltages, the standardized equivalent circuit can be reduced to the equivalent circuit [3]shown in Figure 1.

The rise time and the overshoot of the outputvoltage, are mainly defined by the leakage inductance $L_\sigma$and the capacitance C_d. Assuming an ideal step voltage atthe primary, the output voltage v_{out}(t) can be calculated withthe Laplace-transform as described in [2]

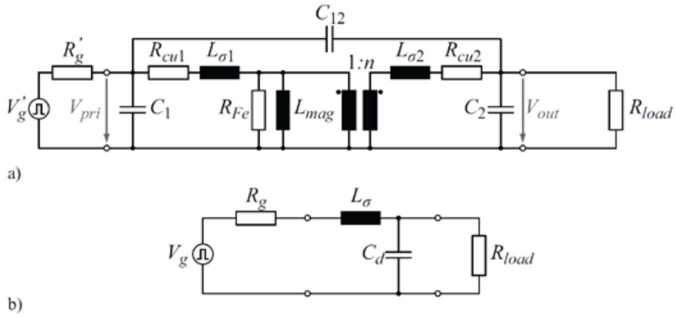


Figure 1.
a) IEEE standardized equivalent circuit of a pulse transformer b)simplified equivalent circuit during the leading edge.

$$v_{out}(t) = \frac{V_g R_{load}}{R_g + R_{load}}\left[1 - e^{-at}\left(\frac{a}{k}\sinh(kt) + \cosh(kt)\right)\right] \quad (1)$$

with $k^2 = a^2 - b$ and

$$2a = \frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}}, \quad b = \frac{1}{L_\sigma C_d}\left(1 + \frac{R_g}{R_{load}}\right)$$

where the damping coefficient σ of (1) is given by

$$\sigma = \frac{a}{\sqrt{b}} = \frac{C_d R_g R_{load} + L_\sigma}{2\sqrt{R_{load} L_\sigma C_d (R_g + R_{load})}}. \quad (2)$$

If it is assumed, that the output pulse shape is mainlydefined by the transformer characteristics, the modulator'impedance $R_g$can be neglected. Thus, the dampingcoefficient σ considering only the influence of thetransformer can be simplified to

$$\sigma = \frac{a}{\sqrt{b}} = \frac{1}{2R_{load}}\sqrt{\frac{L_\sigma}{C_d}} \quad (3)$$

Where$L_\sigma$isleakage inductance and $C_d$is capacitance.

The overshoot and rise time of the output are given by

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \quad (4)$$

$$T = \frac{\sqrt{b}}{2\pi}t, \quad T_r = 2\pi T_{10\%-90\%}\sqrt{L_\sigma C_d} \quad (5)$$

II. LIGHT UP TRANSFORMER

Light up transformer provides high voltage pulse in the order of 12 to 15KV to the He-Ne medium by capacitive couplingfor initiating discharge. A 0.15µf capacitor stores the energy (8mJ) from 230Vac through half wave rectifier (peak detector) and discharges it across light up transformer primary winding, which leads to bidirectional pulse (damped sinusoidal oscillation) across light up transformer primary. The schematic of the Light up transformer and waveform across Light up transformer primary are given in Figure 1&2 respectively.

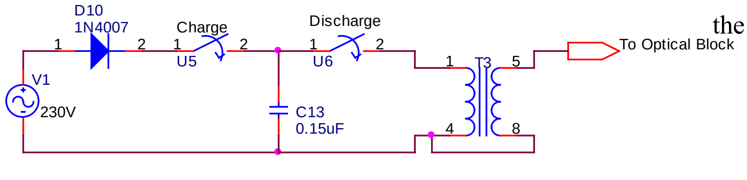


Figure 2: Schematic of Light up transformer

The light up transformer is a high frequency, high voltage pulse transformer with primary and secondary windings connected in auto transformer configuration with step up turns ratio of 1:50. The effective frequency range of operation is from 100Khz to 1MHz.The specification of the light up transformer is given in table 1.

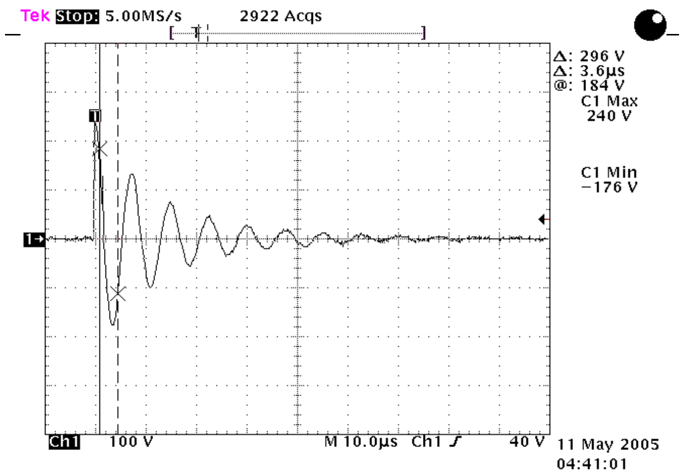


Figure 2: Waveform across Light Up Transformer Primary:

TABLE 1. SPECIFICATION OF THE LIGHT UP TRANSFORMER

SL. NO.:	PARAMETER		SPECIFICATION
1	DC Link Voltage	*Vin*	400 V
2	Output Voltage	*Vout*	20 KV
3	Pulse Duration	*Tp*	1 to 10 µs
4	Output Energy	*Eout*	≈ 10mJ max.
5	Rise Time	*Tr*	< 500ns
6	Overshoot	*Vmax*	<70%
7	Turns ratio		1:50
8	Temperature		-55 to 125°C

The primary and secondary windings of Light Up Transformer are wound on a hollow ferrite bar core. This hollow ferrite bar core is constructed by stacking toroidal ferrite cores (P material) one above another, which provides lesser core losses and higher magnetizing field strength.The light up transformer primary and secondary windings details are given in table 2.

The light up transformer in Ring Laser Gyro is given in the figure 3.

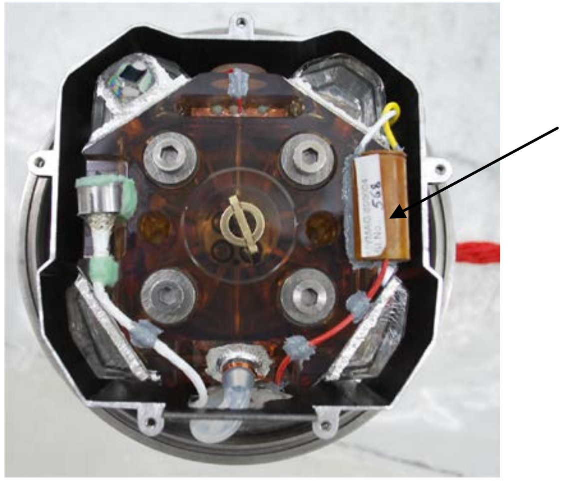


Figure 3: Light up transformer in Ring Laser Gyro indicated with arrow

MAGNETICS make ferrite - P material is used for transformer core and its properties are given below,

- Usable frequency up to 1.2MHz.
- Curie Temperature > 230°C.
- Saturation flux density is 5000 Gauss @15Oes & 25°C.
- Initial permeability, $\mu_i = 2500$.
- Retentivity = 1100 Gauss.

TABLE 2. LIGHT UP TRANSFORMER PRIMARY AND SECONDARY WINDINGS DETAILS

PARAMETER	PRIMARY	SECONDARY
Wire Diameter	0.375mm	0.081mm
Wire Gauge	28 SWG	44 SWG
Wire Type	Insulated Copper	Insulated Copper
No. of turns	20	1000
No. of layers	1	11

Turns per layer	20	93*11+70
Insulating Material	Teflon+Keptone tape	Teflon tape
Insulation between layers	---	1 Layer teflon
Resistance	**425 mΩ**	**125 Ω**
Inductance	**13mH**	**7µH**
Insulation between windings	2 layers teflon + 4 Layers Keptone	2 layers teflon + 4 Layers Keptone

III. QUALIFICATION TEST PLAN

Five samples of the light up transformer were subjected to the following qualification tests,

1. The following parameters were measured,

   - Primary winding resistance and inductance
   - Secondary winding resistance and inductance

2. Two samples were subjected for 1000 switch on cycles (100 per day) after that the samples were de-capped and inspected for any material degradation.

4. The light up transformers were subjected to ILG Sensor level vibration and thermal tests.

The test setup with light up circuit and ILG sensor block for simulating the 1000 switch on cycle is given in figure 4.

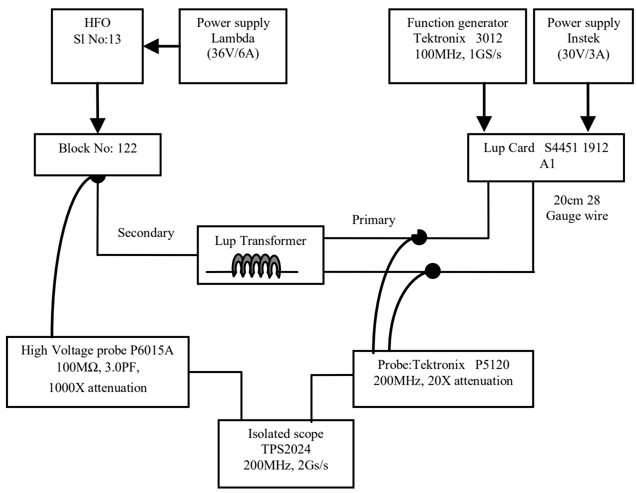


Figure 4: Test Set up

The voltage across the charging capacitor was set to ~420 V pp and 80µsec pulse width in the light up circuit in order to get the transformer output voltage of ~20KVand 500 ns. The light up transformer output was fed to the ILG sensor block and the sensor performance was monitored.

IV. QUALIFICATION TEST RESULTS

1. Resistance & inductance measurement of light up transformer

The resistance & inductance of the primary and secondary windings of light up transformers were measured for five samples using Agilent 34401A,6 ½ digitmultimeter and LCR meter and the measured values are given in table 3.

Probe Resistance	:	0.121Ω
Red terminal	:	Secondary - 8.5cm
Yellow terminal	:	Primary - 18cm
White terminal	:	Common - 18cm
Instruments used	: digit	Agilent 34401A,6 ½ multimeter &LCRmeter
LCR meter settings	:	200 KHz,0.25Vrms

Table 3: The resistance & inductance of the primary and secondary windings of light up transformers

Sl.No.	Between the terminals	Resistance	Inductance
358	Red-White	125.121Ω	13.372mH
	Yellow-White	432.5 mΩ	0.0071mH
357	Red-White	122.821Ω	13.276mH
	Yellow-White	434.8 mΩ	0.0064mH
373	Red-White	124.118Ω	12.891mH
	Yellow-White	436.21mΩ	0.0065mH
376	Red-White	124.557Ω	13.633mH
	Yellow-White	432.6mΩ	0.007mH
382	Red-White	127.941Ω	13.132mH
	Yellow-White	431.5mΩ	0.0075mH

2. Results of 1000 switch on cycles (100 per day)

Twolight up transformers Sl no:578 and Sl no: 579 were subjected to 1000 s witch on c ycles (100 per day)and the light up function was verified. Before and after the above tests the inductance and resistance of transformers were recorded. The test results were analyzed and noted that light up function was satisfactory during the test and the passive measurements ofthe transformers were also normal. The results are summarized in table 4 and 5.

Table 4:Results of 1000 switch on cycles (100 per day)

*Lup Card A1, capacitor 0.22uF,Resistor value 24.3K,Pulse width 80usec,Amplitude 5V, Voltage across capacitor 318-320V					
Date	Input Voltage	Output voltage	Pulse issued	Sl No 578 (Lup ok)	Sl No 579 (Lup ok)
25.06.14	419Vpp	20KV	100	80	75
26.06.14	426Vpp	19KV	100	90	92
27.06.14	420Vpp	18.2KV	100	82	89
28.06.14	422Vpp	22KV	100	75	80
30.06.14	422Vpp	23KV	100	75	91
01.07.14	444Vpp	22KV	100	72	75
02.07.14	422Vpp	20KV	100	78	73
03.07.14	420Vpp	21KV	100	83	74
04.07.14	430Vpp	21KV	100	72	73
05.07.14	415Vpp	18KV	100	63	64

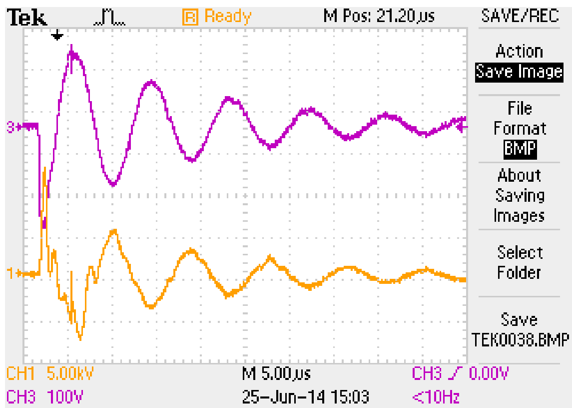
* LUP : Light up

Table 5: The resistance & inductance of the primary and secondary windings of light up transformers before and after 1000 switch on cycles.

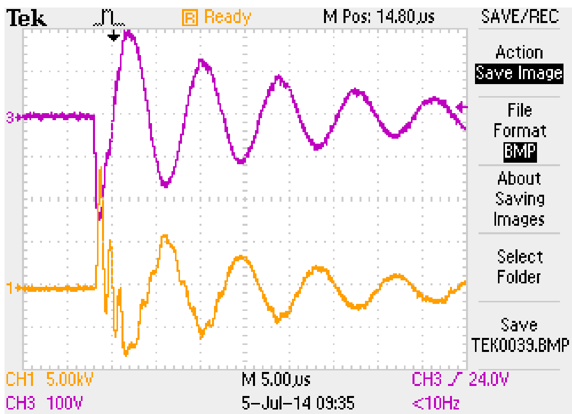
	Primary		Secondary	
Spec. & unit	Resistance 0.3-0.4Ω	Inductance 6-12uH	Resistance 240-290 Ω	Inductance 12-15mH
578Before & after	0.328 Ω	8.78uH	265 Ω	13.83mH
	0.333 Ω	8.79uH	257 Ω	13.62mH
579Before & after	0.316 Ω	8.01uH	273 Ω	14.282mH
	0.322 Ω	7.95uH	268 Ω	14.5mH

The first and last pulse waveforms for Sl. No:578& 579are shown in figure 5.

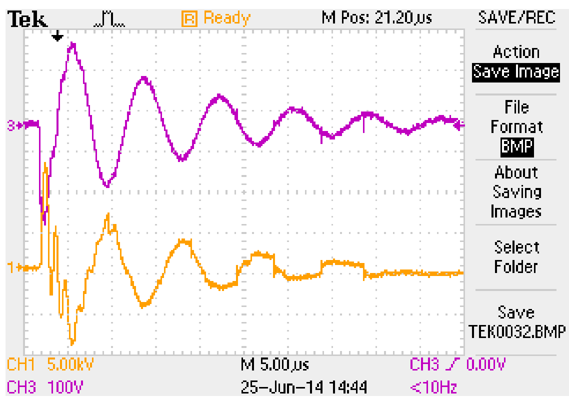
First pulse for Sl. No:578



Last pulse for Sl. No:578



First pulse for Sl. No:579



First pulse for Sl. No:579

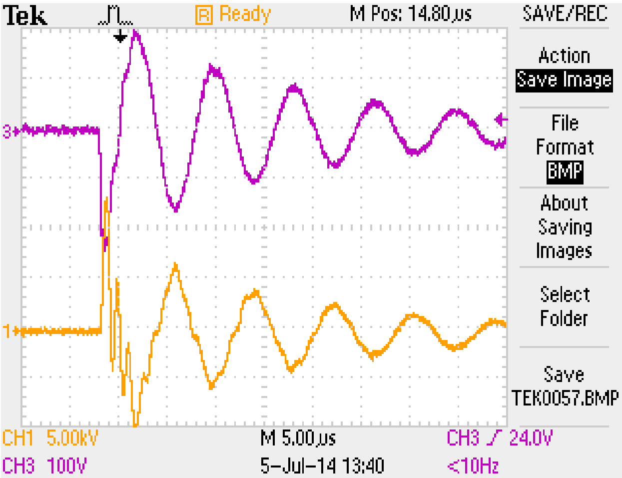


Figure 5 : Pulse waveform

The waveforms of Initial and final pulses for the light up transformer are identical and the performance is repeatable for different light up transformers connected to same ILG sensor block.

1. The Light up transformer passive measurements after 1000 Light up pulses are comparable withthe measurement before start of the test.
2. No performance degradation was seen after 1000 switch on cycles of operation.

De-capping and visual inspection

The light up transformersSl.Nos: 578&579werede-cappedfor assessing any degradation of materials used. The Epoxy moulding of transformer was carefully removed and inspected with respect to winding configuration, wire termination&insulation. It was found that the wire soldering and winding insulation were normal.

CONCLUSION

The light up transformer with custom made design for ILG was indigenously designed and developed. The pulse transformer proto models were realized and subjected to qualification tests. The electrical performance and de-cap assessment of the qualification samples were studied. The pulse transformers were cleared for flight and included in Preferred Parts List (PPL) based on the satisfactory qualification test results.

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Inventory management & Storage of EEE parts for Space Payloads

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***Abstract*—Quality & Reliability of a space system is dependent on its constituent parts. The parts are the basic building blocks of the sub-system/system. Therefore, implementation of effective Parts Management program (PMP) is essential for the success of a space mission.The comprehensive Parts Management Program (PMP) for Space system encompasses the various processes and elements, involved throughout the life cycle of the parts. It includes selection, acquisition, transaction, stocking, requisitioning, handling, managing, issuing, and using the parts for intended Space systems.An effective parts inventory management with proper storage and handling, ensures availability of the parts "right on time" for realisation of the space systems. This is achieved through; Computerised Real-time Inventory system with full traceability, stock alerts, procurement call, long-term storage, ESD Control, segregation, environment control with strict monitoring.**

***IndexTerms*—EEE Parts, Inventory, Bonded Stores**

I. INTRODUCTION

EEE (Electronics, Electrical & Electromechanical) parts are the building blocks and hence the Quality & Reliability of the constituent parts determine the success or failure of a Space mission. An effective Part Management Program (PMP) therefore shall be implemented that should cover all the elements, right from selection and acquisition of the parts till the usage/EOL on-board performance. The management of parts inventory with proper storage and safe handling, is one of the key element of a comprehensive PMP. This paper describes, the parts stock/inventory management methodology and procedures, being followed for Space Payload systems, at SAC/ISRO.

II. NEED OF AN EXCLUSIVE FACILITY

A space project typically requires more than thousand different part-types, several thousand different line-items amounting to hundreds of thousands of parts. Typically, 10-20 % of the spacecraft cost is shared by the parts used to build it.

In the current scenario, multiple payloads are under development in parallel and time schedules are squeezing. These challenges essentially demand the "right-part on right-time" mechanism to attain the set goals of Time schedule and Reliability.

To mitigate the effects of longer procurement cycles, limited sources, diminishing & obsolescence threats, "Volume-buys" approach is adopted for space part procurement that necessitates an effective Parts inventory management alongwith long-term storage and safe handling procedures implemented. The Bonded Stores at SAC, is the exclusive entity that fulfils all these requirements.

III. THE BONDED STORES

The Bonded Stores, preserves and distributes EEE parts for the realization of space payload systems. Besides the EEE parts, other electronics items i.e. fabrication material, bare PCBs, packages/sub-systems/modules are also preserved/stored.

Fig. 1. Bonded Store, SAC

Through multi-step verification & regulation in the Bonded Stores, it is assured that only APPROVED items are issued for the system realization.

A. Environment conditions and control

In the bonded stores area, the environmental conditions are controlled and maintained round the clock and in full compliance with ISRO-PAX-300. Environment parameters are kept within the limits and strictly controlled as below.

- Temperature: 22°C ± 3°C
- Humidity: 50 ±10% RH

Temperature and humidity are continuously measured with calibrated instruments and recorded.

- Light intensity: 100 ft. Candle (min.)

The lighting is uniform, shadow-less and free from severe reflection for correct execution of the tasks.

- Cleanliness: Class 1 Lac as per ISRO-PAX-300 with ±ve pressure

Potential sources of contamination are controlled & maintained. Entry/Exit is separate and isolated for Main storage through Air Showerto prevent ingress of

contaminants. Cleanliness level is measured using calibrated Particle counter.

- ESD Safety / Measures / Control: ESD control system is implemented to ensure that electrostatic potential difference is reduced below the sensitivity levels of items.

Work table mats are Static dissipative (10^5 to 10^{10} Ohms/square) and grounded through 1 MOhm resistance.

All working personnel, are suitably connected to ground through wrist straps. Work tray, containers, bags, tools, garments, foot-wears, chairs used are also made from static dissipative material.

Fig. 2. ESD Safe Work Stations

The entire floor is made up of Static dissipative tiles with adequate grounding.

The efficiency of ESD control measures are periodically verified and Independent audit is also carried out as per defined schedule per ISRO-PAX-300 guidelines.

Access rules applied for personnel, materials & equipments.Adequate surveillance aided with CCTV system, Fire-safety system with alarms and unobstructed emergency exit are also in place. Furniture is minimum and allow the easy and thorough cleaning.

IV. PARTS INVENTORY MANAGEMENT SYSTEM

The management of Parts Inventory is necessary to know how much stock is available at any time with its full traceability so as to facilitate users to have visibility of existing stock and its availability at production time.

Realizing these needs, a customised software was developed and made operationalised at SAC since 2006. This software, named as Bonded Store Inventory Management System (BS-IMS) Software, is the core part of inventory management and real-time operations of the Bonded Store transactions.

The BS-IMS Software was developed in Java technology using Struts 2 Frame work and upgraded twice thereafter. It is extensively used to know the availability and transactions of the items (EEE parts, PCBs, Packages, Fabrication Material) by users from Projects, QA/QC, PFF & other facilities.

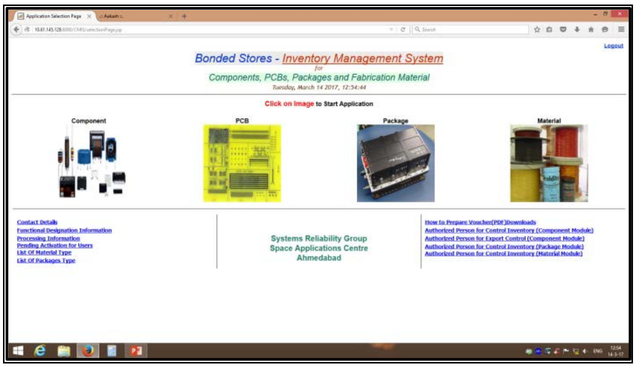

Fig. 3. BS-IMS Portal Homepage

A. Development Technology

- Application is web based developed in Java with struts 2 frame work.
- Webserver: Apache Tomcat 7.0
- Database: SQL server 2008 R2 (Relational database)
- Operating System: Windows Server 2012

B. Accessibility

The BS-IMS Software is hosted on 24 X 7 s erver and accessible through SACNET as well as SPACE NET across the ISRO centres.

At present, there are 600+ user accounts and there is no limitations or restrictions for simultaneous usage and accessibility.

C. Database Volume and Structural Complexity

- No. of Screens: 125 (30+ screens are of high complexity: 40 Fields, 25 buttons)
- No. of Reports: 60
- No. of Tables: 60 (at least 20+ tables are of high complexity: upto 40 fields)

D. Key features

- Web based software system, Menu Driven with user friendly comprehensive GUI.
- Total Four Modules (one each for Components, PCBs, Packages, Fabrication Materials) for transactions and know about stock availability.
- User and Role based authentication and assignments of rights.
- Five Transaction Typesi.eDeposit, Issue & Return *(Screening, Fabrication,Construction/Failure Analysis, MRB, Tinning, Compatibility etc.)*,Transfer between projects and Reservation.
- Configuration screen for addition of new projectsand stocks, user & projects, projects and project stock, projects & authorization etc.
- Complete information for Quality and Quantity of the stocked items.
- Complete information on transactions; (Project wise deposit/issue/return over a time span/period, for each item with history records.

- View availability of'All items' across all the project stocks.
- Views and reports as per customised requirements.
- Reservation of items for contingency.
- Master Database (MDB) Part No creation and approval online.
- Upload/Download of End Item Data Package (EIDP) i.e. Test reports, CoCs and other documents pertaining to deposited items.
- Assignment of location tag to deposited items for easier and faster access.
- On-line Components Screening request by users.
- Import of BOM prepared using excel sheet to prepare SIVs.
- Notification to user on processing of voucher through email.
- Inventory control of "Export controlled" and "Critical" items.
- Mapping of unused stock to new project(s) with complete screening history.
- Threshold limit setting with notification to user through email
- Auto cancellation of transaction request after stipulated time to prevent undue reservation and release of items for other user

V. OPERATIONS & WORK FLOW

The item(s) first time deposited into the Bonded stores is allotted an *IssueNo*, sequentially per deposition batch/lot. Prior to deposition of the item, an MDB No (Master Data Base no) is created/generated that comprises of key information coding of the respective part.

The structure of the MDB No. is standardised for each category of the items. For example; an MDB No for a transistor is as below;

TABLE 1. MDB No. Structure Example

Part No	Package	Pins	Quality	RHA
2N2222A	TO-18	3	MIL-S	100K

The items are stored *IssueNo* wise. Each transaction thereafter, from/to the Bonded Stores for screening, inspection, fabrication, storage and other purpose is done through Voucher. Each voucher has its reference no (VoucherNo) linked to the respective *IssueNo* of the respective item.

A. Deposition procedure

Store Deposit Voucher (SDV) is prepared using allotted MDB No of the item and submitted for deposition of the item in the Bonded Stores. The FM item(s) is deposited in UNSCREEN Grade and LAT item in the TS grade.

B. Issue/Withdrawal procedure

Store Issue Voucher (SIV) is for the withdrawal of the items from the Bonded Stores for screening, testing, fabrication, MRB (Non-conformance disposition) and other purposes. Item withdrawal is restricted and only authorised persons have the withdrawal right.

Fig. 4.Issue / Deposit process

C. Return procedure

Store Return Note (SRN) is used to return the (earlier withdrawn) items after completion of screening, inspection, testing etc. The returned item is deposited under appropriate grade i.e. ACCEPTED, REJECTED etc.

D. Reservation procedure

Through Store Reservation (SRV) Voucher, the items are allowed to be reserved for contingency situation.

E. Transfer Procedure

Store Transfer Voucher (STV) is to be used for transfer of the items from one project stock to another project stock, with previous linkage and history.

VI. STORAGE MECHANISM AND METHODS

The entire area of the Bonded Stores is divided (with physically isolation) into five different zones.

EEE parts, material & PCB zone having three separate sub-zones with clear demarcation. The items are stored separately as SCREENED, UNSCREENED, ACCEPTED and REJECTED with identification labels and History cards with full traceability and quantity account.

Fig. 5.EEE Parts Storage

The ESD safe modular boxes are used for storage of these items having traceability with Issue No. tagging.

Packages / sub-system zone wherein the In-house fabricated as well as procured packages, assemblies, modules and sub-systems are stored.

Fig. 6.Package / Sub-system Storage

The storage location and item *IssueNo* is cross-referenced with each other and computerised for identifying and faster retrieval of the item for issuance.

Critical parts zone is specifically for storage of the critical items. Special storage Cabinets having dehumidier / desiccator with Auto Nitrogen flow mechanism in-built are in place for the storage of critical parts like MMICs, Semiconductor Chips (Dice), CCDs, Optical filters & lenses, Silver plated parts, O2 sensitive parts. In these cabinets required level of humidity can be set, control and maintain to guarantee the integrity of stored items

Fig. 7.De-Humidifier Chambers

In the Critical parts zone, an exclusive facility of dry Nitrogen purging and sealing is installed for the packaging of humidity sensitive and silver plated items for long storage. This method of item packaging with Nitrogen purging is very effective to preserve sensitive items for longer storage without degradation.

Fig.8.Nitrogen purging facility

Considering traceability as a prime requirement for items used in space systems, a comprehensive End Item Data Packages (EIDP), consisting of Test reports, Certificates and documents are shipped with procured items. These EIDPs (Hard Copy and/or soft copy) are preserved with respective *IssueNo* linkage and maintained in the Document archives / zone.

User interface & interaction zone is for receipt and issue of the Items, Vouchers. Verification, voucher processing tasks. User interaction and paper work is done here.

For better management, storage effectiveness and to rule out possible mistakes/errors, following implementation is done.

- Program/Project wise segregation with S creened and Unscreened items stored separately with records.
- Segregation, identification and correct labelling of the items.
- Multi-step verifications and logging during deposition and issuance of the items.
- Rejected items are quarantined and disposed-off after stipulated time.

Fig. 9. ESD safe stress-free storage

- Use of the ESD Safe Tools during handling, transfer, re-packing of Sensitive components/items
- Periodic training and sensitisation to working personnel for handling of the items, ESD control awareness and execution of the jobs.
- Data packages and Documents (deposited with items) are well preserved, maintained and made available to users for reference.

ACKNOWLEDGEMENT

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Authors also acknowledge Paper Reviewers; Shri A.N. Bhattacharya, DD ESSA/SAC and Dr. S. C. Bera, Head SNSED/SAC for their critical & value adding suggestions.

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Space grade EEE component procurement – Centum Capabilities and Experience

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***Abstract*—Space is not only one of the harshest environments that electronics need to operate in, but it's also one of the hardest to replicate. The grades of EEE components contribute a significant portion to the quality and reliability of the space mission. The characteristic features of Space grade EEE components like low volume requirements versus minimum order quantities, high value, huge amount of technical data pack, pre-shipment clearance requirements, long lead times and limited source of suppliers are to be well understood to strategize the procurement process. The statutory requirements like Export License procedures, documentation and compliance to End use requirements are additional complexities to be addressed.**

This paper details the capabilities and experience of Centum Electronics team in technically and operationally managing the Space grade EEE component procurement process. The systems followed, ERP tools used, tracking mechanism and interdisciplinary team involvement covering design, sourcing and quality and the roles and deliverables of each of the teams in successful procurement are highlighted in the paper.

***Index Terms*—EEE component procurement, ERP, End-Use certificate, ITAR**

I. INTRODUCTION

Various Space agencies across the globe establish baseline criteria for selection, screening, qualification, and derating of EEE parts for use on space flight projects. ISRO is no exception and clearly has very well established guidelines on EEE parts selection and procurement for different types of programs like Launch vehicle, LEO and GEO missions.

The 'grade' or the 'level' of the EEE components is generally classified into three categories.

- Level-1: Parts for highest reliability and lowest level of risk with mission life more than 5 years.
- Level-2: Parts for low to moderate level of risk with mission life of 1- 5 years.
- Level-3: Parts for mission applications where use of high risk parts is acceptable. Sometimes, these are used for initial development, engineering or Proto models for use on ground, prior to procuring the expensive, long lead time parts of Level-1 and 2.

These parts are reviewed for radiation hardness and if required, specific radiation tests need to be performed.

The selection of the EEE parts is an interdisciplinary responsibility covering Designers, Quality agencies, Parts procurement teams, Material specialists and Radiation experts. However the procurement activity, which is the topic of relevance in this paper, is also interdisciplinary with additional team members coming from Project (for timelines), Finance (for commercials) and Sourcing (for alternate source management) as shown in Fig.1.

Fig. 1. Procurement specification finalization team

Centum Electronics Limited is a leading Indian Electronics Design and Manufacturing company in Space and Defense sectors[1]. The "Space-journey" at Centum has started in 2001 and several successful turn-key projects have been executed for various ISRO missions with hundreds of modules and subsystems onboard every ISRO mission since 2003. An important capability in turn-key space project execution in both BTS (built to spec – design to delivery) and BTP (built to print – manufacture to customer design) mode is the ability to procure the right grade of components, process the documentation (technically, commercially and meeting the statutory compliance like Export license requirements), store the parts and use them for the space electronics hardware.

The following sections give the details of specialties of Space EEE component procurement, Centum Capabilities and advantages it offers for its customers, Challenges faced and Processes followed.

II. SPACE EEE COMPONENT PROCUREMENT SPECIALTIES

The following are the special features of space grade EEE component procurement.

- For a given program in BTS mode, one has to procure at least two grades of components viz., industrial/MIL grade for initial development, prototype models and Space grade rad-hard components for Flight models.
- The quantity required is very small to small and hence the Minimum Order Quantity (MOQ) and Minimum Order Value (MOV) challenges are to be dealt with.
- Many times, there are single approved vendor situations making it extremely difficult to negotiate on technical and lead time related requirements.
- Very high value Class-A components also generally have very long lead times resulting in significant impact on project timelines.
- The date code requirements for space application will have significant bearing on the cost and lead times.
- Obsolescence is a c ontinuous threat in space component procurement.
- Non-compliance management during the procurement process, sometimes getting into a situation of “take-it-or-leave-it” from the supplier end, poses significant challenge to bridge the gap between “the requirements of the customer and capability of the supplier”.
- Documentation gaps between the requirements and the deliveries with over-riding project schedules.
- Unclear lead times for Export License clearances. This can be from few weeks to few months.
- Multiple programs need multiple time procurement of the same component, each time with low quantities and with different end use documentation.
- Some times after accepting the order, suppliers report issues on the lot qualification tests thereby creating huge setback to schedules.

III. CENTUM CAPABILITIES AND ADVANTAGES

With a very strong Design, Engineering and Manufacturing capabilities in Space domain and with a credible history of more than 15 years, Centum has the following capabilities in EEE parts procurement area:

A. Technical:

- Technical teams with ability to understand differentiate and match the requirements in grade of components for different space missions.
- Strong experience of preparing the procurement specifications document with clearly spelt requirements on grade of parts, documentation requirements, screening and qualification requirements and applicable standards as given in Fig 2.

Fig. 2. Constituents of a typical procurement specification

- Well established procurement specification approval systems with internal and external stake holders sign off.
- Bank of approved procurement specification documents that can be very handy for expedited procurement for short execution lead time programs. Once approved, for the same or similar application, there is no need for second time approval of the component specifications.
- Ability to interact and negotiate on technical matters with the suppliers, during the procurement cycle.
- Strong Incoming Goods Inspection (IGI) team to inspect and clear the components received along with necessary documentation and Parts Review Board decisions if applicable.
- Ability to do Up screening activity when left with no options.
- Presence of a Component Engineering team to help procure quickly and more efficiently by alternate management using software tools having alternates suggestions for most of the components.
- Well established Parts Review Board (PRB), Non-Conformance Review Board (NCRB) and Materials Review Board (MRB) to take quick decisions. Customer team is also involved to help take the expedited decisions.

B. Managerial/Operational:

- Strong history of procuring large amount of electronic components from most of the standard and approved vendors across the globe for its hi-rel customers in defense, industrial and medical sectors apart from Space grade EEE parts procurement.
- Being a direct account, the large scale procurement from reputed component manufacturers results in strong access to the technical and application teams at the supplier end, including the quality teams, resulting in seamless interaction on all technical matters and clarifications. This significantly enhances the speed of procurement, once the decision or selection is made.

- Ability to effectively use the ERP and other software tools to automate the procurement process helps in tracking the status of each of the component ordered.
- Strong procurement teams comprising commodity wise members with their experience in International component procurement, follow up and compliance background.
- Trained resources to deal with the Export license requirements, paper work and other statutory requirements.
- Being an Export Oriented Unit, the ability to handle the logistics, freight forwarders, expedited and normal consolidation systems and extensive experience of in-wording the components through government clearing procedures such as customs.
- Ability to consolidate annual requirements and negotiate better for lead times by multi-batch deliveries.
- Capability to travel to any supplier across any part of the globe and track the supplies and ability to Negotiate the lead times and reaching out to Escalation hierarchy at Supplier end with speed for expedited deliveries.

IV. PROCUREMENT FLOW AND CYCLE TIME

A typical set of activities that form a procurement cycle for EEE components of a space project is given in Fig.3.

Typical cycle team of successful component procurement depends on the component, its earlier procurement history, availability in active list at Supplier end. For a totally new part or a totally old part needing fresh manufacturing, the supplier lead times vary between 20-50 weeks. The task will always to bring them under a maximum lead time of 26 weeks. More proactive measures, correct documentation, minimizing back and forth interactions can clearly cut down around 6-8 weeks of lead times. Many times, business considerations at supplier end will also result in pleasant surprises reducing the lead times.

A judicious combination of techno-commercial interactions, use of all previous learnings, proactive measures like forecasting to the suppliers, combining multiple project requirements and other such actions help reduce the lead times.

Use of technology, video conferences, quick responses, regular and need based visit to suppliers across the globe can help build the rapport with the supply chain partners and help in lead time reduction.

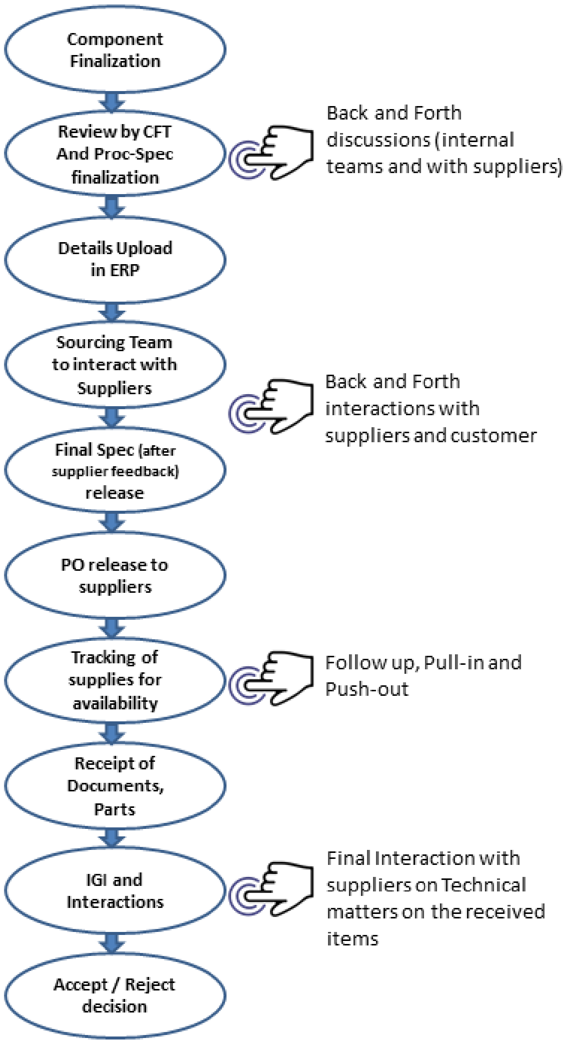

Fig. 3. EEE component procurement flow at Centum

V. PROCUREMENT EXPERIENCE

Centum is one of the leading Indian Private industries who started procuring the space grade EEE components since 2002. The types of components procured are increasing year by year. The Table1 gives the overview of types of components procured and the grade to which they are procured.

TABLE I. OVERVIEW OF COMPONENTS PROCURED

Type of Components	**Remarks**
Passives (Resistors, Capacitors, Inductors)	Respective MIL Standard and best available failure rate, typically FR “S” or better
Semiconductor	JANS as per MIL PRF 19500

Devices (Diodes, Zeners, Transistors, MOSFETs etc.)	JANKC as per MIL PRF 19500
Microcircuits (Opamps, Digital ICs, Regulators)	QML V as Per MIL PRF 38535 Class K as per MIL PRF 38534
Magnetics	Space Grade Parts
Bare Boards	Space Grade
Mechanical Housings, Fasteners	Space Grade for bought items. Fabrication in Certified and Qualified vendor

For Centum, the procurement of space components has been a continuous learning experience. There have been few instances of challenging situations, as given below, where the understanding errors coupled with supplier shipment related errors have brought schedule related challenges.

- Instead of a die, a packaged device is ordered.
- Instead of an ordered DIP (through hole) IC, a SMD packaged IC has been received.
- After a long wait for the arrival of parts, a communication received regarding the failure of the lot at the supplier end, have resulted in schedule overruns.
- Documentation errors / missing data packs have resulted in situations where the parts are available, but could not be cleared for use onboard, due to incomplete consignment.
- Clarifications back and forth, after the parts are received, also have taken significant time to keep the parts ready for use.

It is the ability to quickly get over such challenges, and get the deliveries back on track, that will determine the capabilities of supply chain cycle

VI. CONCLUSIONS

During the earlier years, the Indian space industries were neither ready, nor allowed to procure EEE components. However, the scenario has drastically changed. For a successful outsourcing of space electronics hardware in turnkey mode, the component procurement responsibilities lie with the outsourced partner. Centum Electronics, through its supply chain management, has successfully demonstrated procurement of EEE components in large variety and quantity. The ability to understand all aspects of procurement from design, preferred parts list, procurement specification, export licensing procedures, ERP driven ordering and tracking, interaction on technical and commercial areas with the supplier base have made Centum a key turn-key space grade solution provider in Space for ISRO.

ACKNOWLEDGMENT

The authors would like to thank the sourcing and procurements teams at Centum Electronics for sharing their “continuous learning” experiences towards procuring space component. It is only through interactions with ISRO scientists that team Centum has understood the adage that no detail is trivial. The comprehensive reviews conducted by team consisting of members from all the technology area that leave no s tone unturned in terms of addressing all details and this review process is indeed the foundation for successful procurement of parts prior to product realization.

Special thanks are due to the quality teams of ISRO Centers for handholding Centum team towards improvisation of procurement specifications, resolution of technical deviations resulting in successful component procurement for on-time delivery of critical space projects.

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Counterfeit Part Control Plan and Obsolescence Management of EEE parts in Space systems

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Abstract: A counterfeit electronic component is one whose material, performance, or characteristics are knowingly misrepresented by the vendor, supplier, distributor, or manufacturer. The existence of counterfeit Electrical, Electronic, and Electromechanical (EEE) components, materials and assemblies is not a new phenomenon. In space missions, it is absolutely essential to implement a counterfeit parts control plan to reduce the risk and costs associated with re-working systems with bad parts, or a worst case scenario of catastrophic failure after launch. The consequences can, obviously, be drastic when critical systems begin to fail due to the use of counterfeit or low-quality components.

With the advancements in the field of technologies, the need for high performance, high density parts are ever increasing. Due to the growth in electronic components supply chain, a diverse set of suppliers have emerged thereby increasing the global trade of counterfeit parts. Space hardware systems are often having long design cycle, which makes them particularly susceptible to counterfeiting, due to problems with the availability and obsolescence of the parts used in these systems.

We are moving towards Productionisation to increase the number of satellites to be launched per year to meet our societal needs. In this direction, satellite production is planned to be outsourced to the industries. Hence a robust counterfeit parts control plan and obsolescence management should be in place.

This paper provides an overview of counterfeit avoidance & detection techniques and obsolescence management of EEE parts to achieve our goal of "Total Quality and Zero Defect in Space Systems and Services.

Keywords : Counterfeit part, Control Plan, obsolescence, avoidance & detection methods

I. INTRODUCTION

A counterfeit part is a fraudulent part that has been confirmed to be a copy, imitation, or substitute that has been represented, identified, or marked as genuine, and/or altered by a source without legal right with intent to mislead, deceive, or defraud.[1]

A counterfeit component 1) is an unauthorized copy; 2) does not conform to Original Component Manufacturer (OCM)design, model, and/or performance standards; 3) is not produced by the OCM or is produced by unauthorized contractors; 4) is an off-specification, defective, or used OCM product sold as ''new'' or working; or 5) has incorrect or false markings and/or documentation. Based on the definition, counterfeit parts are classified into seven categories (Fig 1) :

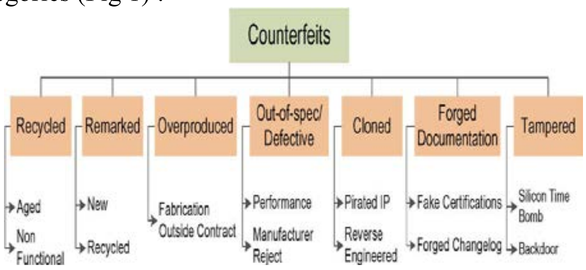

Fig. 1: Shows the taxonomy of counterfeit components [2]

During the infancy of the semiconductor industry, a single company performed specification, design, manufacturing, and testing. Today, technology development and production are globally dispersed. As the technology evolved, and the semiconductors became smaller and more complex, the costs of in-house manufacturing became prohibitive. As is the case in many industries, it became cheaper for a company to send design specifications to an external facility that would manufacture semiconductors for multiple entities, thereby capturing economies of scale and reducing production costs. As a result, semiconductor technology continues to evolve, leading to the production of ever-advancing systems that are superior to their predecessors. However, semiconductors are among the electronic parts that are the most prone to counterfeiting and other forms of manipulation. As the component supply chain has become globalized and thus more complex, additional sources of failure have become a concern. Specifically, the trustworthiness of supply chain is much harder to assess. Even if these semiconductors work initially, they may have a r educed lifetime and can pose reliability risks. The counterfeit devices are expected to have shorter time to failure compared to brand new (original) devices. Fig. 2 illustrates typical device failure characteristics, often known as the bathtub curve.

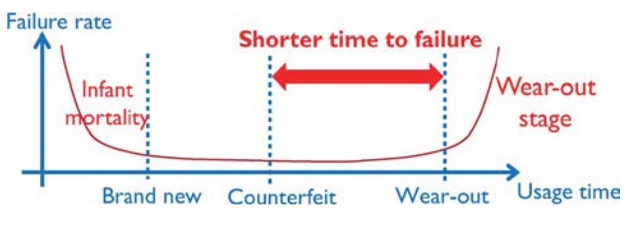

Fig. 2. The classical bathtub curve illustrating typical device failure characteristics [2]

II. WHY IS SPACE SYSTEM MORE PRONE TO COUNTERFEITING? [3]

The following are the main reasons behind the possibility of existence of counterfeit parts in space systems :

- With the advancements in the field of technologies, the need for high performance, high density parts are ever increasing which may lead to usage of commercial parts.
- Space hardware systems are often having long design cycle. Hence non-availability and obsolescence of the parts is a major concern.
- Even when obsolescence is planned for, long program life cycles may still require the purchase of obsolete parts. User may be required to go out to the independent market
- Usage of space grade components is less compared to commercial devices. So commercially it is not viable for manufacturers to continue building these devices for a long run
- Supply chain has become complex and extreme price pressure exists.
- Due to the global nature of supply chain, many critical activities are outsourced. Suppliers of goods and services are spread all over the world. Keeping track is difficult.

III. COUNTERFEIT PART CONTROL PLAN IN SPACE SYSTEM

Counterfeiting is not a static process. As new methods are devised by industry to discriminate fraudulent/counterfeit Electrical, Electronic, and Electromechanical (EEE) parts, new methods are introduced by counterfeiters to disguise their parts. In order to assure mission success it is absolutely essential to implement a counterfeit parts control plan to reduce the risk and costs associated with re-working systems with bad parts, or a worst case scenario of catastrophic failure after launch. In space system, a single failure is unacceptable, so a stringent control plan is mandatory at each level to avoid failure due to counterfeit part. In an effort to keep ahead of the evolution of counterfeiting, we should continue to develop new and/or revised techniques to mitigate the risk of use of fraudulent/counterfeit EEE parts and a robust counterfeit parts control plan and obsolescence management should be in place.

A good Counterfeit parts control plan has several practices to identify fake parts. They are broadly classified into counterfeit detection and counterfeit avoidance methods. Counterfeit detection focuses on the detection of counterfeit parts in the supply chain whereas counterfeit avoidance concentrates on adding extra hardware in the circuit such that a suspect part is authenticated without costly and time consuming detection methods (e.g., design for counterfeit avoidance, design for test, design for security)

IV. Counterfeit Control Plan

- Avoidance
- Detection
- Disposition

a. Avoidance

The avoidance methods addresses how to prevent counterfeit parts from entering into supply chain and to identify counterfeit parts without performing the costly and time consuming detection methods.

- Avoidance begins with the choice of suppliers in the supply chain. Preferably procure devices from QML/QPL(Qualified Parts List / Qualified Manufacturer List) certified manufacturer. It starts during the procurement stage itself. Authorization letter should be demanded during procurement.
- Knowing the people, policies, and practices of manufacturers is the best up-front way of knowing what you're buying before parts even come through the door. All it takes is a single gap or unexpected supplier in the chain for counterfeit parts to get in. [3]
- Documentation should be scrutinized for unrecognized sources in the supply chain and affected lots flagged for closer scrutiny. [3]
- The vendor shall maintain a method of item supply chain traceability that ensures tracking of the supply chain back to the manufacturer of all Electrical, Electronic, and Electromechanical (EEE) parts included in assemblies and subassemblies being delivered. This supply chain traceability method shall clearly identify the name and location of all of the supply chain intermediaries from the manufacturer to the direct source of the product for the seller, and shall include the manufacturer's batch identification for the item(s) such as date codes, lot codes, serializations, or other batch identifications."
- Specify flow down of applicable requirements of our control plan to applicable contractors and their sub-contractors. In the event that one or more supply chain intermediaries do not have a fraudulent/ counterfeit part control plan compliant to our control plan, a risk analysis shall be required for every application of the part.

b. Detection

Over the past several years a specialized service of testing has been created for detecting counterfeit components. The components must be authenticated by these tests before being placed in systems. Fig 3. shows a generalized classification of counterfeit detection methods[2]. The methods are broadly classified into physical and electrical inspections.

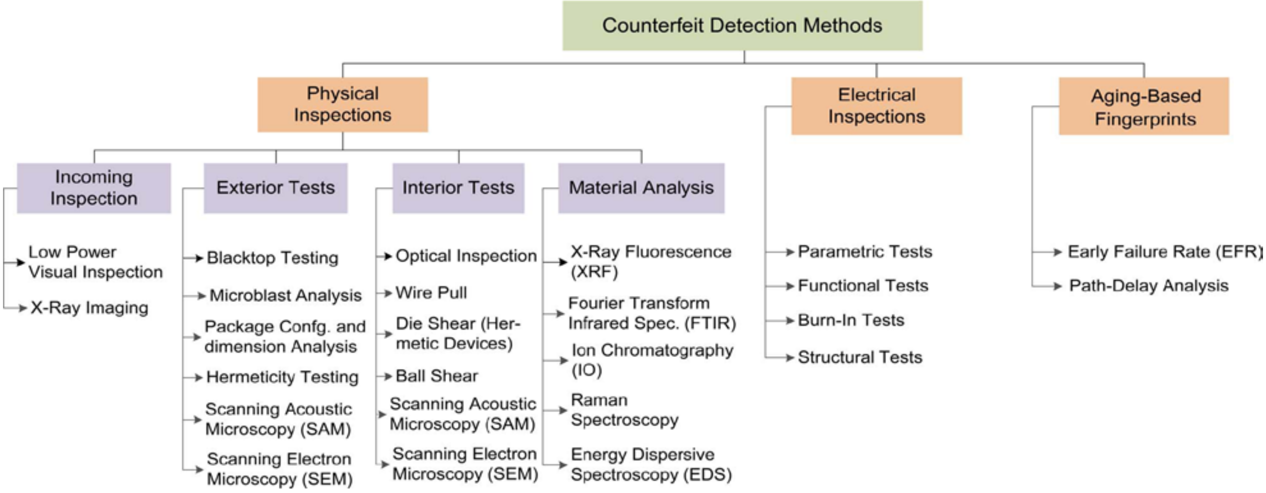

Fig. 3. Classification of counterfeit detection method [2]

A sequence of Verification of Quality (VoQ) that are carried out at our end to detect fake parts are:

- Visual examination by trained personnel to verify leads, package condition ,marking on device(part no , date code, serial no etc), manufacturer, country of origin.
- Verification of r eceived documentation (i.e. Certificate of Conformance, purchase order, packing list) to confirm authentic conforming parts and traceability to manufacturer, part number, date code, lot number, and/or serial no.
- Marking permanency tests may be used to detect re-marking and blacktopping
- Radiographic examination to inspect the internal structure of a component without decapsulating the device .
- Life Tests to ensure the long term reliability of the component.
- Destructive Physical Analysis to check workmanship of the device.
- Electrical testing wrt to detailed specification to determine if device is functional & operational.
- Seal leak tests on samples to check the hermiticity of device.
- EDAX to determine the composition of lead material.
- Scanning Electron Microscopy to verify the quality and acceptability of device interconnect & metallization thickness of wafers or dice

c. Disposition

- Appropriate decisions have to be made by authorized personnel/review boards within an Organization concerning future treatment of nonconforming parts.
- Dispositions may be to scrap, use-as-is (normally accompanied by an approved variance/waiver), retest, rework , repair, or return-to-supplier based on the severity of the non conformance and criticality of the part .
- Proper disposition of known or suspected counterfeit parts prevents their reintroduction into the supply chain. It is critical that parts dispositioned as counterfeit are reported and quarantined so that they do not re-enter the supply chain.
- As counterfeiting increases, both suppliers and customers must be informed and vigilant. Lots conclusively identified as being counterfeit should be reported to organizations such as GIDEP, ERAI, and applicable Government investigative authorities.[3]

V. PRODUCTIONISATION AND COUNTERFEIT CONTROL PLAN

As we are moving towards Productionisation to increase the number of satellites to be launched so as to meet our societal needs and also, as satellite production is planned to be outsourced to the industries, it is imperative that a good counterfeit parts control plan should be laid down. A document containing all guidelines pertaining to avoidance, detection and disposal techniques to be provided to Contractors and subcontractors at all tiers. Strict adherence to this is mandatory. Any deviation from this to be notified to the concerned personnel/review board. Regular auditsto be carried out and continuous vigil to be kept on them to control entry of counterfeit part in the supply chain.

VI. COUNTERFEITING AND OBSOLESCENCE MANAGEMENT

Obsolescence Management is needed to mitigate the risk of electronic component obsolescence and counterfeiting. Driven by constant and rapid technology changes, component obsolescence has long been a fact of life for users and managers of electronic components. Electronic components can become obsolete in the span of very short period due to the extreme pace and scale of technology shifts in the electronics industry. Manufacturers of electronic components frequently abandon old technologies for new ones to stay competitive. In this environment, the length of time required to develop and test complex systems, virtually ensures that many electronic components that were state-of-the-art in the design phase will be obsolete before the systems they are embedded in can be fielded; unless obsolescence management is part of the system lifecycle from the beginning. Space hardware systems are often having long design cycle, which makes them particularly susceptible to counterfeiting, due to problems with the availability and obsolescence of the parts used in these systems. E ffective obsolescence management strategies can save a lot of money and time, by avoiding the redesign of end products or entry of counterfeit parts in the system. The following are the solutions to mitigate the risk of obsolescence: [6]

- Finding alternate (drop-in) replacement from a different reputed manufacturer
- Costly 'last time buys' (LTB) or 'Die Banking'. Buying the components in bulk and store them in inventory for future needs.
- Finding nearest equivalent alternate part, to reduce the redesign cost.
- Creating a custom component similar to the obsolete one, and having a contract signed with a qualified manufacturer for a certain period.
- Redesign a sub-section or entire product.
- If buying from open market, check for the credibility of the supplier. Electronic Supply chain traceability should be there at each level (Wafer Manufacturers, Chip Manufacturers, Board Manufacturers, System Manufacturers, After Market Sales and Refurb Support, disposal/recycle)

VII. CONCLUSION

Counterfeit Components are major source of concern in the electronic component supply chain because of reliability issues .The long design cycle and global supply chain make Space System prone to counterfeiting. A concrete Counterfeit Control Plan to be implemented in our system as productionisation is the need of the time. The Counterfeit Control plan for EEE parts comprises of counterfeit avoidance measures to emphasize what needs to be done in order to detect these counterfeit components in a proactive, rather than reactive manner & various detection techniques to control the entry of fake parts in the supply chain . Proper disposition, if encountered with a fake part, is key to mitigating the reentry of counterfeit part in the supply chain. This paper illustrated the overview of the robust Counterfeit Component Control Plan which we follow to achieve our goal of "Total Quality and Zero Defect in Space Systems and Services".

ACKNOWLEDGMENT

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Strategic Components Initiative Towards self-reliance in strategic electronics

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Abstract— **The National Policy of Electronics was approved by the Union Cabinet in 2012 to create an indigenous manufacturing eco-system for electronics in the country and foster the manufacturing of indigenously designed and manufactured chips creating a more cyber secure ecosystem in the country. This paper evaluates similar initiatives undertaken globally and suggests an approach relevant to India towards the creation of IP and the realisation of high reliability EEE components within the country. This approach calls for a close partnership between the national agencies in the strategic sector and the Indian electronics industry by leveraging the expertise and infrastructure built over the past several years and has immense potential in positioning the country as a global leader in the niche market of high reliability EEE components, ultimately leading to a position of prominence in the global electronics market**.

Index Terms— *ESDM, AESDM, Strategic electronics*

I. INTRODUCTION

The National Policy on Electronics [1] was notified by the Government of India in 2012 with the vision to transform India into a global hub for Electronics Systems Design and Manufacturing (ESDM) and provide the necessary policy interventions and support for creating the right ecosystem within the country in order to nurture a globally competitive electronics design and manufacturing industry.

In order to replicate the success in the software and software services sector, the policy outlines several initiatives to address the gap areas to accelerate the growth of ESDM to meet the increasing domestic demand and the potential export demand. The biggest challenge here is to achieve the status of a global player in the presence of major competitive players such as China, Korea and Japan, who have achieved the status of giants in ESDM. The Make-in-India Strategy for Electronic Products argues in favour of an export-oriented strategy, considering the smaller domestic market ($65 billion) in relation to the world market, which is in excess of $2 trillion. The strategy targets to emulate the Chinese strategy to go for the larger market to exploit the economies of scale and agglomeration to become globally competitive [2].

This paper examines the strategies adopted by the global giants in the area from the latest perspective and argues for an alternate Aerospace Electronics System Design & Manufacturing (AESDM) strategy to carve a niche in the area of high quality & high value strategic electronic components and systems. The attainment of global leadership in this vital area could be the cornerstone from where the country can expand into the global electronics industry. This strategy is made possible by the collective experience gained over the decades within the national departments of space, defense and atomic energy.

II. ACQUIRING COMPETITIVE ADVANTAGE

What is responsible for the rise of an industry? The managerial perspective identifies core competence as the primary sources of growth of firms, industries and organisations; whereas the economic perspective emphasizes national productivity and efficiency as the basic source of growth [3]. The market or demand is the prime mover of productivity increase across nations. The National Policy on Electronics has rightly identified the electronics industry to be the fastest growing manufacturing industry in the world and the domestic demand is expected to reach $400 million by 2020 [1]. However, in spite of the presence of more than 200 companies in the area of electronics & semiconductors along with the skilled labour, India's total electronics hardware production in 2014-15 was just 1.5% in world electronics hardware productionand has less than 1% share in the export market [2]. Moreover, this industry has received just 0.66% of the total FDI flow in the country during 2000-15 and contributed only 1.7% of the GDP [2]. While the National Policy aims to create the right ecosystem within the country, it has to be properly backed up with the right strategy to utilize the opportunity existing at the moment.

It is worthwhile to bear in mind the three Cs: (1) the principle of Competitive advantage, (2) the principle of Comparative advantage and (3) the principle of Core competence. Together they form a growth synergy: a cumulative process of sustained growth through a complementary set of principles of action [3]. The principle of competitive advantage emphasizes the network of opportunities that exist in the given environment and the dynamic strategies that may be adopted to exploit them [3]. While it is true that there is a huge global electronics market, it is obvious that it requires far more than a fertile ecosystem to tap into this demand overcoming Chinese and Korean dominance (and low-cost), considering the late entry and the

brand perception of India in this specific area. It is to be noted that Samsung in Korea rose to prominence through cost efficient clones and new products at cost efficient prices. China seized the opportunity presented by the high technology companies who were looking for low cost outsourcing of their manufacturing requirements to clock high returns. If India has to grab a major share of the market addressed by the likes of China, Korea and South-east Asia, it has to overcome its own image as a small time player in the global as well as the domestic markets. This is illustrated by the Indian consumer's preference for a globally branded computer in spite of home grown PC companies in the country. Hence, the optimum strategy is to focus on a market which is not served by the globally established Asian players viz. the space and military electronics market. The opportunity that exists in this sector can be summed up in two terms – obsolescence and counterfeiting. This sector is characterized by long product cycles, low volumes and the requirement of high reliability. Recently this sector has been plagued by the limited availability of electronic components due to obsolescence and the dwindling of older technology nodes to make way for higher technology nodes driven by the more lucrative mobile phones and consumer electronics market.The danger of unintentional sourcing of counterfeited components from China has been causing a lot of concern to the aerospace manufacturing industry. The design, development and manufacturing of high reliability electronic components presents an opportunity for the country to achieve global leadership and is in line with the principle of competitive advantage. This capability exists in pockets within the national agencies of space, defense and atomic energy including the knowledge base required for the testing & qualification of such components, which could be consciously leveraged and disseminated to capable indigenous industries to establish global competitive advantage.

The string of successes achieved by the country in space technology especially the Mars Orbiter Mission, the development and operationalization of satellites and space transportation systems like PSLV and GSLV,including the associated high reliability avionics and the successful establishment of a robust test infrastructure provide the country a comparative advantage, which could be leveraged to build brand India as a manufacturer and supplier of components and systems including the quality certifications required for aerospace and defense. The specific experience gained during the design, development, qualification, verification and validation of electronic systems for space/defense/nuclear energy applications could be consciously disseminated to the industry to build the image of India as a specialist in strategic electronics. This brand must be the starting point prior to its foray into the global electronics market. This is similar to the building of Japan as a brand for high quality consumer electronics and automobiles. While China's space programme is perceived to be superior, it has failed to emerge as a global supplier of strategic electronics components in spite of its dominance in ESDM. In fact, counterfeit components and IP theft has left China at an immense disadvantage. The other comparative advantages of India are the talent pool of knowledge workers to build the necessary core competence in this area and a strong IP regime. Building upon this capability is essential as core competence rather than market power has been identified by Prahlad and Hamel (1994) as the basic cornerstone of success in the hypercompetitive world of technology-intensive industries today [3].

The other opportunity is to foster effective alliances with companies holding the Intellectual Property cores that could replenish the supply of obsolete parts through the manufacturing, testing & certification of these parts, which in turn is beneficial to the domestic strategic sector as well. The emergence of India as a global supplier of cost efficient strategic components is expected to generate sufficient interest in the global aerospace market, which is continuously engaged in efforts to reduce the cost without compromising performance.

A re-orientation of the National Electronics Policy to provide sufficient focus on astrategic electronics – centric approach is required, wherein the proposed ecosystem incentivizes faster growth in this sector.

III. GLOBAL LEADERS IN ESDM AND THEIR STRATEGIES

While it is natural to formulate a strategy adopting the best practices from the global leaders in ESDM, it is essential to analyse the effectiveness of these strategies in the Indian environment. It is worthwhile to relook at the strategies adopted by these countries and their effectiveness.

A. China

In the 1990s, when developed countries were looking at outsourcing their manufacturing, China seized the opportunity to position itself as an electronics manufacturing destination. The Government identified semiconductors as an imperative industry and offered extensive support through publicly subsidized bank loans, tax breaks and funding for design centres. Foreign companies doing business in China are generally required to form joint ventures and the entrance by foreign companies to the Chinese market is often determined by how much technology and know-how the Chinese can get from the foreign company [4]. In spite of the low cost and high incentives, most companies indicated that they would not locate their most advanced and critical R & D activities in China due to the inadequate nature of IP protection in the country [4]. This reason along with an illegal industry pushing counterfeit components has been causing alarm in the western nations, who are looking for reliable alternatives providing adequate IP protection and high quality manufacturing. While many start-ups appreciate the agility and comfort of sourcing from China, few of them have begun to realise the need for additional expenditure related to the positioning of quality control personnel, due to the low adoption of stringent quality control measures by many of the Chinese manufacturing firms. The lack of a standard national minimum wage for a long time helped in maintaining a low wage work force. However, rising labour costs have forced companies to open shop in countries like Vietnam. This is the opportunity that needs to be grabbed by India by offering a IP-safe, reliable, cost efficient & quality

conscious manufacturing destination by encouraging the technology diffusion from the highly quality conscious Indian space & defense agencies to Indian EMS companies.

B. Taiwan

Taiwan followed an export-oriented approach and was helped by US technology infusion. In the presence of a hostile neighbour, the Government had to pursue aggressive economic reforms to preserve political legitimacy. Ninety percent of the manufacturing firms in Taiwan are small businesses, which was ably supported by the Taiwanese government to transform the country into a quality conscious knowledge based economy. Taiwan institutionalised the transfer of technology used in the developed countries to the local industry and innovation within the country through the establishment of institutions such as Industrial Technology Research Institute (ITRI) and Hsinchu Science Park [4]. The country has also invested in the human resources, IP creation and a strong microelectronics curriculum through the Si-Soft Project funded by a public-private partnership. The Taiwanese model is worthy of emulation in India but the free flow of strategic technology from the developed nations may not happen. However, the institutionalisation of the transfer of indigenous technologies from the strategic sector to the electronics industry is possible through suitable mechanisms.

C. South Korea

South Korea owes its success to the Government's "Chaebol" model [4] of cherry picking companies and enabling them to become profitable enterprises. Samsung and LG are beneficiaries of this model. Access to technology from USA and Japan in return for cheap labour and a policy of producing cost efficient clones helped the country to establish itself as a global electronics power.

D. Japan

Japan could not sustain its leadership in high quality owing to competition from the China, South Korea and Taiwan and also due to the imposition of constraints upon Japanese manufacturers by USA. In spite of the higher quality consciousness, the country has not occupied the position of a leading supplier of strategic electronic components mainly due to the higher costs. India could offer the same services at a lower cost.

E. Vietnam

Vietnam is positioning itself as a low cost electronics manufacturing destination and is projected to be a tough competitor to the Asian giants but has limited IP availability. The rising labour costs in China and availability of capital from the banks are presenting an opportunity for Vietnam.

F. Israel

Israel is well-known for its semiconductor design centers (fab-less) and R&D facilities. It ranks third after the U.S. and Taiwan and maintains five semiconductor manufacturing plants. There are approximately 150 local companies developing chips in Israel. In spite of the scarcity of domestic raw materials, sources of energy and the restricted size of the local market, Israel overcame its limitations through its focus on innovations and strong support from the Government. The geographical isolation and military focused R & D proved to be an opportunity for the country. The large number of highly qualified migrants from USSR and other European countries till the end of the 90's fuelled the growth of technology in Israel. The presence of high quality institutes such as Technion-Israel Institute of Technology which is one of the best innovation centres of the world can be cited as one of the factors behind the growth of high technology industry and innovation. Israel also focused on the slow evolution of a comprehensive supply chain management system to sustain its semiconductor industry to overcome its scarcity of raw materials.

G. Europe

Europe has a s pecific mechanism for the design, development and fabrication of EEE components for the space programme, wherein the European Space Components Coordination (ESCC) consisting of representative members from the space agencies of the European Union and European electronics industry coordinate the development and qualification of strategic EEE components. ESCC is also pioneering t he European Component Initiative (ECI), that exists to reduce the dependence of Europe's space sector on non-European component suppliers to increase the availability of European EEE-components used in European space missions by identifying critical space technologies and then developing capabilities to manufacture them within Europe. This could be a model to accelerate the availability of strategic EEE components within the country. A Joint Working Group could be formed between the national space and other strategic agencies along with the Indian industry having the necessary skill sets to kick-start an Indian strategic components initiative , thereby moving towards global leadership in cost efficient high reliability EEE components. An Indo-European collaboration to complement each other could also be fostered to jump-start this programme.

IV. THE NEED FOR A STRATEGIC ELECTRONICS FOCUS

Value addition in India's electronics market is extremely limited as most of the activity is performed in the country accounts for last mile assembling [4]. High value addition (HVA) is characterised by high local sourcing, high levels of indigenous design and complete system manufacturing. This is a conscious policy practiced by the strategic government departments, especially space and atomic energy, which has been in the forefront to realize their systems indigenously in spite of technology denial and absence of domestic capabilities. These agencies have a s ystematic policy of technology development and handholding Indian industry especially MSMEs to meet their increasing requirements. Since 2011, HVA products has been exhibiting a steeply declining trend in spite of high domestic consumption, mainly due to the declining markets for the current high value addition products such as CRT TVs and the highly dynamic nature of the electronics market. In 2010, 3D television was being talked up as the next big revolution in home entertainment, but seven

years later, all the major TV manufacturers have discontinued the product. This illustrates the high dynamic nature and the heavy risks associated with the fast changing electronics market. This also calls for a fast adapting scenario in tune with the developments and changing trends, which has been observed to be very difficult to achieve within the country. This necessitates a focus on the not-so-dynamic but high value strategic electronics market with an end-to-end strategy, which has a potential business of US$ 72 billion in the next 10-12 years [5].

India is the seventh largest aerospace and defense (A&D) market globally [5]. Growth in this segment will not only help in meeting the domestic demand for strategic electronics but also enable India to cater to the global supply chain for strategic & reliable electronics, which can indirectly lead to global leadership in the overall electronics market because Indian electronics would then be associated with high quality.

V. SEMICONDUCTOR DESIGN AND MANUFACTURING

In 2012, it was estimated that India accounted for 5.1% of the global semiconductor industry, which is restricted to semiconductor design services [4]. The lack of a semiconductor manufacturing ecosystem in the country was a major handicap until the establishment of the 180nm foundry at Semiconductor Laboratory, Chandigarh. The National Policy on Electronics also seeks to address this gap area by facilitating the setting up of Semiconductor Wafer Fab facilities and its eco-system for design and fabrication of chips and chipcomponents. Two consortia had proposed the setting up of fabs at a total cost of Rs. 60000 Crore [6], of which one has pulled out citing that the project is not commercially viable. The other fab in Gujarat is yet to take off and has an estimated investment of Rs. 25,250 Crore and is reportedly facing challenges in funding [7]. The proposal was to setup technology nodes of 90nm and below in a phased manner to attain 22nm. The Government had proposed to support these projects with interest free loan to be converted to 11 percent equity in these projects [6]. The difficulty in proceeding with the projects even four years after their announcement could be interpreted as lack of confidence among the investors in the proposed strategy. In 2015, Cricket Semiconductor announced the setting up of a $ 1 billion analog semiconductor fab in Madhya Pradesh but two years later, has expressed concerns over the slow progress and infrastructure issues [8]. In the absence of a viable alternative within the country, the electronics industry is viewing the establishment of the SCL fab along with the end-to-end design-to-test capabilities with interest. With the erstwhile Semiconductor Complex Ltd winding down to a R&D laboratory catering to the strategic sector, its utilisation and capacity to address the huge opportunities in the electronics market through industry remains to be seen.

The setbacks faced in the path of setting up of fabs in India in spite of the favourable environment necessitates a re-think in the strategy. Instead of focusing on sub-90nm fabs in phase 1 as proposed, the proposal could aim at setting up 200mm wafer processing fabs using mature technology nodes (180/130/90 nm), which is expected to bring about substantial savings in the required capital investment compared to the higher technology nodes of 65/45/28/22nm that make use of 300mm wafers. While production of memory and logic devices have migrated to 300mm fabs, strong 200mm capacity growth is observed from Discrete/Power, MEMS, and Analog segments in part to the transition from 150mm production to 200mm production. Foundry has also been gaining share, driven by strong demand for Power management IC (PMIC), display driver IC, CMOS image sensor, Microcontrollers, MEMS, and other devices requiring >90nm process technology. These device technologies are cited as key components for many Internet of Things (IoT) applications. The IoT wave is reversing the declining trend in 200mm fabs and the installed capacity in 2018 is expected to increase to 2006 levels [9]. Apart from these new applications, military and space grade devices depend on these matured 180nm or 130nm technology nodes on 200mm wafer size. Notwithstanding the availability of SCL to the private industry in India, it could be fruitful to focus on the setting up of alternate 200mm fabs in the country in the first phase and acquire competence in manufacturing strategic, industrial and commercial components in these technology nodes, with sufficient capacity for automatic test and packaging. The availability of a strong domestic Aerospace & Defense market coupled with the projected demand in the devices for IoT strongly justifies this strategy.

The other challenge is to acquire equipments for the fabs and sustain support for these equipments over a long term. It is equally important to foster alliances with leading equipment manufacturing companies to support these fabs along with technology transfer to the local companies. It is assumed that the equipment manufacturers would be sufficiently interested in a new market for their mature equipments.

VI. CONCLUSION

Considering the aforementioned factors, an Aerospace Electronics System Design and Manufacturing (AESDM) strategy is recommended for achieving the much needed push towards global competitiveness in the electronics market.

(1) Reorient the National Policy on Electronics from an export-oriented approach to a strategic aerospace electronics – centric approach with the dual purpose of meeting the increasing domestic demand from the Aerospace & Defense industry and establishing global competitiveness in high quality electronic systems and leverage the achieved position to foray into the global electronics market.

(2) Actively encourage the setting up of 200mm fabs in the mature 180/130/90nm technology nodes with end-to-end capability along with sustained efforts to indigenously source the required equipment.

(3) Constitute a joint working group between the national agencies of the strategic sectors and the indigenous electronics industry to identify and foster the growth of an end-to-end capability for strategic electronics systems including the high reliability electronic components. The operation of this group could be similar to that of the European Space Components Coordination (ESCC) with

the objective of identifying the constituents of this strategic electronics ecosystem focusing on the domestic demand along with the potential global market.

(4) Kick-start an Indian Strategic Components Initiative in mission mode involving the national space/defense/nuclear agencies, electronics industry and academia with the objective of creating the IP for high reliability and cost efficient product lines with tremendous export potential.

(5) Work towards the building of India as a destination for high reliability and cost efficient products for Aerospace and Defense with a strong IP protection policy to attract potential investors and customers and use this image to transition towards a greater market share in the $2 trillion global electronics market.

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Storage & Handling of Components

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Abstract : This study identifies the key factors required to be considered for Safe Storage & Handling of components .Component Reliability needs to be evaluated for Extended storage to assure component Solderability,MSL
Packing Materials needs to be evaluated for Structural Integrity, ESD properties. Standard packing materialsdesigned for long term storage are effective for more than 5 years

It is important to follow the Guidelines on Storage & Handling strictly for EEE components used in Space Applications to ensure Long Term Quality & Reliability of Satellite Programs This paper outlines the Physical Integrity of Electronic Hardware, PCBs, Wired PCBs & shall prevent corrosion, Diffusion, Contamination, Embrittlement during storage. Any storage beyond five years is defined as Long Term Storage (LTS).This paper outlines the Risk Factors associated with extended storage

Abbreviations used
MSL : Moisture Sensitivity Level
LTS : Long Term Storage
ISRO-PAS-207 : Storage & Handling & Transportation Requirements of Electronic Hardware

BARE PCBS

PCB is the main frame of Hardware which needs to be handled very carefully. The shelf life of the PCBs is critically dependent on the final finish of the bare PCBs.The PCBs shall not beallowed to come in contact with newspaper or any other paper containing sulphur traces

I. STORAGE GUIDELINES

Bare PCBs shall be packed in the vacuum sealed anti-static bags along with Silica gel. Silica gel should be verified periodically .The bag shall contain the details of the board
The following Environmental Conditions need to be maintained

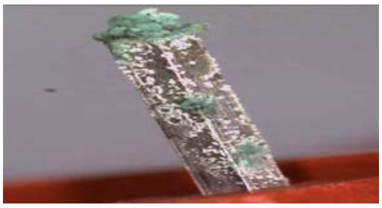
Temperature: 22$\pm$3°C
RH: 55$\pm$5%

II. HANDLING GUIDELINES

Wearing of Gloves during Soldering is desirable& the cards should be handled at the card edges
PCBs shall not be kept in open for long periods.

III. GENERAL FACTORS AFFECTING STORAGE & ERROR PATTERNS

Contamination can occur as a result of gas emissions from surrounding materials
Corrosion occurs if a material reacts with environment .This may result in Loss of shielding, Reduced conductivity of switch & plug in contacts, Leakage from housingCorrosion mechanism may be affected by the following factors like High Air humidity,Temperature,Aerosols,Harmful atmosphere(chlorine gas, nitrogen oxides)
Gas emissions from Sealants, Paints, Varnishesetc.

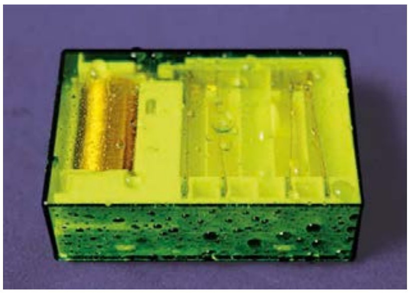


Microclimates present within the devices, sub-assemblies andcomponents can severely impair the operational & storage capabilities

DIFFUSION

Solid state diffusion most commonly associated with Electronics is a physical effect where particles from one substance become mixed with those from another
This phenomenon, which is dependent on time, environmentalcondition & the presence of diffusion particles, can have the following negative effects like Change in solder ability due to ageing mechanism, Change

in contacts layers which affects contact resistance, Impairment of mechanical /Thermal properties due to altered moisture content,
UV light (wavelength range 100nm to 400nm) is a form of EM Radiation which is not visible to human eye. It is generally advisable to use light proof & UV
Proof packaging for long term storage of electronic components



Example of Condensation of a Relay

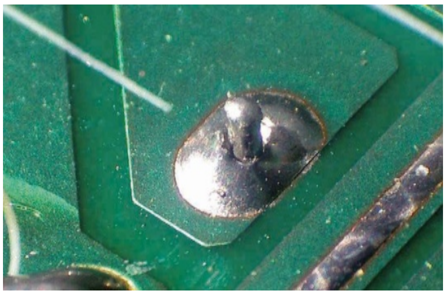
EMBRITTLEMENT

This is loss of Ductility of a material.The use of brittle material increases the likelihood of component being mechanically damaged or destroyed during assembly

Solderability,Wetting,Dewetting,non-wetting

Three distinct soldering mechanisms occur depending upon the extent to which the solder is able to form a stable bond on substrates, wetting,dewetting& non-wetting
Wetting describes the ability of a molten solder to form an intermetallic bond with the base metal, whilst non-wetting is the inability of molten solder to form a metallic bond with the basis metal
Dewetting describes a condition that can arise as a defect after actual wetting
The appearance of wetting, dewetting& non-wetting can easily be distinguished by visual inspection
Wetting forms a largely uninterrupted solder joint characterized by the contact angle at the respective joint or interface (soldered surface)
De wetting occurs when the solder recedes from zones that were initially wet leaving irregularly shaped mounds of solder that are separated by non-solder ableareas, which cannot be wetted

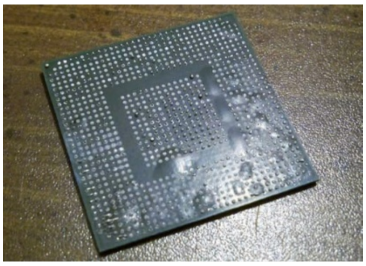
Example of dewetting



Example of non-wetting

Popcorn Effect

Popcorn Effect can occur when components are stored incorrectly, e.g., if moisture-sensitive electronic components are stored outside the moisture proof packaging for too long



Example of BGA Package destroyed by the Popcorn effect & moisture in the housing

Electronic Components

All Flight components should be stored in Desiccators in controlled humidity environment. Use of Polythene Plastic Containers is prohibited.Anti-static trays & covers shall be used for Storage of components

Temperature: 22$\pm$3°C
Relative Humidity: 50_60%
ESD Protective measures shall be followed during handling & storage

HANDLING OF STATIC CHARGE SENSITIVE DEVICES

Static Charge sensitive devices are liable for damage due to improper handling .The most common damage is the Gate Rupture caused by static discharges. This can occur when a device is picked up by its case & handler’s bodycapacitance is discharged to ground through the seriesarrangement of bulk to channel & channel to gate capacitance of the device
Moisture can damage the components (eg Popcorn Effect/Corrosion)

FEATURES OF PASSIVE COMPONENTS

It is always advisable to clarify with the manufacturer whether any specific considerations relating to the technology or function should be taken into account before undertaking long term storage

Handling of Static Charge Sensitive devices

All static charge sensitive devices shall be stored in Antistatic conductive bags. Containers containing ESD sensitive devices shall be labeled as "Sensitive to Static Electric Charges". While soldering CMOS ICs,it is advisable to place a Grounding Clip across the Connector fingers to ground.CMOS devices shall be handled by either ceramic body or the metal can & their leads shall not be touched. Flux residue after assembly shall be cleaned with the approved solvent

The accumulation of Solder Flux between adjacent pins shall be avoided which may cause Leakage Path

FOREIGN OBJECT DAMAGE

FOD :Any damage attributed to a foreign object that can be expressed in physical or economical terms which may or may not degrade the product's required safety and/or performance characteristics

FO: A substance or article alien to the product that could potentially cause FOD

5S : A method for improving workplace using visual controls (i.e., Sort,Straighten,Shine, Standardize, Sustain) resulting in positive i mpact on FODprevention, productivity,& Environmental & Health Safety(E&HS)

The minimum requirements of a FOD Prevention Program for all products/services suppliers shall include: Causes& Effects of FOD, Protection of Product, General Housekeeping program & formal 5S Practices, Tool Control/Accountability, Unrestricted Hardware control, ConsumableControl,Accountability

HANDLING DURING PCB ASSEMBLY

PCB shall be kept over a sponge or rubber until wiring is completed After a day's work, the solder joints & adjacent areas shall be cleaned with IPA, dried The partly assembled PCBs shall be stored in ante-static bag in presence of Silica Gel Operators /Inspectors shall wear overcoats made of cotton. Wearing of Gloves during soldering is desirable PCB assembly shall be lifted using PCB edges only Connectors & wire bunch shall not be permitted to hang which will induce stress on wires& solder joints Approved tools shall be used for lead bending & component mounting. Tinned component shall not be allowed to lie open for extended period oftime. Foodor beverages shall not be taken inside. Operators shall wear leather shoes during assembly

STORING WIRED PCBS

Partially wired cards shall be stored vertically. Parts in wired assembly should not be damaged mechanically. Care shall be taken to avoid contamination due to finger prints. Special care required for boards having Charge Sensitive devices Input & Outputs terminals shall be shorted b y means of shorted connectors. While handling PCBs Care to be taken to remove them smoothly. For long duration Storage requirements, wired PCBs should be stored in closed containers

STORAGE CONTROLS

Facilities, as necessary, provide isolation/protection to material pending use of shipment

Periodic assessment of the condition of material in stock. Firstin Firstout issuance of material subject to degradation. Shelf life control applied to processing ofmaterial, as required

HANDLING OF FLIGHT PACKAGES

All fabricated packages shall be kept individually in suitable ESD safe containers. Racks in which packages are stored shall be properly grounded. Packages shall not hit any surface or fall down. Stacking of packages one over the other shall be avoided. Packages shall not come into abrasion against any hard surface

HANDLING OF MECHANICAL CHASSIS

Chassis should be kept inside a polythene cover to prevent environmental attacks. Formation of scratches shall be prevented on chassis duringassembly. Enough packing materials shall be provided to isolate chassis from shock. Allowed torque shall be applied to screws Screws should be t orqued diagonally during assembly. Heavy material shall not be kept on chassis Chassis shall not be kept in uncontrolled atmosphere Uneven pressure shall not be applied

ESD PROTECTIVE MEASURES

The work table shall be provided with a static dissipative top The working table shall be provided with a co ver of cotton Theoperators shall wear conductive shoes A grounded wrist strap shall be worn while handling component. All Assembly tools should be grounded Static charges generated may be de-ionized with De-Ionizer. Where applicable,institute adequate procedures & controls to prevent damage to electronic equipment and components which are sensitive to ESD. Provisions shall be made for Protection of Electronic & Electrical material which is sensitive to ESD ESD control requirements apply where equipment containing ESD sensitive parts are used during the process of fabrication, calibration, testing or packaging of end item

RISK ASSESSMENT

The devices Functionality & Parametric performance after extended periods of Shelf Storage is measured in terms of FIT(Failure In Time or Failure Rate of devices (one FIT equal to one Failure per billion hours of storage).Devices stored for extended periods may exhibit corrosion of bond pads(Package Qualifications include Autoclave Tests to

evaluate the effect of Moisture on Die Metallization (Galvanic Corrosion)(Autoclave Test is a Environmental test which measures Device resistance to Moisture penetration & resultant effects of Galvanic Corrosion. Packing Materials: Risks The static dissipative properties of Tubes or Tape and Reel may degrade over tine resulting in potential ESD damage to devices.Tribocharge Testing is to be conducted on Conductive & Dissipative tubes Storage bags may leak ,allow moisture to enter and cause problems to MSL.Extended storage bag manufacturer's data supports 5 year storage capability. Independent validation of Water Vapor Transmission Ratio(WVTR) for extended storage bags(5 years) is to be conducted in a laboratory

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REFERENCE **:**

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United Technologies ; Aerospace Supplier Quality Requirements: ASQR: 15.1 Rev
My Industry experience & thoughts

Device Manufacturing Integration System (DMIS)

Tool for Best Known Practices in VLSI Fab

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Abstract : VLSI fabrication process is one of the world's most complex manufacturing process carried out under highly stringent parameters of man, machine & environment. Generally, a 'Wafer Lot' of 25 wafers goes through fabrication process of Lithography; Ion Implantation; Etching; Metallization; Diffusion and CMP (Chemical Mechanical Planarization) under stringent physical and chemical conditions. Because the VLSIs are manufactured by successively building layers, each of which is similar in many respects, any given 'Wafer Lot' passes through the same kind of equipment several times. Typically, a 'Wafer Lot' goes through about 500 steps in the process of fabrication. The complexity of flows and varying equipment conditions makes the overall system highly complex to control and monitor manually.

Semi-Conductor Laboratory (SCL) 'Wafer Fabrication' facilities are based on 180 nm CMOS technology on 8" Wafer Fab line as per international standards and 6" Wafer Fab line with CMOS/MEMS Process capability. Dealing with such finer geometries, process yield is not only dependent on clean room conditions, but there exist probabilities of Wafer contamination from 'VLSI Process' themselves. Process Yield, therefore is directly related to VLSI Fab Process Equipment, Wafer Handling, Wafer Environment, Metrology and above all strict adherence to Best Manufacturing Practices. Moreover, VLSI Manufacturing being a paperless operation performed in class 1/10/100 clean room conditions where no conventional "Run Cards" are used, it is highly desirable to use a "Software Solution" to control and monitor the Fabrication Process such that best practices are used.

For commercial VLSI Fabs running in the production mode where processes are well frozen, there are "Off the Shelf- Readymade Solutions" available. However, SCL Fab is an R&D Fab dealing with lot of experimental runs. Therefore, a dedicated in-house solution has been developed.

SCL, in-house developed DMIS-Device Manufacturing Integration System is a tailor made solution for SCL Wafer Fab such that Best VLSI Manufacturing Practices are followed.

Key Words: Wafer, CMOS, VLSI Process, Silicon, Clean Room, Database,

I. INTRODUCTION

SCL's earlier 6" Fab had used standard CIM tool named PROMIS in the past for planning, monitoring and controlling wafer fabrication operations. Some of the related objectives were to minimize use of paper inside the clean room environment, reduce manufacturing cycle time, planning, scheduling, tracking of lots, managing equipment's time, usage and generating related documentation.

However, in using PROMIS, we observed that procured standard software has some intrinsic limitations like:

- Cost of “Manufacturing Integrated System” is exorbitantly high.
- Annual Maintenance Cost is generally 10 to 12 % of the cost
- Customization is very tricky
- Low Extendibility
- Restricted access to the underlying Database.
- Incompatibility to third party application.
- Bound to Specific H/W
- Underutilized due to lack of proper training and knowledge.
- Cannot be upgraded with upgraded Platform.

Above all, Standard software solution like PROMIS is primarily designed for commercial VLSI Fabs with multiple production lines and bulk wafer processing.

SCL’s upgraded Wafer Fabrication (Fab) Facility to 0.18µm CMOS technology on 8” Wafer Fab Line is primarily an R&D facility. Such R&D facilities processes ASICs that requires regular customization of Wafer Run Cards. With continuously changing requirements, customization of the software code is required frequently. With this background, it was thought prudent to develop in-house solution incorporating best known practices which will always remain dynamic and allow the stakeholders and users to customize as and when required.

It is with this background that DMIS-Device Manufacturing Integration System was developed in-house at SCL. This is a web based application using Windows Server 2008 (Standard Edition) as server operating system and uses Microsoft SQL Server 2008 (Standard Edition) as database and Microsoft Visual Studio 2008 (Professional Edition) as development environment.

DMIS integrates all manufacturing functions into a database. The database stores all data related to production and product development, and helps to track lots, record data and control production in real time.

Modules of DMIS are:

1. Process Modeling
2. Equipment Management
3. Lot Processing
4. Administrative Module
5. Material Management
6. Reports Generation

II. PROCESS MODELING

The whole Process flow is categorized into hierarchical granules, starting from the very core where lies the basic “operation” which is performed on a tool using a recipe. Moving next to the “Layer” which is basically an activity; set and sequence of operations collected together forms a Layer. Next comes the “Module”, it is a masking level formed by set and sequence of various Layers. Top of the hierarchy lays the “Process”, which is group of Modules. (Every time a process is chosen in DMIS to fabricate a device.)
Every single entity here starting from Operation till Process needs to be modeled in DMIS with specific IDs and associated parameters.

Tools and recipes are also bound with individual operations.

III. EQUIPMENT MANAGEMENT

Every tool has been assigned an identification code comprising 2 letters for the tool name abbreviation, 2 letters for Area (location of the tool) and a number for its quantity. These Tools were divided basically into two: Process tools and metrology tools. It was pointed out by the user that metrology

tools (since they were single of each type) need to be shared among all the work areas. Thus these tools are accessed by all the work areas and the type is specified as "Shared". Another issue raised by users was that the tools are having multiple chambers and are identified for multiple capabilities. A major concern here was to deal with combination, sequence, alternatives of these capabilities while performing operations during lot run. In addition to this at the time of tool down DMIS need to identify and differentiate between capability down or full tool down or sequence of

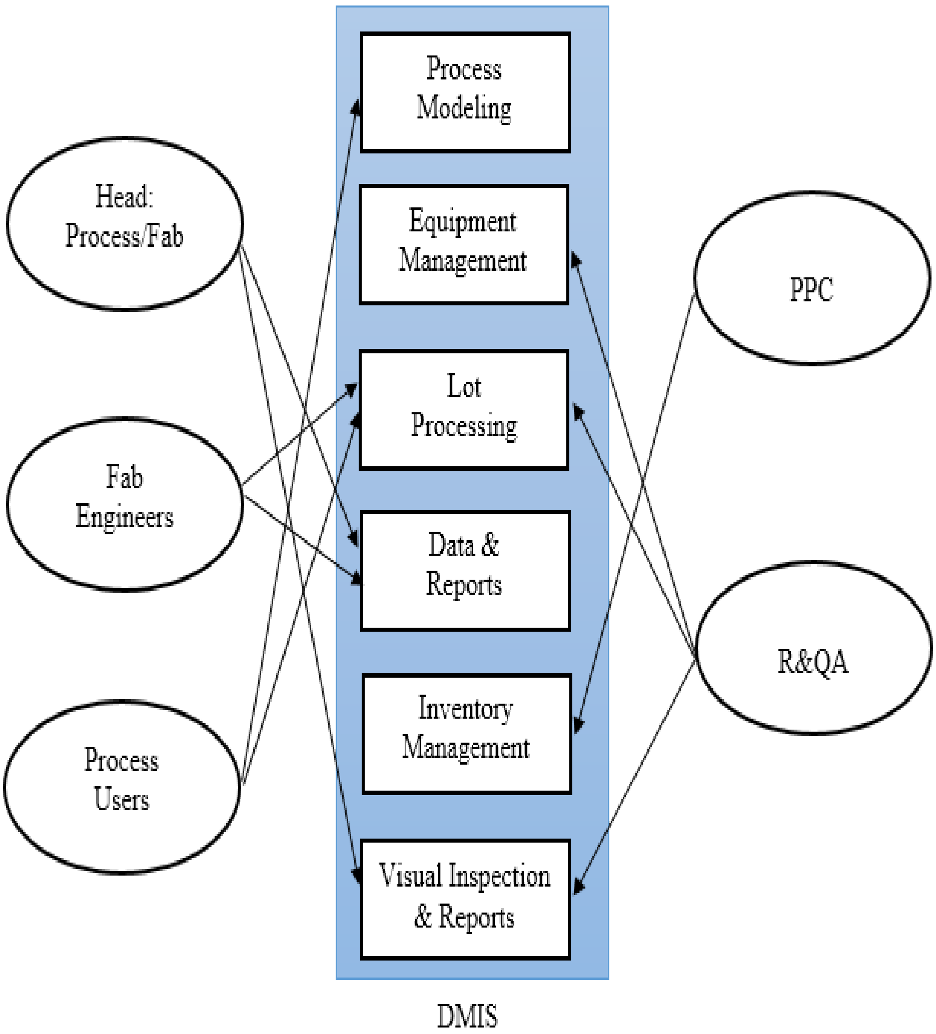


Figure1: Different actor activities and access through the system and its modules.

capabilities down. DMIS gave a solution to this issue by identifying each capability as an independent tool, maintaining its hierarchy in the sequence. Though it was a bit cumbersome task while tool modeling it was gladly accepted by the user as it could give solution to many problems which may arise during lot run.

Other features like Tool Qualification, Maintenance, Recipes, and Utilities hooked to the tool, Auto tool down for QC and Maintenance, Auto alarms in case of Non-Conformance and deviations were taken care in Tool Management Module

1. Lot Processing

Basic activity here which happens frequently is "Track In" and "Track Out". These two pages are accessed every time a lot comes to an area for a specific operation on a certain tool.

Operator logs-in and tracks in / tracks out a lot first in DMIS and then physically on Tool. All the Data Collection Operations happen on these two pages exclusively.

Initially a lot start take place where in one has to choose a device for lot run, types and quantity of wafers, Lot engineer etc. Then continuously track in track out takes place. Lot specific changes can be

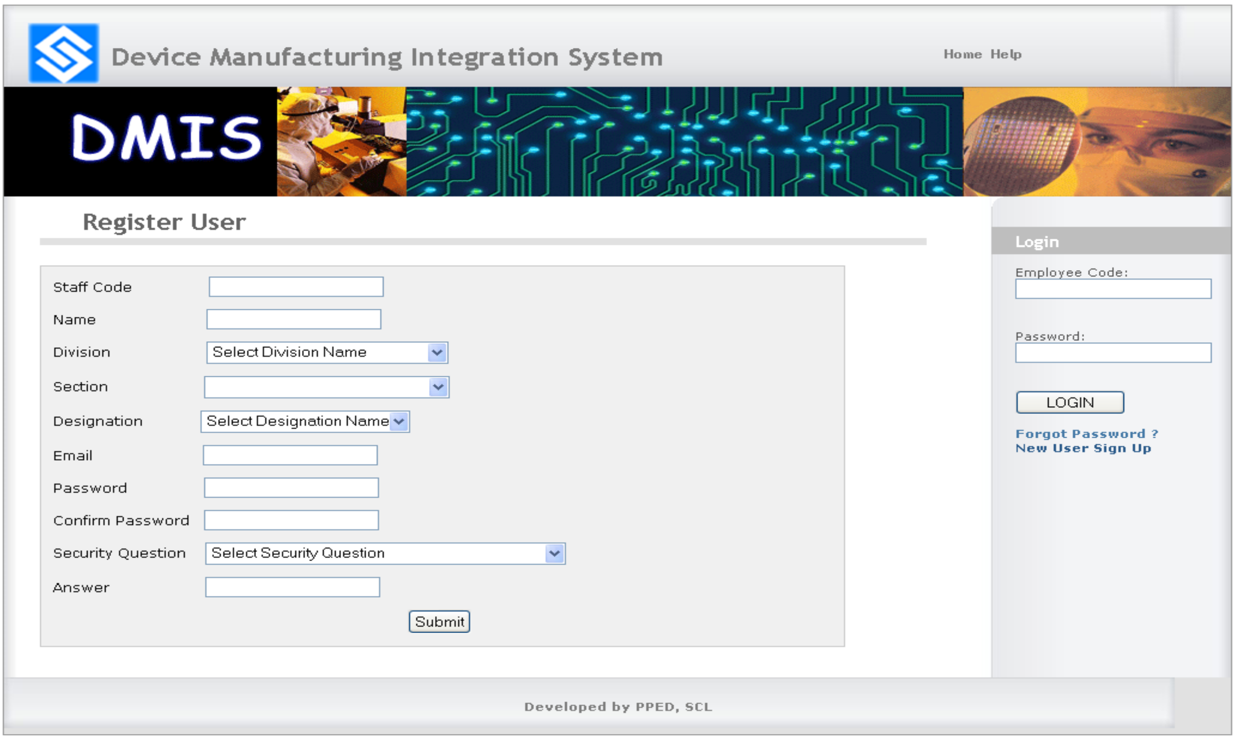
done at any point of time according to requirement, these changes include inserting an operation, deleting or editing.

Splitting a lot is a basic requirement during a lot run especially during the new process establishment. Thus here also it w as a major requirement raised by user. DMIS provides Lot Split into two lots at a time, subsequently point of lot join can be specified or later during lot run; forced join can also be accomplished. DMIS further provides a facility for lot specific changes both in Parent lot and child lot.

Rework, Lot hold, Release hold and Skip an Operation are some other main features.

2. Administration Module

This whole system is Privilege based where in approved and authorized person is given privilege to access a particular feature in DMIS. It is a log-in based system and every user activity, page accessed or query executed is traced and logged; not only this, the hardware information as IP address, MAC address are also logged every time a user logs in.



In case of Non conformances or deviation lot is pushed to Auto hold.

3. Material Management

On floor material (wafers, chemicals and spares) quantity and consumption pattern is dealt in this module.

4. Reports

Numerous reports are being generated by DMIS which comprises real time data. Graphs and comparison charts are also included for analysis purpose. Data mining and archiving has been given an extra attention so as to make DMIS data information extensive.

IV. USERS REQUIREMENTS FROM DMIS FAB HEAD/ PTDD HEAD:

- Views Lot performance. RUN CARD.
- Keeps Track of Work In progress.

- Requires Data for Calculation of yield.
- Requires all measurement data for decision making.
- Views Shift Reports.

Fabrication Engineers/Technicians:

- Performs Track-In/Track-Out.
- Enters measurement and environmental data.
- Viewing collected data in graphical and tabular format.
- Compares collected data, studies Lot-Lot variation and Wafer-Wafer variation

Production Planning & Control:

- On floor material management.
- Keeping track of issued material
- Chemical/consumables consumption pattern
- Generating comparative reports.

Reliability & Quality Assurance:

- Audit of Fab Tools.
- Audit of Process Model
- Visual & Inspection Reports.

V. DMIS INTERFACE

Salient Features:

- The platform enables fully transparent continuous tracking, controlling, and online reporting of all open issues to the involved parties.
- DMIS performs checks on resources and inform other systems about the progress of production processes.
- Collection of production data: This includes collection, storage and exchange of process data, equipment status, and material lot information and production logs in either a form of data history or relational database.
- Production performance analysis: Create useful information out of the raw collected data about the current status of production, like Work In Progress (WIP) overviews, and the production performance of the past period like the Overall Equipment Effectiveness or any other Performance indicator.
- Production Track & trace: Registration and retrieval of related information in order to present a complete history of lots.
- A statistical analysis is also attempted. It provides the basic calculation of Min, Max, Sigma, 3Sigma. Wafer to comparison graph and Lot-to-Lot variation graphs are also included.
- Data collection Operations are to be automated using implementation of SEMI SECS protocol.

VI. CONCLUSION

DMIS is a complete in-house solution that is playing a vital role in Wafer Fabrication at SCL. The solution has evolved alongside the setting up of Fab and with users gaining better insight in the VLSI operations, more features are being added as and when required. This was not feasible with any other standard software available from market.

ACKNOWLEDGEMENT

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Component Obsolescence Risk Analysis and Mitigation Strategies for I&C Systems of Nuclear Power Plant

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***Abstract*—Rapid changes in technology and uneconomical market demand are two major causes of component obsolescence. The risk of component obsolescence has impacted the reliability, efficiency and operation & maintenance cost of Instrumentation and control (I&C) systems for Nuclear Power Plant. As plant I&C system ages and component obsoletes, challenges increases to enhance the I&C system capability to improve plant performance, is also profound. The I&C Program develops and transfers advanced technologies to enable existing and new nuclear plants to tap into functionality and capabilities important in maintaining safe operation, while managing I&C obsolescence and achieving higher levels of equipment reliability and plant productivity. In long-lifecycle I&C systems for Nuclear Power Plant, obsolescence has become a major problem as it prevents the maintenance of the system. The component obsolescence risk analysis for the Bill-of-Materials (BoM) of I&C systems is a daunting task in order to manage obsolescence proactively and cost-effectively. Therefore, it is necessary do risk analysis for the existing system and develop a mitigation strategy for the future obsolescence of components.**

This paper focuses on component obsolescence risk analysis taking into account issues like multiple source of manufacturing, uses in industry verticals, stock availability and operational impact criticality for each of component in the BoM and suggests some proactive mitigation strategies for very high risk components. However, for low risk components it is more cost effective to deal with reactively. This process has been validated using case studies with existing I&C system for Nuclear Power Plant.

***Index Terms*—Component Obsolescence; I&C System; Bill-of-Materials; Planned & Unplanned; Proactive & Reactive;**

I. INTRODUCTION

A 500 MWe Prototype Fast Breeder Reactor (PFBR) is first of its kind in India. Distributed Digital Control System (DDCS) is the design architecture for automating a geographically distributed plant with large number of input/output signals and control loops. DDCS facilitates in locating the Data Acquisition and Control Systems as close to the sensors and Final Control Elements (FCE) as possible, thereby saves lot of cabling and the associated electromagnetic interference problems. De-centralization also helps in modular development of the subsystems and in maintenance. The constituents of DDCS are the sub-systems like VME bus based RTC systems, Standalone Remote Terminal Units and Electrical PLC system, Process computer, Display Stations and the entire networking.

The entire plant is modularly designed with more than 100 subsystems. Subsystems are classified as Safety Class -1, Safety Class-2 and Non-nuclear Safety Systems. Subsystems are geographically located at different buildings namely – Reactor Containment Building, Control Building, Steam Generator Building, Fuel Building and Turbine Building. The purview of DDCS is to send configuration data and soft inputs to I&C sub-systems belonging to SC2 & NNS category, receive data from all I&C sub-systems and display the information in various display formats in display stations located in control room and respective local control centers where the I&C sub-systems are located, store of all plant data for storage & historical data logging purpose and control of pumps, blowers, heaters, valves etc. using soft commands from display stations.

According to Rajeev, Peter and Michael [1], a component becomes obsolete when it is no longer available in the market due to technological obsolescence and diminishing market demand. Obsolescence can be defined as “the loss or impending loss of original manufacturers of items or suppliers of items or raw materials”. Michael and Diganta [2] made a distinction between the ‘obsolescence’ and ‘discontinuance’ concepts. They explained that discontinuance, which takes place when the manufacturer stops the production of a component, occurs at a part number or manufacturer specific level, while obsolescence occurs at a technology level. In this paper we refer the term obsolescence which includes discontinuance in the production of a component if there are no other manufacturers for that specific component. The obsolescence issues can arise not only during operation stage but at any stage of the whole life-cycle of the system. In fact, obsolescence issues may arise even before the end of the implementation phase. This suggests that obsolescence needs to be managed since early stages of the project, especially at the design stage, where several strategies to mitigate the obsolescence risk should be considered.

II. OVERVIEW OF DDCS ARCHITECTURE

All embedded systems located in different Local Control Centers (LCCs) transmit the data and messages to Control Room through a dedicated data highway. Data highways

known as plant backbone are dual Local Area Networks (LANs) with fiber optic cable as the media. Hence, plant backbone has the entire plant parameter information of connected systems. Process Computer receives plant information from the plant backbone. The process computer does all the processing, update the plant parameter database and store the data. The graphic display stations on the operator console & panels, shift charge Engineer's desk and Large Video Display receive the data from these process computers and display the plant information in different display formats like mimic diagrams, bar graphs, soft alarm panel, etc. with its associated units. Supervisory control for giving set points to remote PID controllers running on embedded systems is sent from display station. The architecture of DDCS is shown in Figure 1.

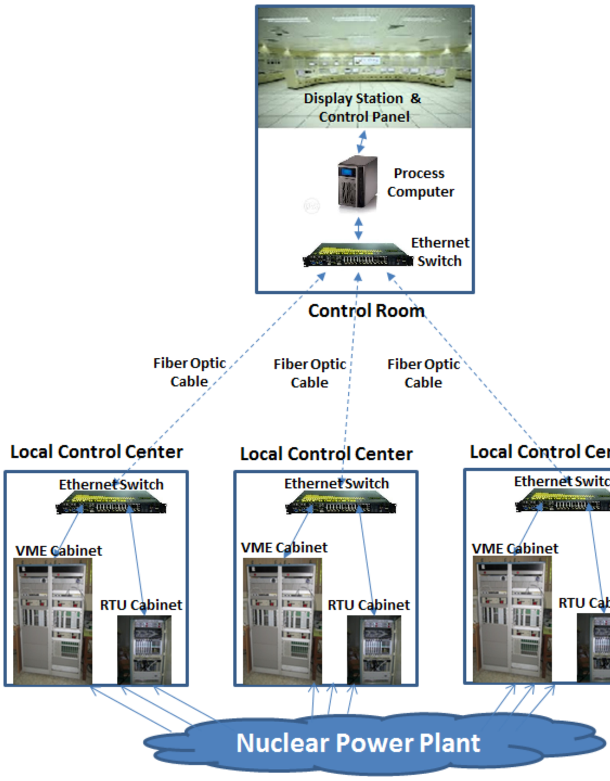

Figure 1: Architecture of Distributed Digital Control Systems

DDCS acts as an information network and serves as 'nervous system' of the entire plant. It senses basic physical parameters, monitors performance, integrates information and controls final control elements for smooth operation of the plant as necessary. It facilitates remote controlling of plant parameter from remote Control Room. It also aids the operator with appropriate information to take appropriate actions. DDCS comprises of redundant display stations at the top layer, process computers in the middle layer and embedded computer subsystems that interface with plant sensors and final control elements at the bottom layer. Ethernet links and switches connect the different layers. DDCS as a whole serves as an interface between the operator and the plant.

The principle of layered modular design is adopted for entire DDCS architecture. At the same time, embedded systems at the bottom layer also adopt layered architecture while designing VME and RTU systems. This approach is quite simple and in most cases logical, where the resultant product is an obsolescence mitigation scheme. The design of DDCS is split into three layers such as embedded layer, communication layer and HMI layer.

The embedded systems are developed as per Atomic Energy Regulatory Board (AERB) safety guidelines D-10 for Safety Critical System, D-20 for Safety Related Systems and D-25 for computer based systems [3]. The hardware and software for these systems are designed and developed on the criteria such as simplicity in design based on proven principles, single failure criterion, fault detection & notification, periodic s urveillance, testability and failsafe capability [4]. The embedded system designs are verified in each stage to achieve high reliability [5] [6]. Two types of embedded system design architectures are followed to cater 30,000 plant signals. One system is based on VME bus based RTC system and the other system is designed based on the principle of single board computer sitting on custom built backplane called Remote Terminal Unit (RTU). Important plant safety parameters are handled by VME bus based system in different architectures like dual hot-standby and 2oo3 voting logic. Whereas signals related to non-safety parameters are handles by RTU boards.

The VME RTC system is mounted in 42U high dual cabinet along with power supply and Ethernet switch as shown in Figure 2. Whereas RTU cards are mounted in 27U cabinet in a custom built backplane along with power supply and Ethernet switch as shown in Figure 3.

Figure 2: VME System

Figure 3: RTU System

The real time embedded system consists of Versa Modula Europa (VME) bus based CPU card, Input/output cards, back planes and power supply modules. MC 68020 processor is chosen for CPU card by considering various facts such as floating point

processor support, no bug list, availability in second source, industrial grade and long support period. In the present system architecture, the maximum number of Input/output (I/O) signals handled by an embedded system is 450. Hence, a backplane bus becomes necessary to communicate between the CPU and I/O boards. This guides for the construction of embedded system in modular type for easy maintainability, which also helps to reduce Mean Time to Repair (MTTR). Industry grade VME bus has been chosen as the backplane bus due to the facts that it is simple, processor independent, open bus, 21 slots for I/Os, flexible address and data bus widths, multi-master support, matured and proven operation in military, aerospace and Industrial control applications and supported by IEEE/ANSI-VITA standard. The in-house designed and qualified VME bus based CPU, Analog input, Digital input, Analog output, Relay output and Synchro-to-Digital Converter cards are shown in Figure 4.

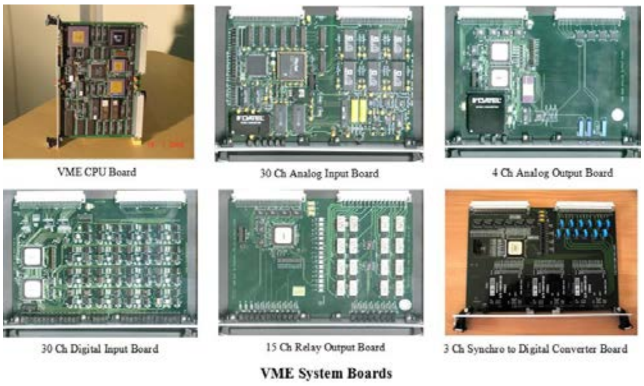

Figure 4: VME System Boards

Similarly, RTU card are designed for field deployment and installed in several LCCs situated near to field sensors to acquire analog/digital signals from sensors; processes and generate control outputs for final control elements. These systems send data to process computer, local display stations kept in the same LCC or other LCC and to various other peer level DACs on LAN. The RTU is a general purpose 8051 micro-controller based single board data acquisition and control card which can be easily deployed in the field environment. It can sustain elevated ambient temperature, humidity and dust. It is based on Atmel 89C51RD2 flash micro-controller. RTU card has provisions like; on-board 32KB NV SRAM with battery backup, RTC, programmable WDT, power ON and manual reset, serial port, two 10/100mbps Ethernet ports and I/O channels depending on applications.

The in-house designed and qualified RTU system boards are Analog input, Digital input, Relay output, Thermocouple input and Leak Detector input cards are shown in Figure 5.

RTU cards are designed for long-term sustainment and are usually composed of low volume electronic components such as memory module, watchdog timer, Ethernet controller.

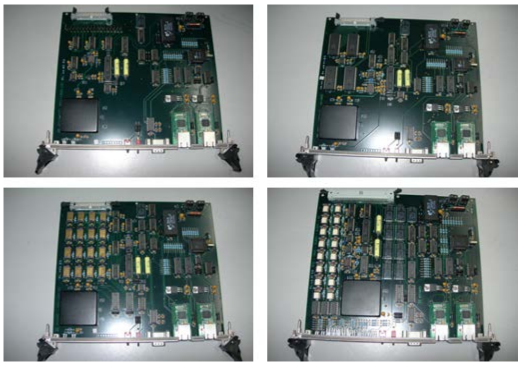

Figure 5: Different types of RTU System Boards

The life-cycle of these systems is expected to be 40 years or even more. One of the main problems these systems will face during their lifetime is component obsolescence.

III. LIFE CYCLE MODEL OF I&C SYSTEM

Components of I&C system can be broadly classified into Replaceable and Non-Replaceable. Replaceable items include sensors, transmitters, instrument cables, power supplies, embedded systems, switches, process computer and display station whereas non-replaceable items include mechanical components of the reactor. The design life of a N PP is typically 40 years. This may be extended by 10 to 20 years provided the components of the plant can be upgraded by managing obsolescence and aging.

All industrial products normally have some sort of life cycle model defining if the product is in active operation state or not. A typical lifecycle model of I&C system in NPP is as shown Figure 6.

Figure 6: Life Cycle Model of I&C systems for NPP

Development

During this phase new systems are designed keeping stringent requirements in mind adhering to regulatory guidelines. Technological assessment should be done at this stage for future refurbishment or replacement.

Deployment

During this phase developed systems are deployed in the field for its intended use and field data are collected for design refreshment prediction. System is also maintained during this period for long life support. Depending on field return and component failure information, life time buy can also be initiated at this stage.

Refurbishment

At this stage, decision like design refreshment is taken and new systems are designed for system up gradation without affecting major overhaul in the design architecture/philosophy.

Replacement

It is possible to continue using technology that is obsolete but the risk with doing this should be identified, considering issues like available spare parts, competence and reliability. At this stage where there is no support from major component manufacturer and the plant demands new additional features in the I&C systems, it is better to go for major replacement in order to enhance safety, security, reliability and maintenance.

IV. OBSOLESCENCE RISK ANALYSIS

Obsolescence risk can be categorized in two ways: Planned and Unplanned [7] [8]. Planned obsolescence is designed into the asset by the developer whereas unplanned obsolescence refers to a l ack of support, spare parts and service due to changes in the technology and functionality, as well as evolving plant safety needs. Many nuclear power plants struggle with obsolescence brought about by the latter.

It is important for the plant asset manager to monitor life-cycle stages of all equipment, collect information to perform a comprehensive audit of the installed I&C system and plan for risk management and mitigation. Hence, it is prudent to have obsolescence policy covering all aspects of assessing and managing risk in nuclear power plant. Such a policy when complemented by scheduled audits can better support maintenance decision, including allocation of spares for legacy equipment and design refreshment.

Unplanned obsolescence must be properly assessed to ensure the continuity of plant operations through proactive obsolescence policies or alleviated completely with alternative solutions.

Analyzing Risk

It is important to perform an objective assessment of obsolescence risk on all components of I&C systems. In our risk assessment, we include the following factors.

The first step is to identify critical assets of entire plant. A typical plant has hundreds of assets comprising instruments and bespoke systems, control systems, standard and configurable software packages. The asset hierarchy at the site level for a typical I&C system is shown in Figure 7. Risk assessment can be divided into two parts i.e., likelihood and impact [9]. Likelihood is a function of obsolescence and reliability whereas impact is a f unction of operational and revenue. Obsolescence of component occurs due to functional, technological and market demand [10]. Obsolescence of assets

Figure 7: Framing Asset Risk Analysis

can also happen due to lack of skilled manpower and inventory status. Reliability of asset plays a major role as it determines the design refreshment plan. Asset reliability and supplier reliability are two major factors while considering likelihood of risk assessment [11]. In nuclear power plant, risk of obsolescence also impacts plant operation and loss of revenue. F or example, "average downtime" can be defined as the time an asset is unavailable. Approximating downtime takes into account any possible redundancy and workarounds in the event of a b reakdown. "Revenue impact" is determined by gauging the unavailability of an asset and average demand.

In assessing "obsolescence likelihood," suppliers play a crucial role. "In-house capability" refers to the ability of an organization to manage a system, which depends heavily on tools, skill sets, and the availability of back-ups and spares/stocks inside the plant site. "Reliability likelihood" typically refers to both asset reliability and the reliability of the supplier [12] [13] [14].

Both asset and system data must be gathered and taken into risk analysis. Normally, details such as vendor information, system part number, technical features, installation dates, software versions, availability of application back-up, etc., reside with maintenance and engineering teams. Interaction with the supplier base is needed to gather information on their future manufacturing plans, as well as spare and repair support plans.

Obsolescence Evaluation

To manage the complete life cycle of I&C system components, obsolescence evaluation should be given more proactive attention as the life cycle moves through different phases towards replacement. As a p art of a development of an Obsolescence Management Plan, it is important to have a complete overview of the assets of I&C system. The

following steps should be followed to develop the Obsolescence Status Overview.

Step 1: Create Component Inventory

As-built document is an essential element of the obsolescence management. For each obsolescence plan, the first step is to create an inventory of I&C system equipment component details. This inventory provides details of the obsolescence status of each element in the list. A sample I&C system equipment component details has been included as shown in Table 1.

Table 1: Component Inventory

Equipment	Equipment Source	Year of development	Current Status	Alternate Source	Risk: Component	Risk: Competence	Comments / Strategy Summary
Hardware							
VME RTC	In-house	2012		Yes	Me	Hi	
RTU	In-house	2011		Yes	Me	Hi	
Network Switches	COTS	2013		Yes	NA	NA	
Power Supply	COTS	2013		Yes	NA	NA	
Process Computer	COTS	2014		Yes	NA	NA	
Display Station	COTS	2014		Yes	NA	NA	
Software							
Compiler for VME RTC	COTS	2008		Yes	NA	NA	
Compiler for RTU	COTS	2008		Yes	NA	NA	
Application Software	In-house	2013		NA	NA	Hi	
Process Computer OS	Open Source	2014		Yes	NA	Hi	
Database Software	Open Source	2014		Yes	NA	Hi	
Display Station OS	Open Source	2014		NA	NA	Hi	
HMI Software	Open Source	2014		NA	NA	Hi	

The current status of component inventory is coded with following colors during evaluation.

- Active
- After sales support
- Obsolete and no supplier support
- Status unknown at this date

Step 2: Risk Assessment of Component Inventory

This can be assessed as two different scenarios taking component availability vs. failure rate as shown in Table 2 and design competence vs. complexity as shown in Table 3. The results of risk analysis (High, Medium or Low) should be documented into the component inventory, clearly indicating the status of each component in appropriate color coding. A typical risk assessment of RTU card is shown in Table 4. RTU board uses discrete components along with hardcore microcontroller from a specific vendor. Components like resistors, capacitors and inductors are not taken into risk assessment as it can be replaced reactively during any stage of card life cycle.

Table 2: Component Availability vs. Failure Rate

Failure Rate \ Availability	High	Medium	Low
Low	Low Risk	Low Risk	Medium Risk
Medium	Low Risk	Medium Risk	High Risk
High	Medium Risk	High Risk	Very High Risk

Table 3: Design Competence vs. Complexity

Complexity \ Competence	High	Medium	Low
Low	Low Risk	Low Risk	Medium Risk
Medium	Low Risk	Medium Risk	High Risk
High	Medium Risk	High Risk	Very High Risk

Table 4: Component risk assessment of RTU card

Component Description	Manufacturer	Part Number / Model	Package	Qty	Status	Risk Rank	Risk Level	Technology	Alternate Source	Color Code
Microcontroller	ATMEL	AT89C51RD2-SLSIM	PLCC	1	Obsolete	8.85	Danger	CMOS	Y	
Microcontroller Socket	ASSMANN	A-CCS44-G-R	THRO' HOLE	1	LTB	8.54	Danger		Y	
Ethernet Module	WIZNET	NM7010B+	DIP	2	Active	NA		HYBRID	N	
RTC, Watchdog Timer, Memory	MAXIM	DS1554-70IND	DIP	1	Obsolete	8.83	Danger	CMOS	N	
Reset Chip	MAXIM	DS1232N	DIP	1	Active	0.3	Low	CMOS	Y	
LDO Voltage Regulator	NATIONAL-SEMI	LM1117T-3.3	TO-220	2	Active	0.3	Low	BIPOLAR	Y	
RS232 Driver/Receiver Chip	MAXIM	MAX232AEPE	DIP	1	Active	0.2	Low	CMOS	Y	
16 Channel Analog Multiplexer	ANALOG DEVICES	ADG406BN	DIP	4	Active	0.8	Low	BICMOS	Y	
4 Channel Analog Multiplexer	ANALOG DEVICES	ADG409BN	DIP	1	Active	0.1	Low	CMOS	Y	
16-Bit A/D Converter	ANALOG DEVICES	AD976BN	DIP	1	LTB	6.9	High	BICMOS	N	
2.5V High Precision Reference	ANALOG DEVICES	AD780BN	DIP	2	Obsolete				Y	
Precision Instrumentation Amplifier	BURR BROWN	INA114BP	DIP	1	Active	0	Low	NA	Y	
Ultra Low Offset Voltage OPAMP	ANALOG DEVICES	OP07CP	DIP	1	Obsolete	9.6	Danger	BIPOLAR	Y	
DC-DC Converter	C&D Technologies	BWR-12/625-D5A	DIP	1	Obsolete	8.8	Danger	HYBRID	Y	
Voltage Regulator	TEXAS INSTRUMENTS	UA78L05ACLP	TO-92	1	Active	0.1	Low	BIPOLAR	Y	
Octal Bus Transceiver	ST-MICRO	M74HCT245B1R	DIP	1	Obsolete	8.6	Danger	CMOS	Y	
3-8 Decoder	ST-MICRO	M74HC138B1R	DIP	1	Obsolete	7.8	Danger	CMOS	Y	
Quad 2 Input AND Gate	ST-MICRO	M74HC08B1R	DIP	1	Active	0.3	Low	CMOS	Y	
Hex Inverter	ST-MICRO	M74HC04B1R	DIP	1	Active	0.2	Low	CMOS	Y	
Quad 2 Input OR Gate	ST-MICRO	M74HC32B1R	DIP	1	Obsolete	6.9	High	CMOS	Y	
Octal D-Type Latch	ST-MICRO	M74HC373B1R	DIP	1	Obsolete	6.9	High	CMOS	Y	
Octal D-Type Latch with Clear	ST-MICRO	M74HC273B1R	DIP	1	Obsolete	7.2	High	CMOS	Y	
Seven Darlington Array	ST-MICRO	ULN2003A	DIP	1	Active	0	Low	BIPOLAR	Y	
11.0592MHz Crystal	OSCILENT	142-11.0592M-32-05W	THRO' HOLE	1	Unknown	6.3	High		Y	
3mm Red Color LED	AVAGO	HLMP-1321	THRO' HOLE	1	Active	0.6	Low		Y	
3mm Green Color LED	AVAGO	HLMP-1521	THRO' HOLE	1	Active	0.6	Low		Y	

The color coding for obsolescence risk analysis is as shown below:

- Low Risk
- Medium Risk
- High Risk
- Danger
- Status Unknown

The obsolescence status of components present on RTU card is shown in Pi chart in Figure 8. From this chart it is evident that 60% components are under active stage and 20% components are obsolete for which there is no support from vendors. Hence proper action should be initiated to mitigate this obsolescence.

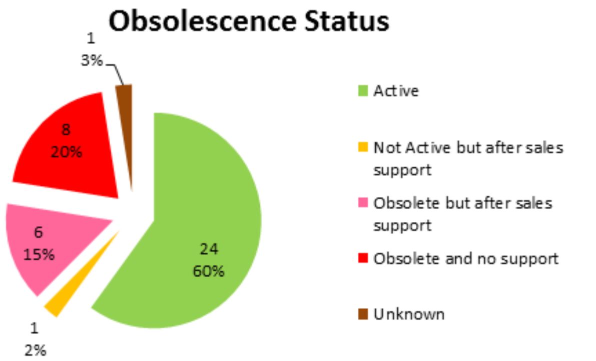

Figure 8: Obsolescence status of components in RTU card

V. OBSOLESCENCE MANAGEMENT STRATEGIES

Obsolescence management strategies can be broadly classified into Reactive and Proactive Management. In reactive management, once the obsolescence of component occurred, action shall be taken to fix the problem immediately. However it is important to do the risk analysis of all components in the BOM, before choosing a reactive strategy. If the obsolescence of a component has low impact on plant safety and downtime, then it may be advisable to use a reactive strategy as these strategies are easier to implement. If the probability of obsolescence is low and the impact on plant safety and downtime is high, then it is advisable to use proactive mitigation measures. If both the probability of obsolescence and impact on plant safety & downtime are high, then these components are regarded as 'critical' and hence, it is necessary to adopt a proactive mitigation strategy. Figure 9 shows the four quadrants of obsolescence management strategies.

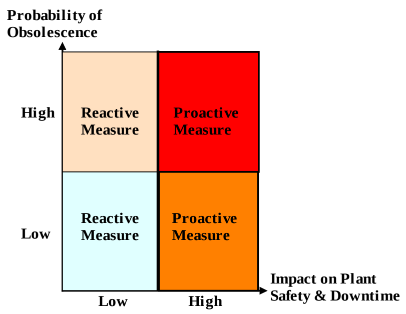

Figure 9: Obsolescence management strategies

Design Refresh Planning

The objective of design refresh planning is to determine, when to do design refresh, what obsolete system components should be replaced and how much non-obsolete system components should be retained in new design. It is required to devise a methodology that determines the best dates for design refreshes.

To address this issue we have designed soft-core processor based RTU card by implementing the glue logic along with 8051 microcontroller present in existing RTUs into a single FPGA. Implementation of glue logic is done in VHDL and TSK51 soft-core is used in place of 8051 microcontroller as shown in Figure 10. This reduces component count and power consumption apart from obsolescence issue and thereby achieving a higher reliability than before. This illustrates how the life of an electronic design can be extended to provide longevity, when components used in the first scheme become obsolete. The design started life as a discrete component in DIP package. Due to obsolescence of microcontroller from a particular manufacturer, the RTU was redesigned using FPGA. With the functionality of the previous design was protected, the design was mostly concerned with the interface between TSK51 and glue logic. To protect future iterations the code was transferred into VHDL. The life expectancy of this device is at least another 15-20 years.

Figure 10: Soft-core Procesor based RTU Card

VI. CONCLUSION

In long-life cycle projects, component obsolescence has become a major problem as it prevents the maintenance of the system. In order to manage obsolescence effectively, it is essential to perform an obsolescence risk assessment for the Bill-of-Materials. The best practice in managing obsolescence of component is demonstrated by using FPGA in place of discrete components as mitigation strategy in our case study of RTU card. The key factors that have to be analyzed in the obsolescence risk assessment process for each BOM are the failure rate and functional impact criticality. For very high risk components like microcontrollers and microprocessors, a reactive approach is required to inform the decisions regarding the most suitable mitigation strategies. On the contrary, for low risk components like resistors, capacitors and inductors, a fully proactive approach is appropriate and cost effective. This process has been validated using case study for RTU cards used in PFBR. Using layered modular design and configurable mitigation methodologies, it is possible to provide future design support which can introduce new operational requirements at the later date.

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